Virtex US+ FPGA Discrete Power Solution

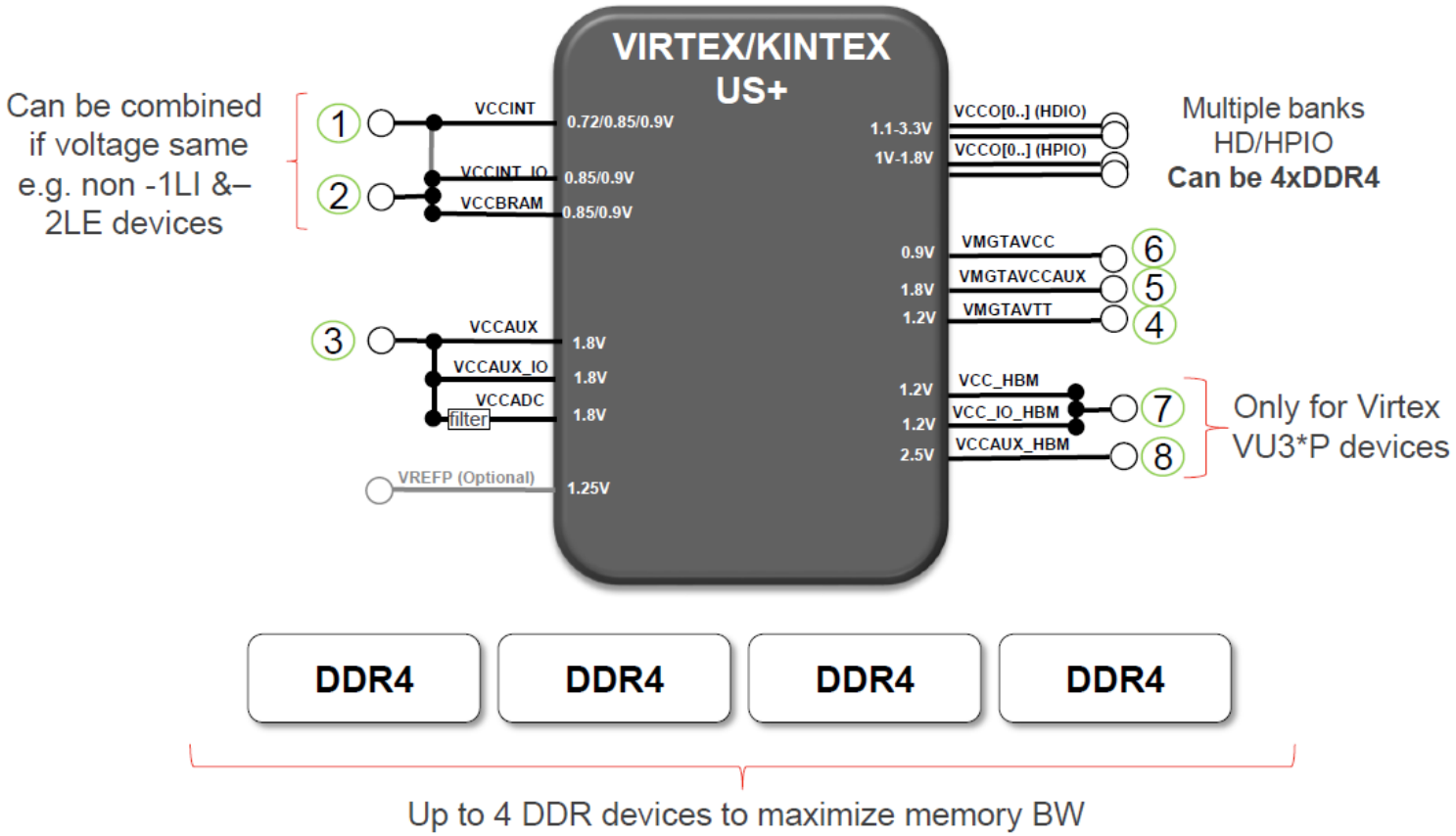
June 18, 2018

Simple, Easy Solutions™

rev 20170706

Power Rail Combination options

Rail Combination Options



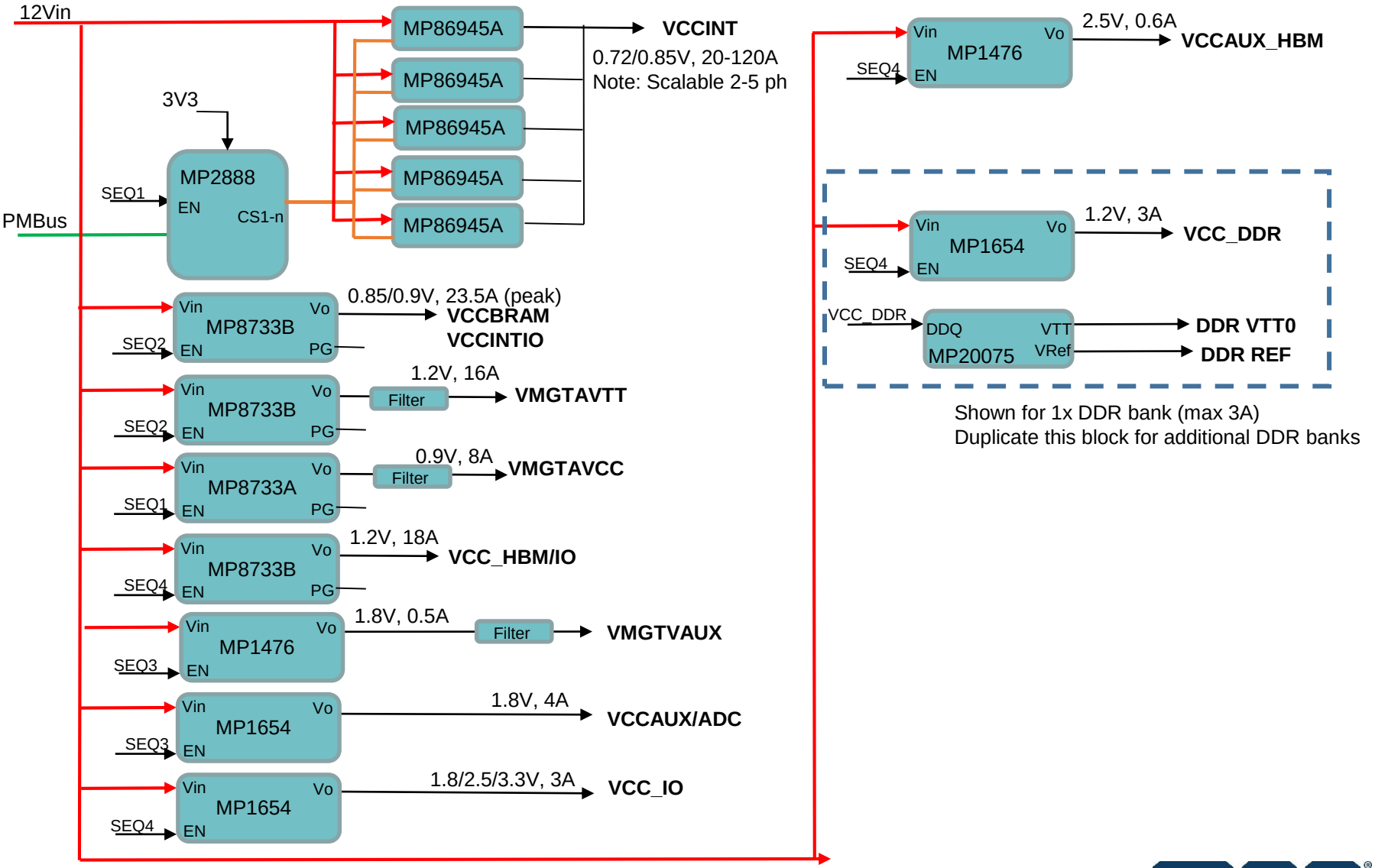
VirtexUS+ Power Requirements

Vin=12V

Rail#	Rail	Voltage	Ripple (DC+AC)	Step Load	Comments	VirtexUS+
1	VCCINT	0.72/0.85/0.9V	±3%	25%	Assume up to 100A/us 25% load steps	20-120A
2	VCCBRAM/INT_IO	0.85/0.9V	±3%	40%	Normally tied to VCCINT, except for -L devices	1-25A
3	VCCAUX/ADC	1.8V ±3%	±3%	90%	Additional current may be needed for 1.8V IO	1-4A
4	VMGTAVTT	1.2V	±3%	25%	10mV pk-pkripple at FPGA pins. See UG578	5-16A
5	VMGTVCCAUX	1.8V	±3%	25%	10mV pk-pkripple at FPGA pins. See UG578	0.2-0.5A
6	VMGTAVCC	0.9V	±3%	25%	10mV pk-pkripple at FPGA pins. See UG578	2-8A
7	VCC_HBM/IO	1.2V	±3%	80%	For VirtexUS+ only	0-18A
8	VCCAUX_HBM	2.5V	±3%	80%	For VirtexUS+ only	0-0.6A
9	VCC_IO	1.8/2.5/3.3V	±5%	90%	IO current varies widely depending on app	
10	VCC_DDR	1.2V		80%	Upto 4 Ext. DDR.	
11	DDR_VTT	VCC_DDR/2			Upto 4 Ext. DDR.	
12	DDR_VREF	VCC_DDR/2			Upto 4 Ext. DDR.	

Assume 10A/us for all rails except VCCINT

VirtexUS+ Lowest cost (Discrete)



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Key Features VirtexUS+ (Discrete)

VIN 12V +/-5%

Rail	VOUT	Ripple	Load	Step Load	Seq Up/Dwn	MPS Part#		pcb Area (mm2)	Efficiency @ 50% load
VCCINT	0.72/0.85/0.9V	+/-3%	20-120A	25%	1/4	MP2888 cntrl 5x MP86945A		1220	92.00%
VCCBRAM/VCCINTIO	0.85/0.9V	+/-3%	0.5-23.5A	40%	2/3	MP8733B		216	88.00%
VCCAUX/ADC	1.8V	+/-3%	1-4A	90%	3/2	MP1654		90	90.50%
VMGTAVTT	1.2V	+/-3%	5-16A	25%	2/3	MP8733B		216	89.00%
VMGTVCCAUX	1.8V	+/-3%	0.2-0.5A	25%	3/2	MP1476		90	86.00%
VMGTAVCC	0.9V	+/-3%	2-8A	25%	1/4	MP8733A		216	90.00%
VCC_HBM/IO	1.2V	+/-3%	0-18A	80%	4/1	MP8733B		216	89.00%
VCCAUX_HBM	2.5V	+/-3%	0-0.6A	80%	4/1	MP1476		90	89.00%
VCC_IO	1.8/2.5/3.3V	5%	3A	90%	4/1	MP1654		90	94.00%
VCC_DDR	1.2V	5%	3A	80%	4/1	MP1654		90	88.00%
DDR_VTT DDR_REF	VCC_DDR/2	5%	3A	80%	4/1	MP20075		19	
							sq mm	2553	
						Total	sq in	3.96	90.8%

Efficiency ~91%, size ~4.0sqin

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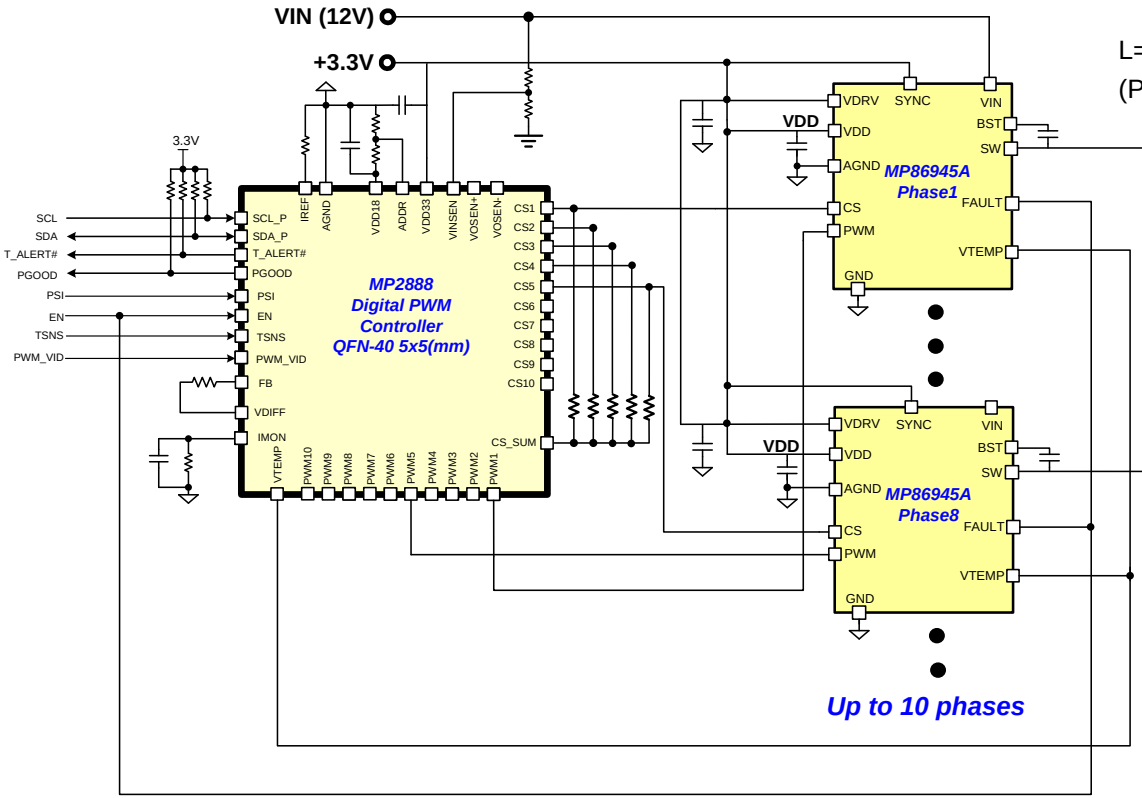
Overview – VirtexUS+

- 12Vin design (no intermediary regulator required)
- Design can be easily scaled/modified for customer requirements
- Common use of parts allow step and repeat for easy design

- Lowest cost
  - Scalable 5ph design (120A VCCINT) for high efficiency and fast transient response
  - Total system efficiency ~ 91%
  - Total solution size ~4.0 sqin including input & output Caps

MP2888 + MP86945A (VCCINT) 120A

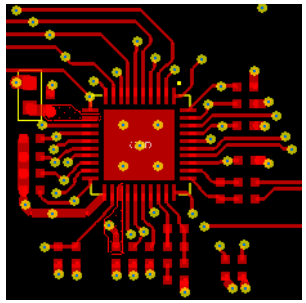
Schematics

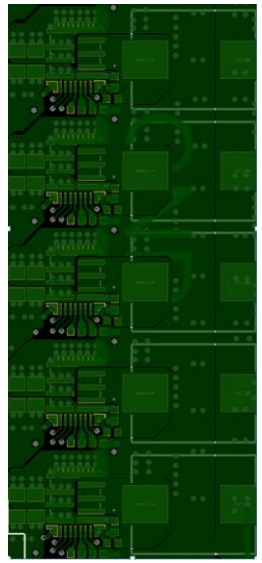


L=150nH

(Panasonic ETQP3LR15CFM, 0.66mOhm, height=3mm)

Layout guidelines





Caps included in area calculations:

Input Caps: 12x Ceramic 1210 caps, 47uF/16V, Murata GRM32ER71C476ME01L

Output Caps: 12x Ceramic 1210 caps, 330uF/2.5V, Murata GRM32EC80E337ME01L on PCB top,

28x 22uF 0603 on PCB bottom

Solution size:

Controller: 215mm^2

Power Stages (5x153) = 765mm^2

Input Caps 24x 1210 on top = 120mm^2

Output Caps 24x 1210 on top = 120mm^2

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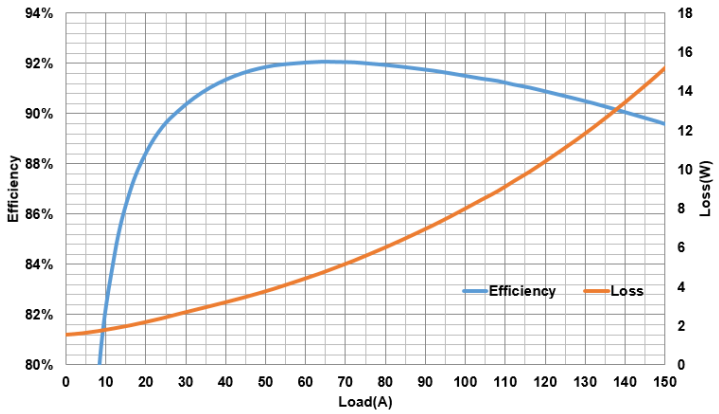
VCCINT Design details

Controller MP2888

- ❑ *Programmable Multi-phases up to 10phases*
- ❑ *Automatic loop compensation*
- ❑ *Excellent Transient Performance*
- ❑ *Less External Component than Analog Cntrl*
- ❑ *PMBus compliant with Built-in NVM*
- ❑ *Input and output voltage, current, power and temperature monitoring*
- ❑ *UVLO/OVP/UVP/OCP/OTP protection*
- ❑ *Digital Load Line Regulation*
- ❑ *RoHS compliant 5x5 QFN-48*

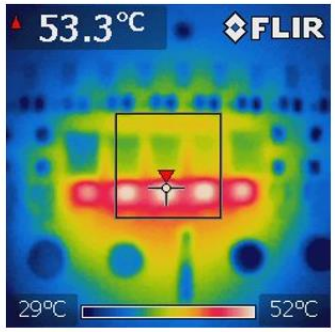
Test Condition: $12V_{IN}$, $0.85V_{OUT}$, 500kHz, L=120nH(0.125mOhm), 5phases APS Off, 400FPM airflow, cap to cap, including 3.3V(Vdrv) loss



DrMOS MP86945A

- ❑ *Wide 4.5V to 16V Operating Input Range*
- ❑ *60A Output Current*
- ❑ *Current Sense: Accu-Sense™*
- ❑ *Temperature Sense*
- ❑ *Accepts Tri-State PWM Signal*
- ❑ *Current Limit Protection*
- ❑ *Over Temperature Protection(OTP)*
- ❑ *Fault Reporting*
- ❑ *TQFN(4mmx5mm) Package*

Test Condition: $12V_{IN}$, $0.85V_{OUT}$/120A, With 2m/s(400FPM) Airflow , Ambient Temp 25°C



MP86945A Vtemp Pin voltage: 0.45V
DrMos junction temperature: 55°C
T_j=(Vtemp+100mV)/10mV
VTEMP Gain=10mV/°C

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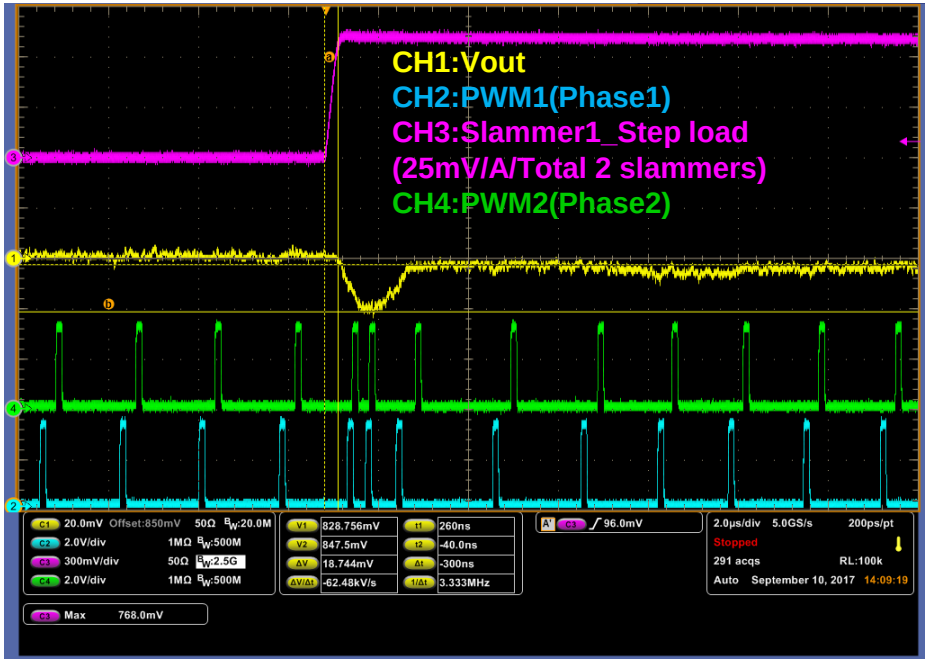
VCCINT: Load Transient 50% step (100A/µs)

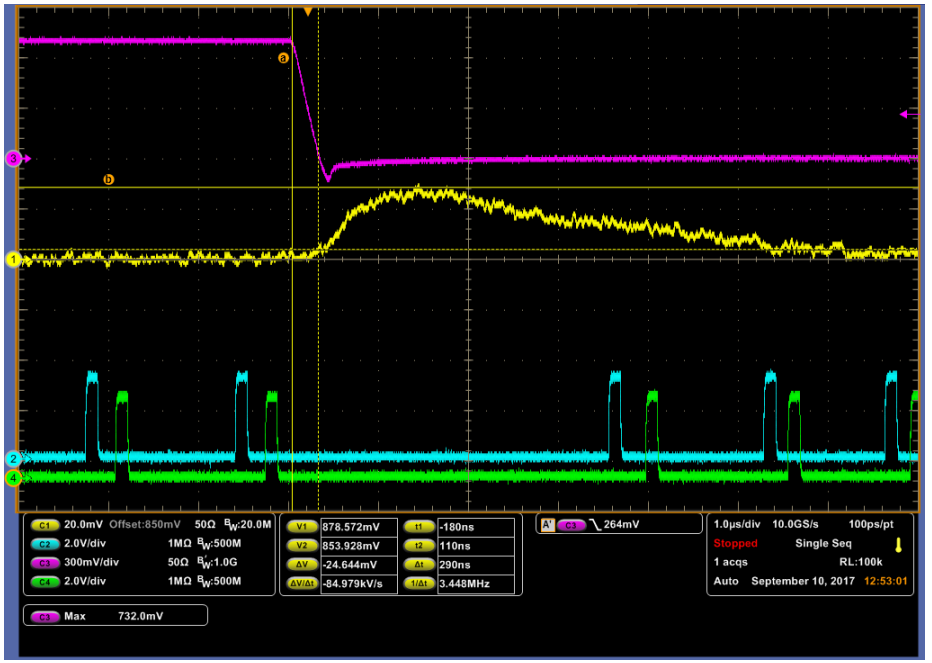
- $12V_{IN}$, $0.85V_{OUT}$, 60->120A Undershoot



Negative excursion measurement

Undershoot: 18mV

- $12V_{IN}$, $0.85V_{OUT}$, 120->60A Overshoot



Positive excursion measurement

Overshoot: 25mV

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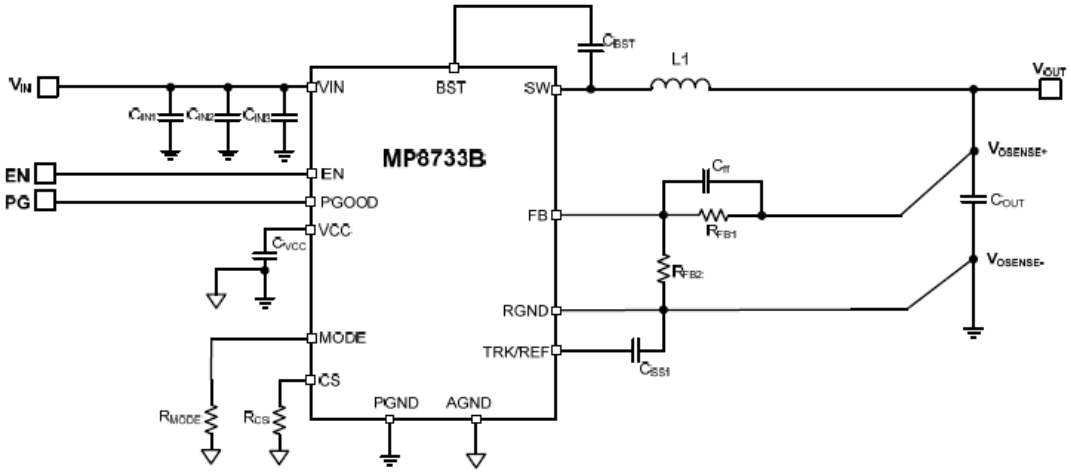
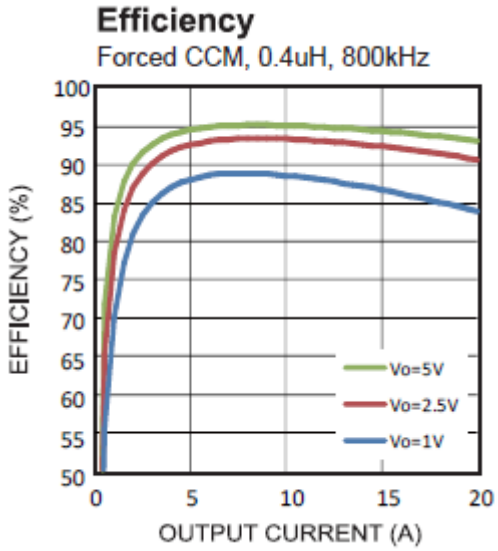
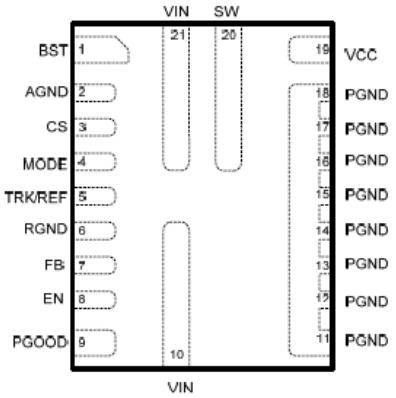
MP8733A/B

Schematics

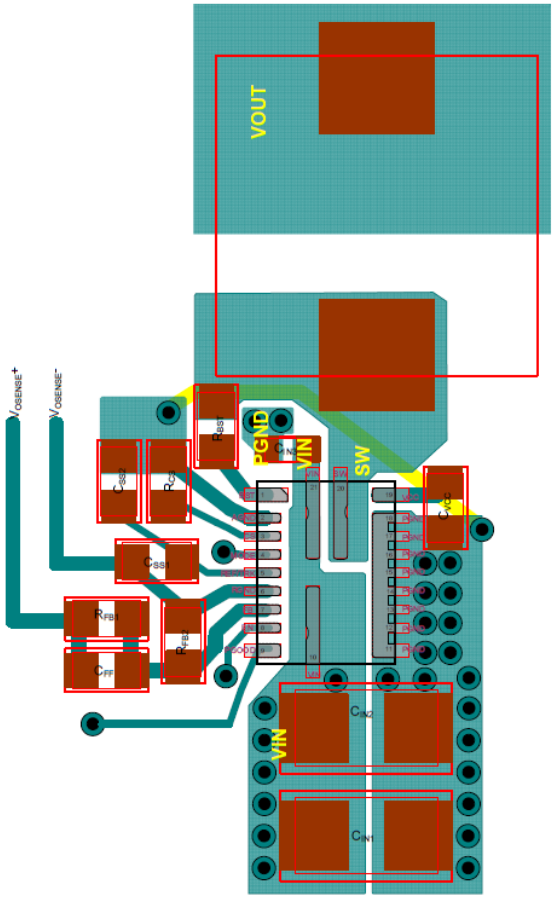






QFN-21 (3mmx4mm)

Layout guidelines



Solution size: 216mm^2

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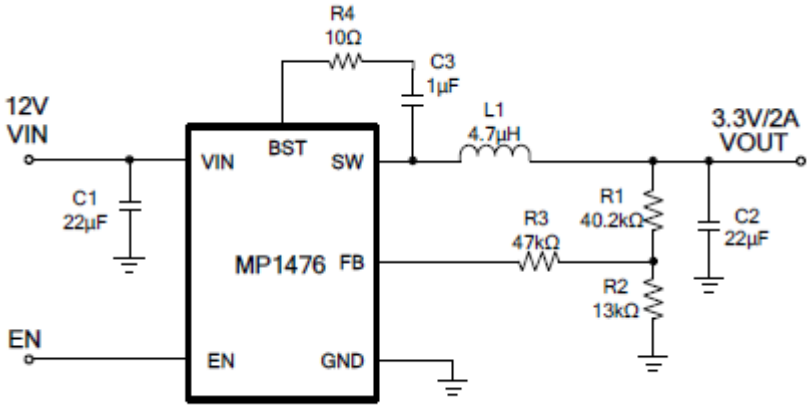
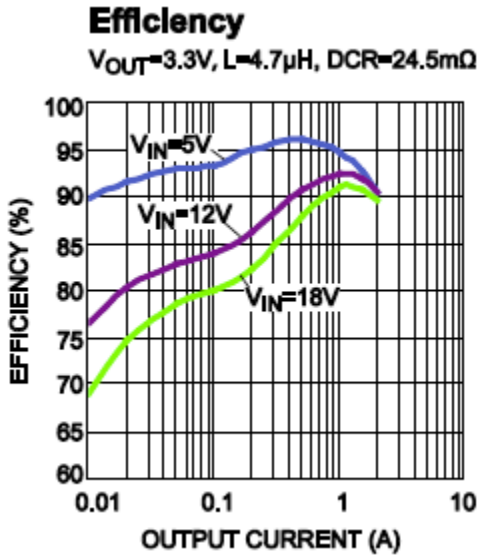
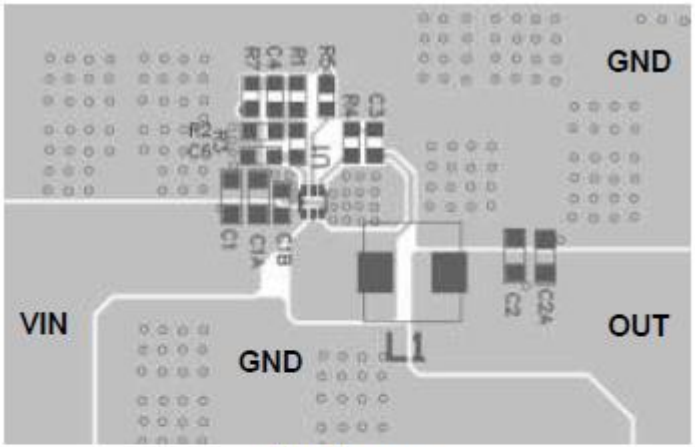
MP1476

Schematics

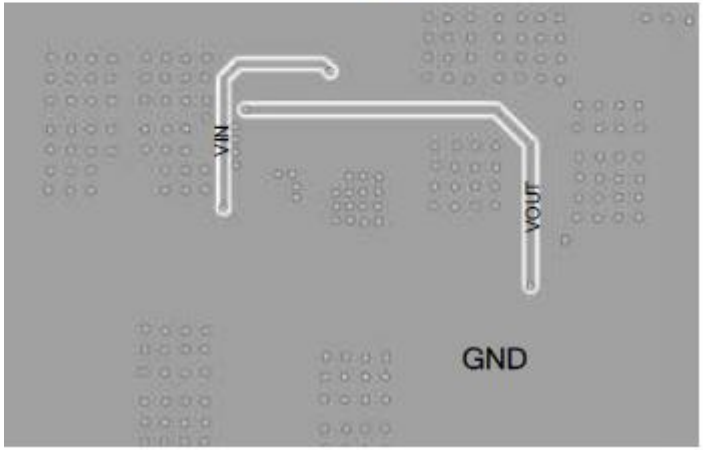




Layout guidelines



Top Layer



Bottom Layer

Solution footprint: 90mm2

External components: 9

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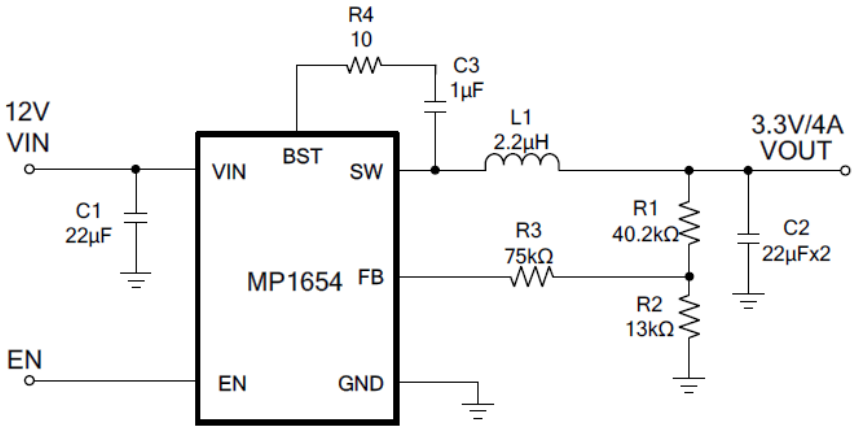
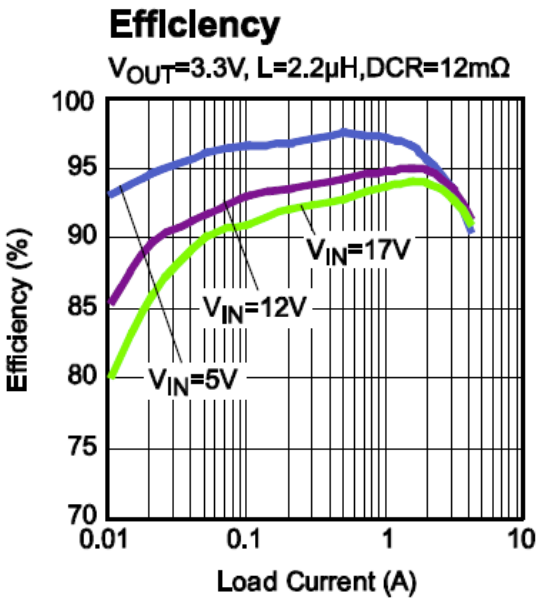
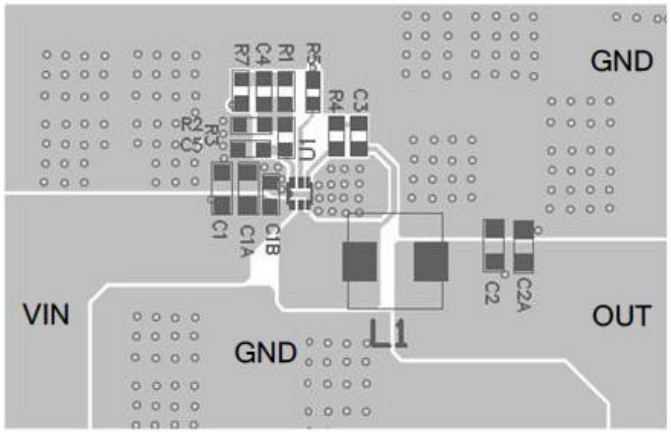
MP1654

Schematics





Layout guidelines



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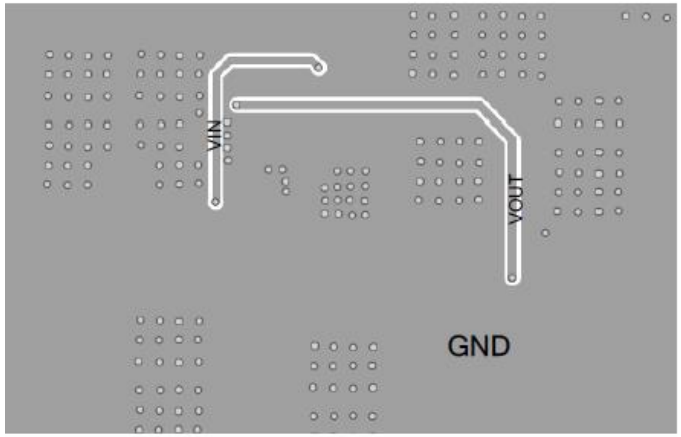

Bottom Layer

Solution footprint: 90mm2

External components: 9

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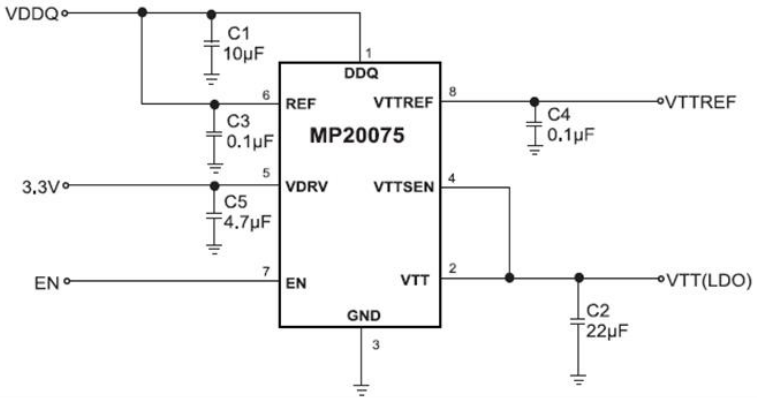
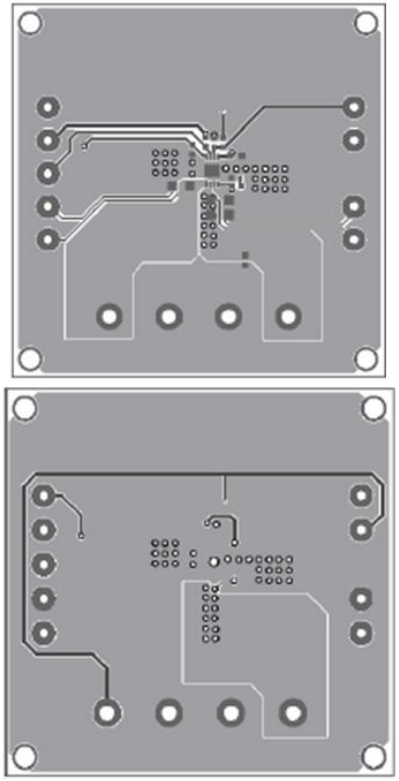
Schematics (Typical)



Layout guidelines



- For DDR4VTT
- Solution footprint: 19mm^2
- External Components:5

Caps included in area calculations:

Output Caps 1x 22uF 0805, 1x 0603 on PCB bottom

Input Caps: 3x 0603 on PCB bottom

MPS Support

MPS support for Xilinx customers

- Engineering support for design reviews, bring up and debug
- Our FAEs can assist with optimizing reference designs for customer's exact requirements
- MPS already working with leading SoC vendors and have support teams already in place for reference designs
- Power FAEs located in all major territories for world wide support

Simulation tools:

- Models available for predicting Efficiency, Power loss, Load step response, Phase margin and other key requirements.

Evaluation

- EVBs available
- MPS can provide free samples for evaluation and prototyping

MPS contact Thomas.fenn@monolithicpower.com

MPS Reference Design Team at referencedesign@monolithicpower.com

For general information
http://www.monolithicpower.com

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