Virtex US+ FPGA Module Power Solution

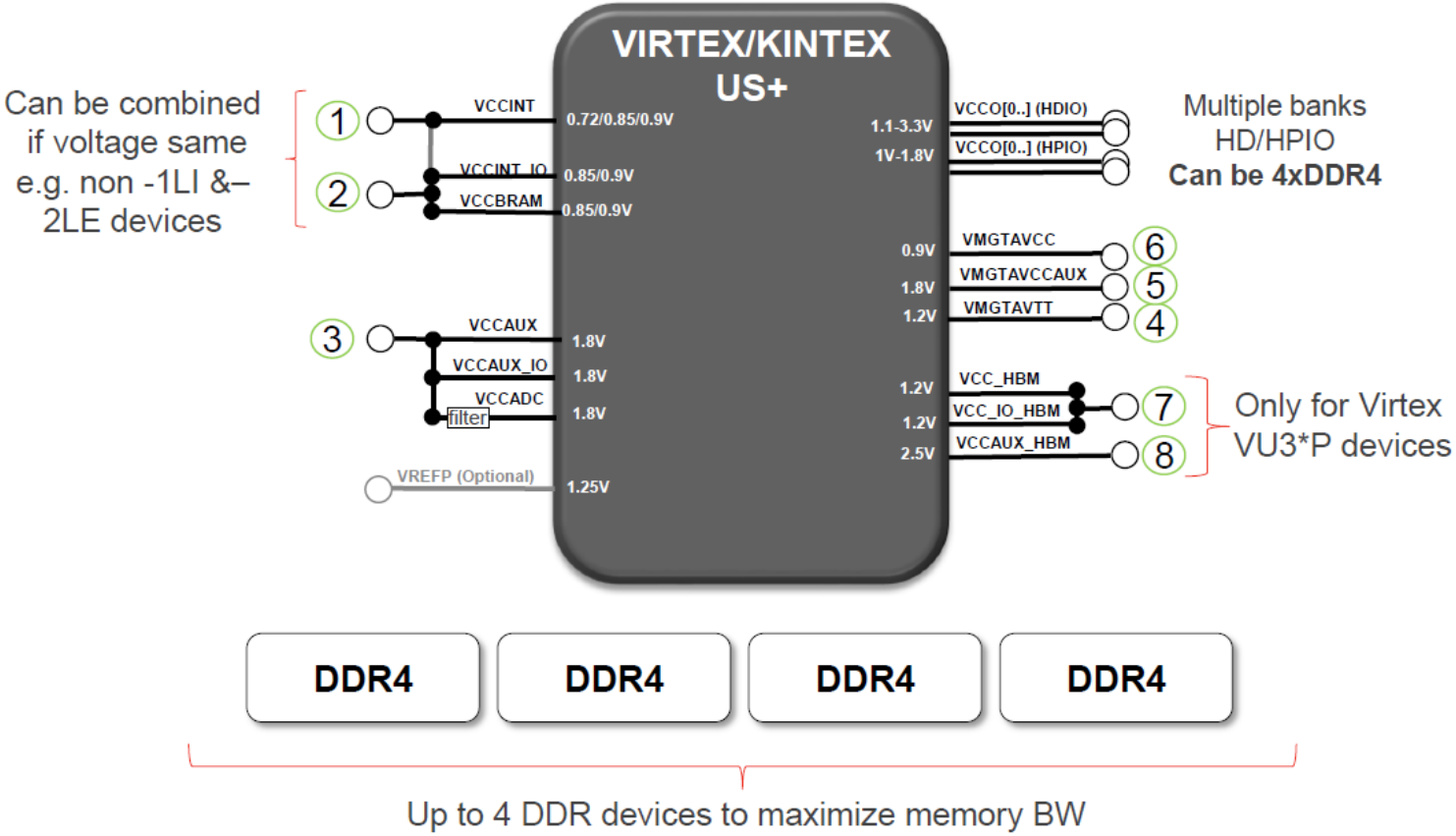
June 18, 2018

Simple, Easy Solutions™

rev 20170706

Power Rail Combination options

Rail Combination Options



VirtexUS+ Power Requirements

Vin=12V

Rail#	Rail	Voltage	Ripple (DC+AC)	Step Load	Comments	VirtexUS+
1	VCCINT	0.72/0.85/0.9V	±3%	25%	Assume up to 100A/us 25% load steps	20-120A
2	VCCBRAM/INT_IO	0.85/0.9V	±3%	40%	Normally tied to VCCINT, except for -L devices	1-25A
3	VCCAUX/ADC	1.8V ±3%	±3%	90%	Additional current may be needed for 1.8V IO	1-4A
4	VMGTAVTT	1.2V	±3%	25%	10mV pk-pkripple at FPGA pins. See UG578	5-16A
5	VMGTVCCAUX	1.8V	±3%	25%	10mV pk-pkripple at FPGA pins. See UG578	0.2-0.5A
6	VMGTAVCC	0.9V	±3%	25%	10mV pk-pkripple at FPGA pins. See UG578	2-8A
7	VCC_HBM/IO	1.2V	±3%	80%	For VirtexUS+ only	0-18A
8	VCCAUX_HBM	2.5V	±3%	80%	For VirtexUS+ only	0-0.6A
9	VCC_IO	1.8/2.5/3.3V	±5%	90%	IO current varies widely depending on app	
10	VCC_DDR	1.2V		80%	Upto 4 Ext. DDR.	
11	DDR_VTT	VCC_DDR/2			Upto 4 Ext. DDR.	
12	DDR_VREF	VCC_DDR/2			Upto 4 Ext. DDR.	

Assume 10A/us for all rails except VCCINT

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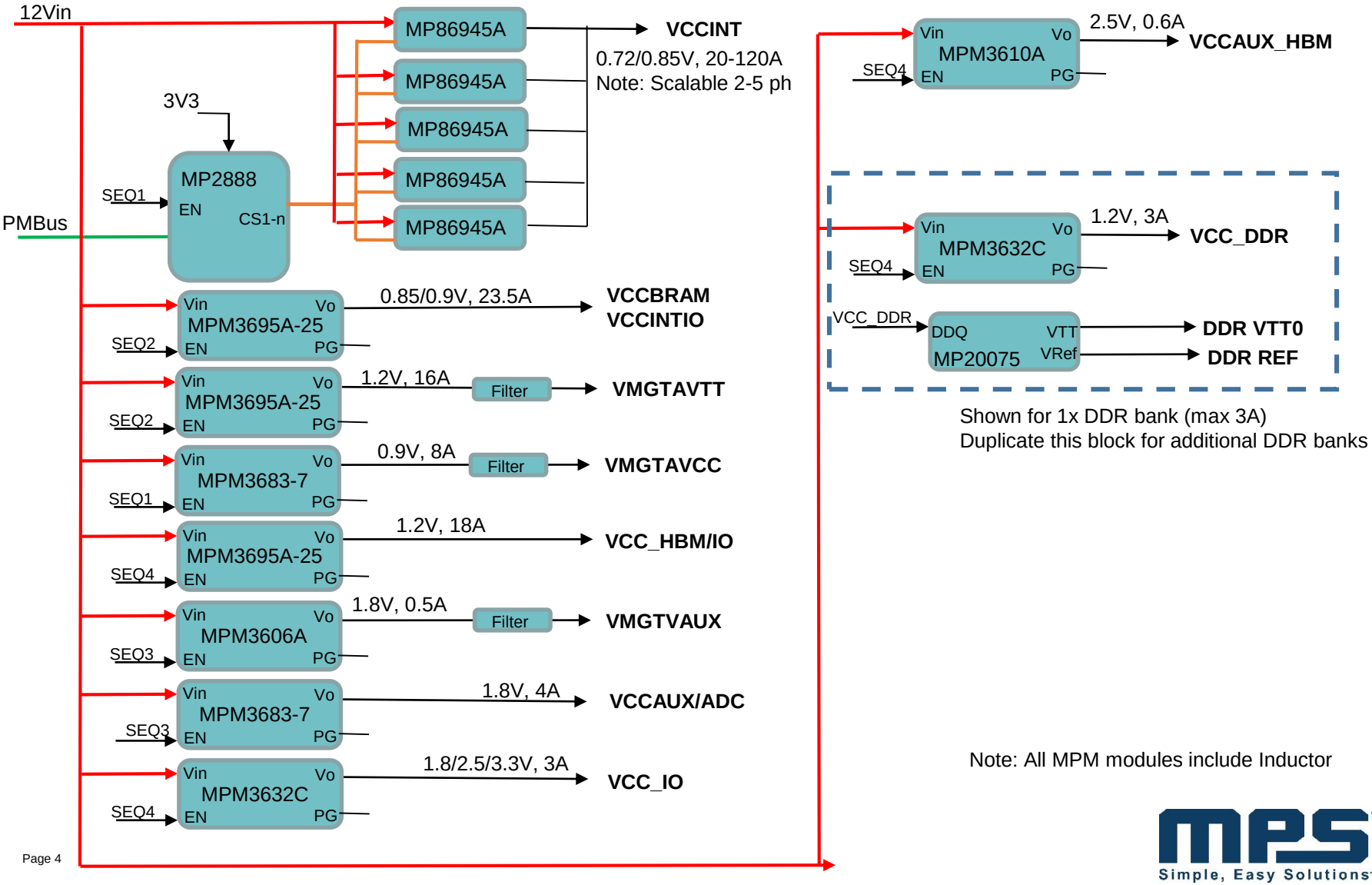
VirtexUS+ Smallest area, min effort (Modules)



Key Features VirtexUS+ (Modules)

VIN 12V +/-5%

Rail	VOUT	Ripple	Load	Step Load	Seq Up/Dwn	MPS Part#		pcb Area (mm2)	Efficiency @ 50% load
VCCINT	0.72/0.85/0.9V	+/-3%	20-120A	25%	1/4	MP2888 cntrl 5x MP86945A		1220	92.00%
VCCBRAM/VCCINTIO	0.85/0.9V	+/-3%	0.5-23.5A	40%	2/3	MPM3695A-25		230	88.00%
VCCAUX/ADC	1.8V	+/-3%	1-4A	90%	3/2	MPM3683-7		80	90.00%
VMGTAVTT	1.2V	+/-3%	5-16A	25%	2/3	MPM3695A-25		230	90.00%
VMGTVCCAUX	1.8V	+/-3%	0.2-0.5A	25%	3/2	MPM3606A		35	70.00%
VMGTAVCC	0.9V	+/-3%	2-8A	25%	1/4	MPM3683-7		80	89.00%
VCC_HBM/IO	1.2V	+/-3%	0-18A	80%	4/1	MPM3695A-25		230	89.50%
VCCAUX_HBM	2.5V	+/-3%	0-0.6A	80%	4/1	MPM3610A		35	79.00%
VCC_IO	1.8/2.5/3.3V	5%	3A	90%	4/1	MPM3632C		55	90.00%
VCC_DDR	1.2V	5%	3A	80%	4/1	MPM3632C		55	80.00%
DDR_VTT DDR_REF	VCC_DDR/2	5%	3A	80%	4/1	MP20075		19	
							sq mm	2269	
						Total	sq in	3.52	90.3%
							Note: MPM module includes inductor		

Efficiency ~90%, size ~3.5sqin

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Overview – VirtexUS+ Proposals

- 12Vin design (no intermediary regulator required)
- Design can be easily scaled/modified for customer requirements
- Common use of parts allow step and repeat for easy design

- Smallest size, Lowest Engineering effort
  - Scalable 5ph design (120A VCCINT) for high efficiency and fast transient response
  - MPM modules are fully factory tested solutions and require minimum engineering effort
  - MPM modules include inductors
  - Total system efficiency ~90%
  - Total solution size ~3.5 sqin including input & output Caps

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Design details

- Modules with integrated Inductors
  - MPM3695A-25 (25A scalable module)
  - MPM3683-7 (7A module)
  - MPM3732C (3A module)
  - MPM3610A (1A module)
  - MPM3606A (0.6A module)

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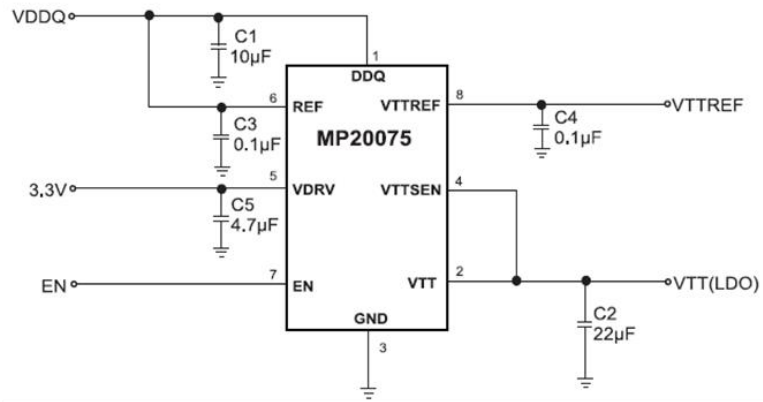
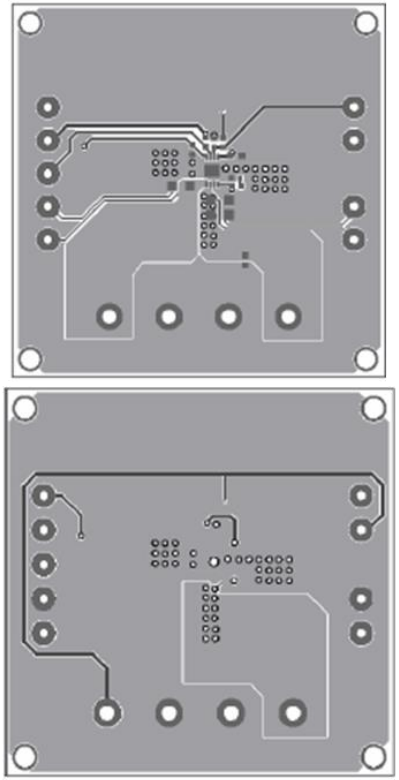
Schematics (Typical)



Layout guidelines



- For DDR4VTT
- Solution footprint: 19mm^2
- External Components:5

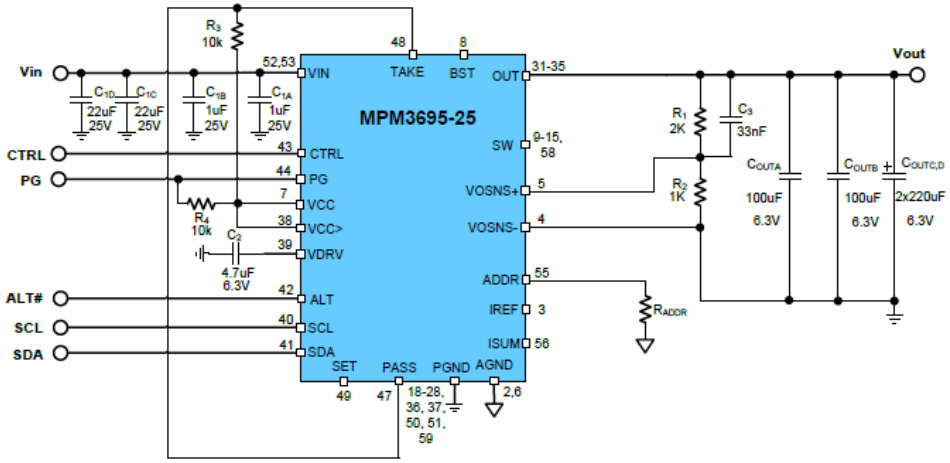
Caps included in area calculations:

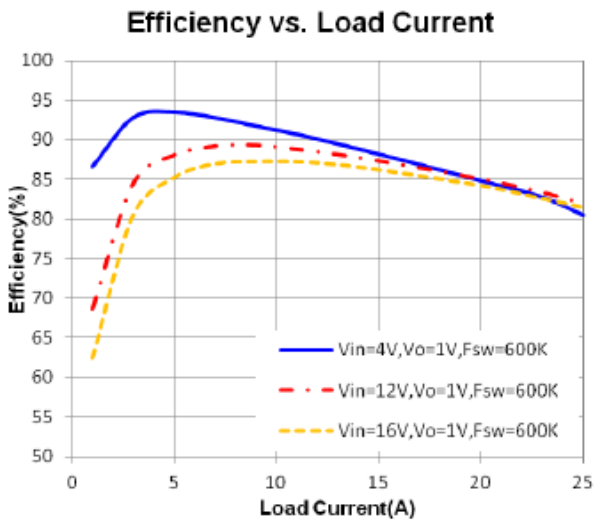
Output Caps 1x 22uF 0805, 1x 0603 on PCB bottom

Input Caps: 3x 0603 on PCB bottom

MPM3695A-25

Schematics





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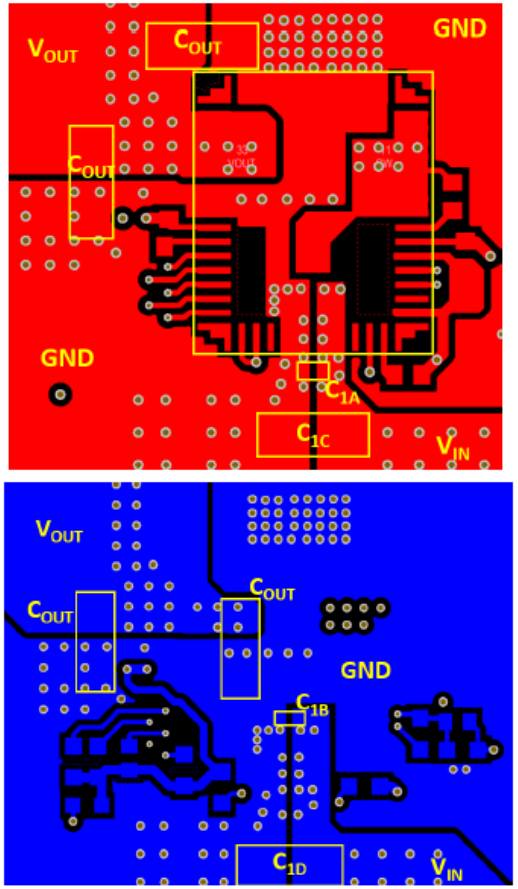
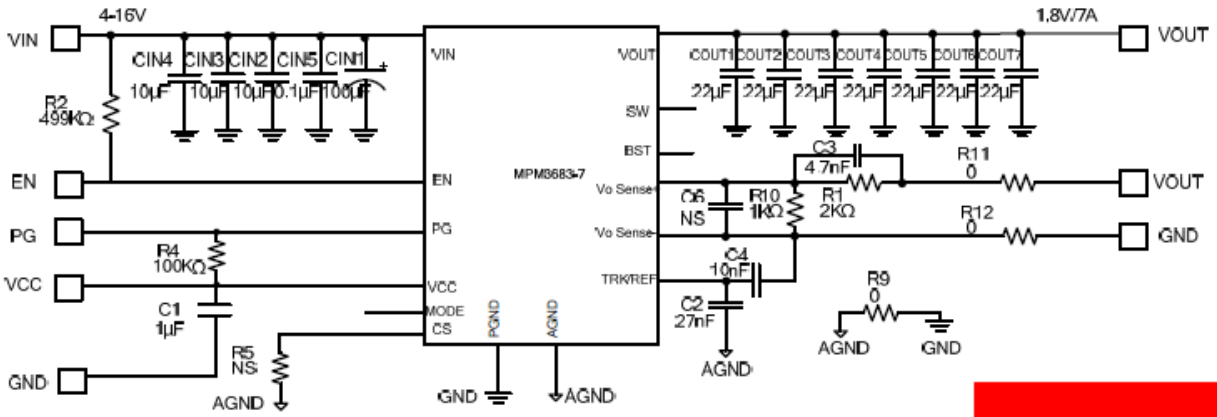
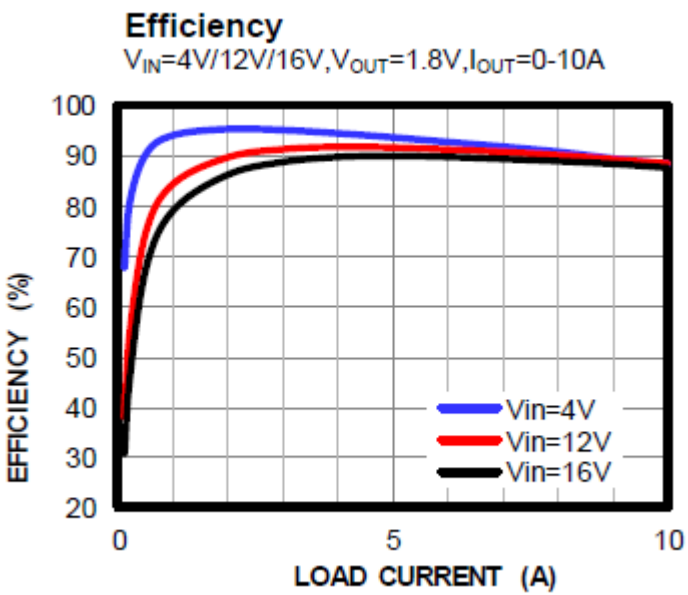


Solution size: 230mm2

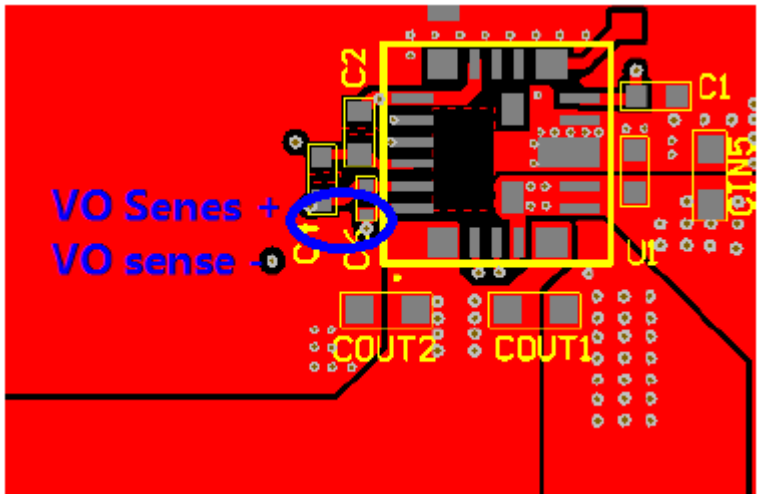
MPM3683-7

Schematics





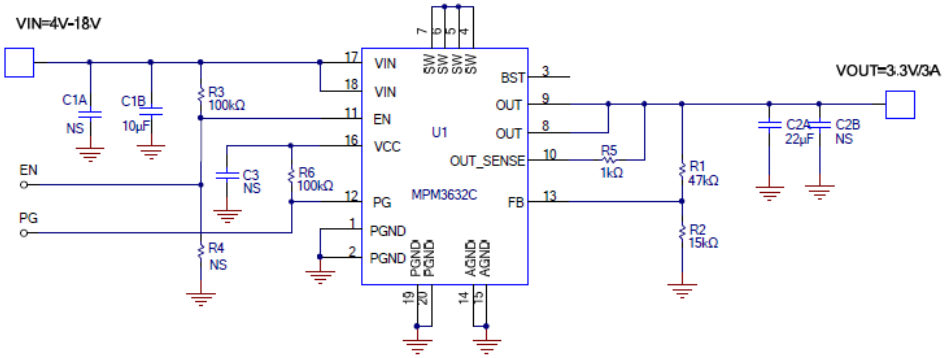
Layout guidelines



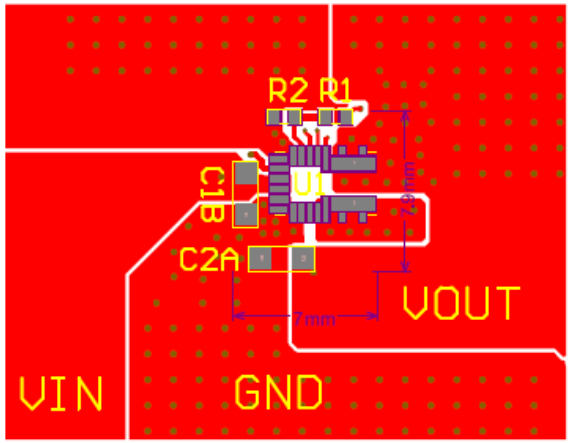
Solution size: 80mm2

MPM3632C

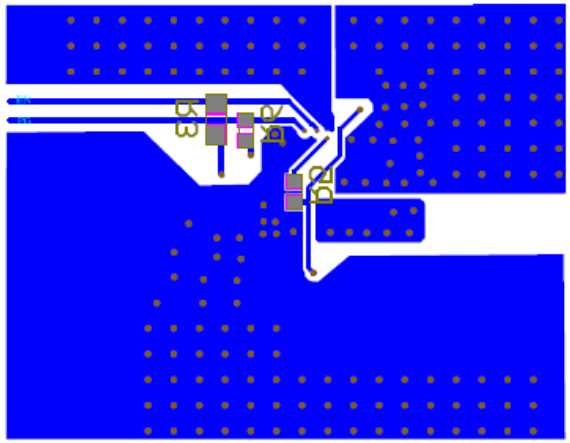
Schematics

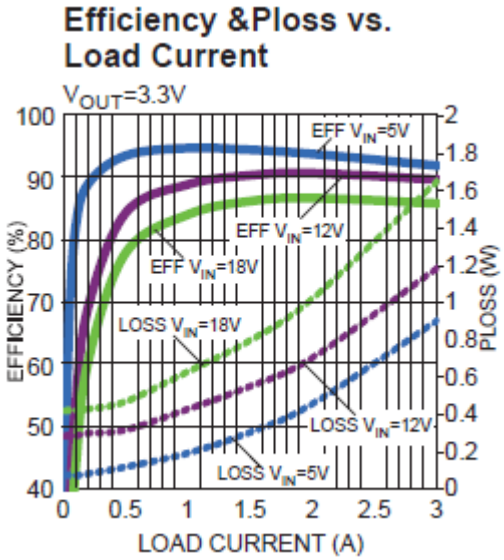


Layout guidelines



Top Layer





PCB area 55mm2

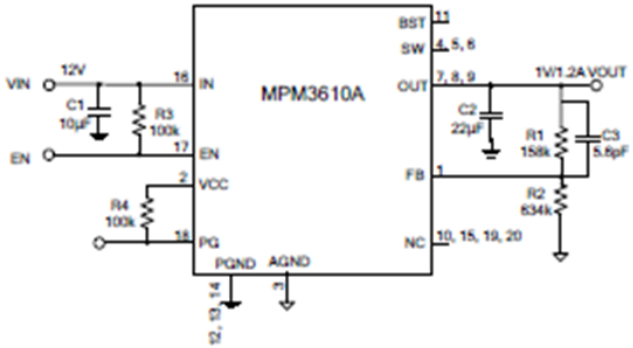
Caps included in area calculations:

Output Caps 1x 22uF 0805

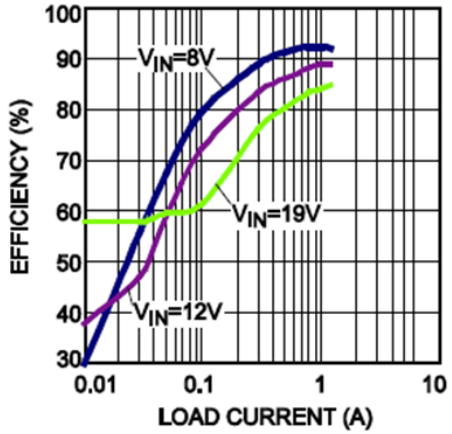
Input Caps: 2x 0603 on PCB bottom

MPM3610A

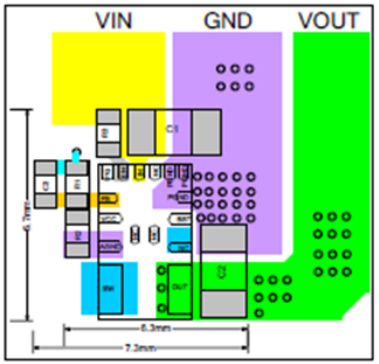
Schematics (Typical)



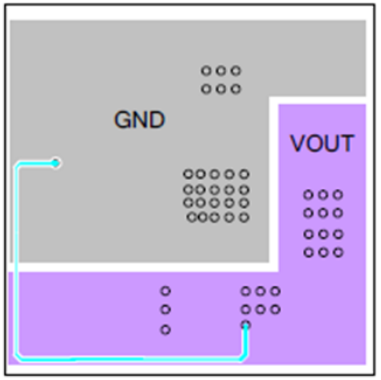
V_{OUT}=5V



Layout guidelines



Top Layer



Bottom Layer

- Solution footprint: 32mm^2
- External Components: 7

Caps included in area calculations:

Output Caps 1x 22uF 0805

Input Caps: 2x 0603 on PCB bottom

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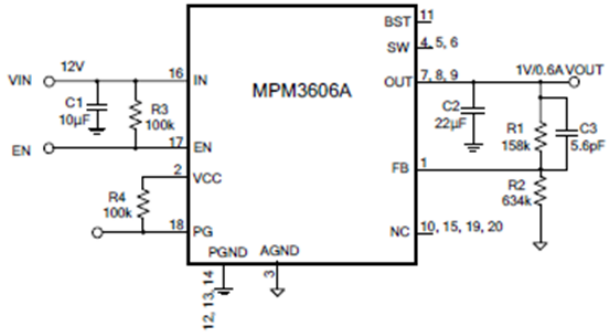
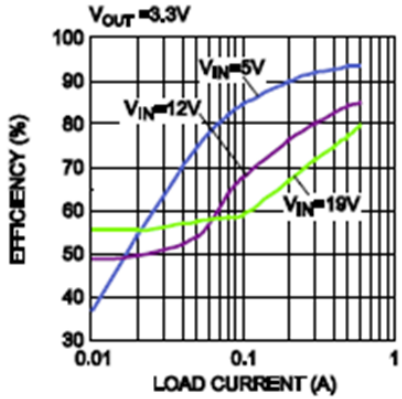
Schematics (Typical)





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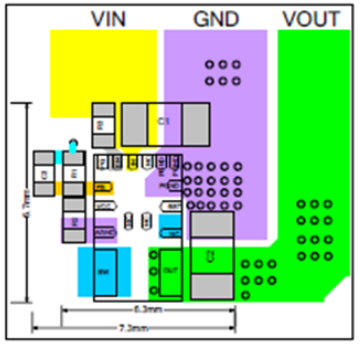
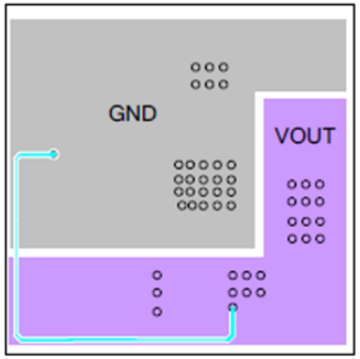


Top Layer



Bottom Layer

- Solution footprint: 32mm^2
- External Components:7

Caps included in area calculations:

Output Caps 1x 22uF 0805

Input Caps: 2x 0603 on PCB bottom

MPS Support

MPS support for Xilinx customers

- Engineering support for design reviews, bring up and debug
- Our FAEs can assist with optimizing reference designs for customer's exact requirements
- MPS already working with leading SoC vendors and have support teams already in place for reference designs
- Power FAEs located in all major territories for world wide support

Simulation tools:

- Models available for predicting Efficiency, Power loss, Load step response, Phase margin and other key requirements.

Evaluation

- EVBs available
- MPS can provide free samples for evaluation and prototyping

MPS contact Thomas.fenn@monolithicpower.com

MPS Reference Design Team at referencedesign@monolithicpower.com

For general information
http://www.monolithicpower.com

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