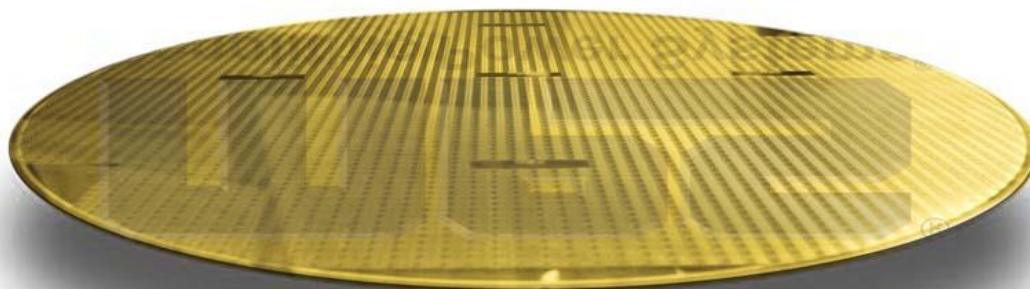


**MPS**<sup>®</sup>

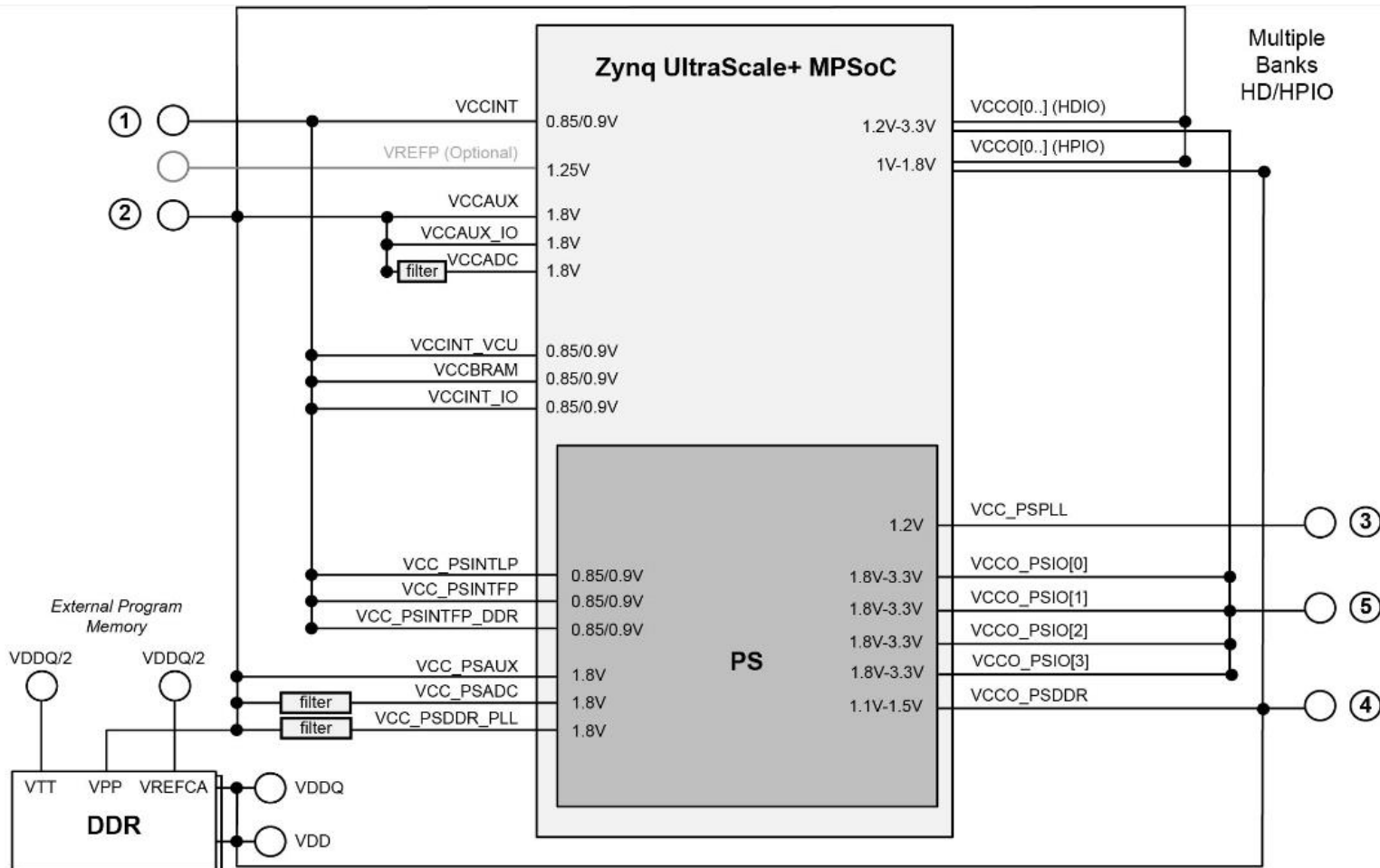
**MPS**<sup>®</sup>

**Monolithic Power Systems**<sup>®</sup>



Scalable Power Solutions for Zynq UltraScale+ MPSoC

Last update  
Feb 9, 2017



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Two configuration options:

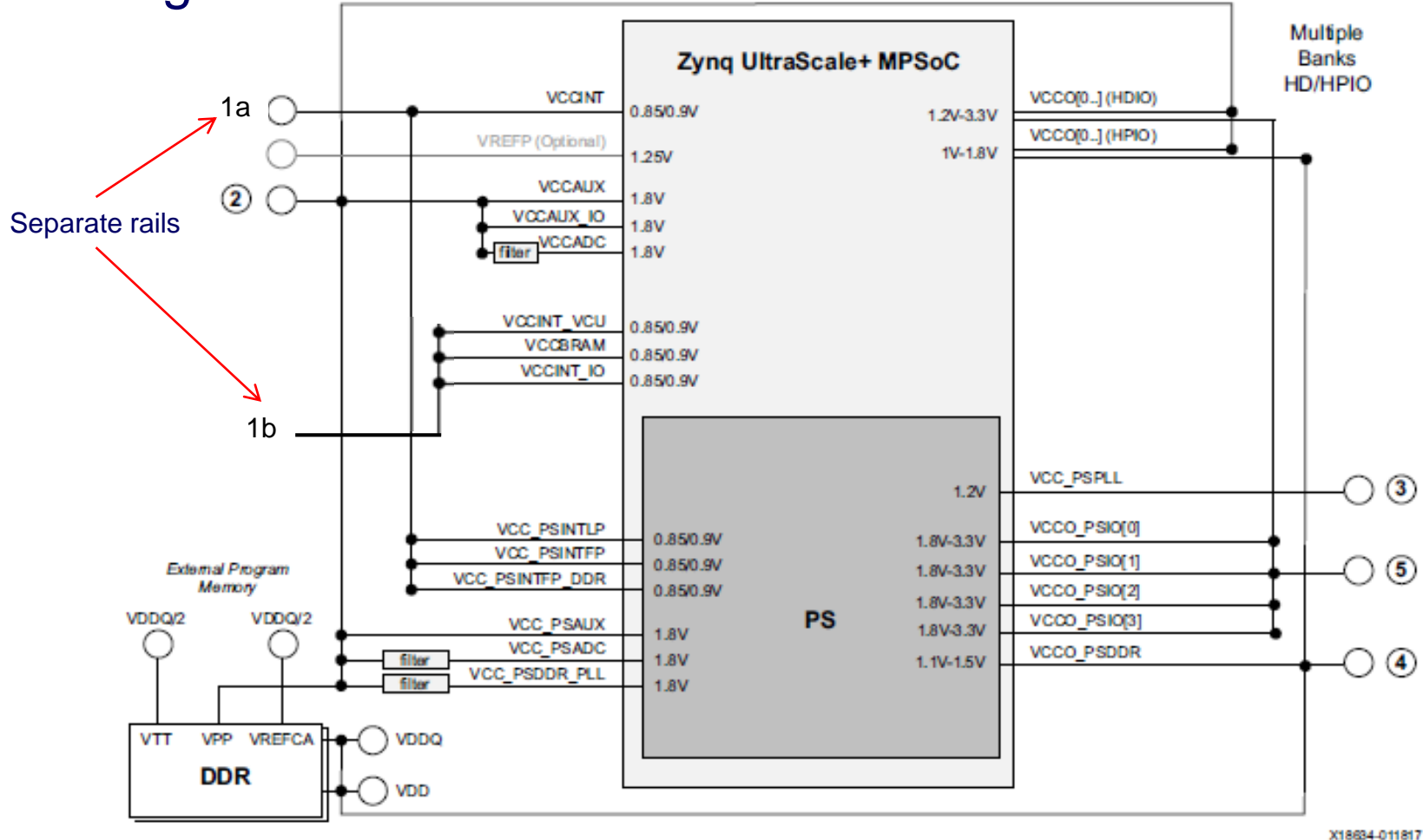
## Config1

- Separate rails for
  - VCCINT\_VCU, VCC\_PSINTF, VCC\_PSINTLP, VCC\_PSINTFP\_DDR
    - Max 4A
  - VCCINT, VCCINT\_IO, VCCBRAM
    - Max 4.5A

## Config2

- Combined rail for
  - VCCINT\_VCU, VCC\_PSINTF, VCC\_PSINTLP, VCC\_PSINTFP\_DDR, VCCINT, VCCINT\_IO, VCCBRAM
    - Max 6.0A

## Config1

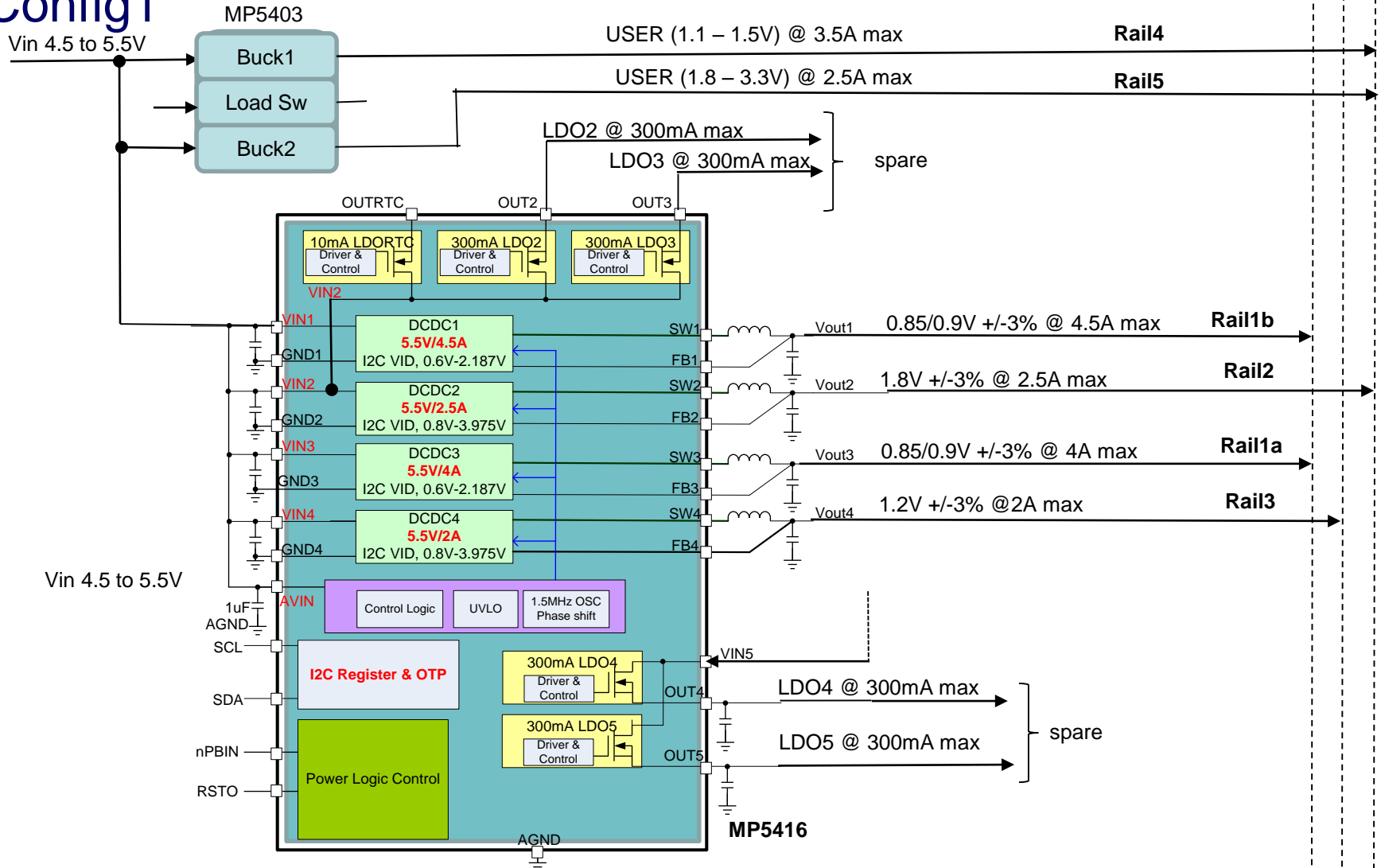




# Design Specifications – UC1-3 Always ON 5 Rails (PMICs Config1)

Rail#	Config1 Rails	Vout	max Load	MPS part#	Footprint
1a	VCCINT_VCU, VCC_PSINTF, VCC_PSINTLP, VCC_PSINTFP_DDR	0.85/0.9V +/- 5%	4A	PMIC MP5416	QFN-28(4mmx4mm)
1b	VCCINT, VCCINT_IO, VCCBRAM	0.85/0.9V +/- 5%	4.5A		
2	VCC_PSAUX, VCC_PSDDR_PLL, VCC_PSADC, VCCAUX, VCCAUX_IO, VCCADC, DDR_VPP1, VCCO(0..)HDIO, VCCO(0..)HPIO	1.8V+/-3%	2.5A		
3	no MGT, VCC_PSPLL, VCC_VCU_PLL	1.2V+/-3%	2A	mini PMIC MP5403	UTQFN-20 (2.5mmx3mm)
4	VCCO_PSDDR, DDR_VDD2, DDR_VDDQ, VCCO(0..)HDIO	USER (1.1- 1.5V)	3.5A		
5	VCCO_PSIO[0..2], VCCO(0..)HDIO	USER (1.8- 3.3V)	2.5A		

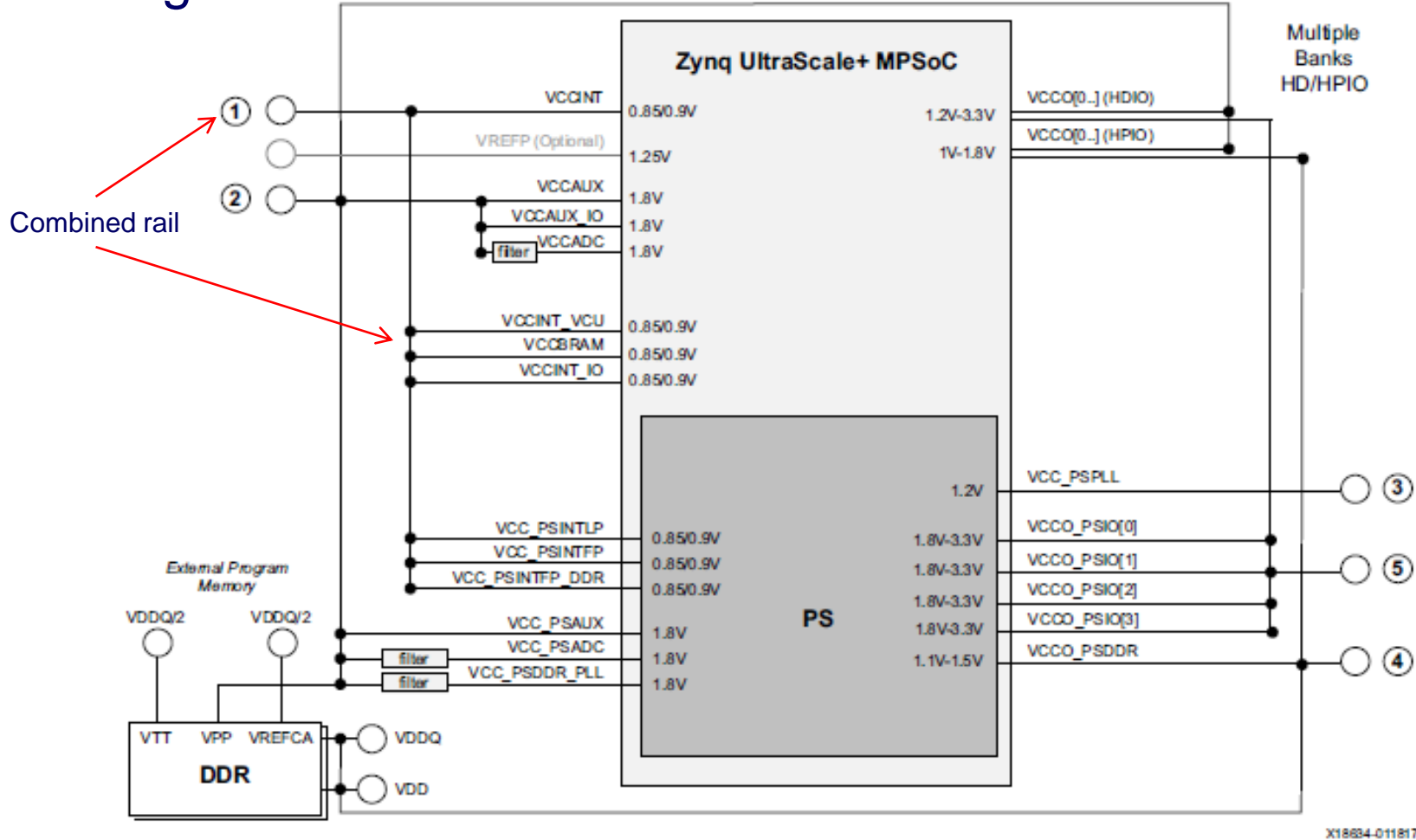
## Config1



Requires factory programming

Power on sequence 1 2 3

## Config2



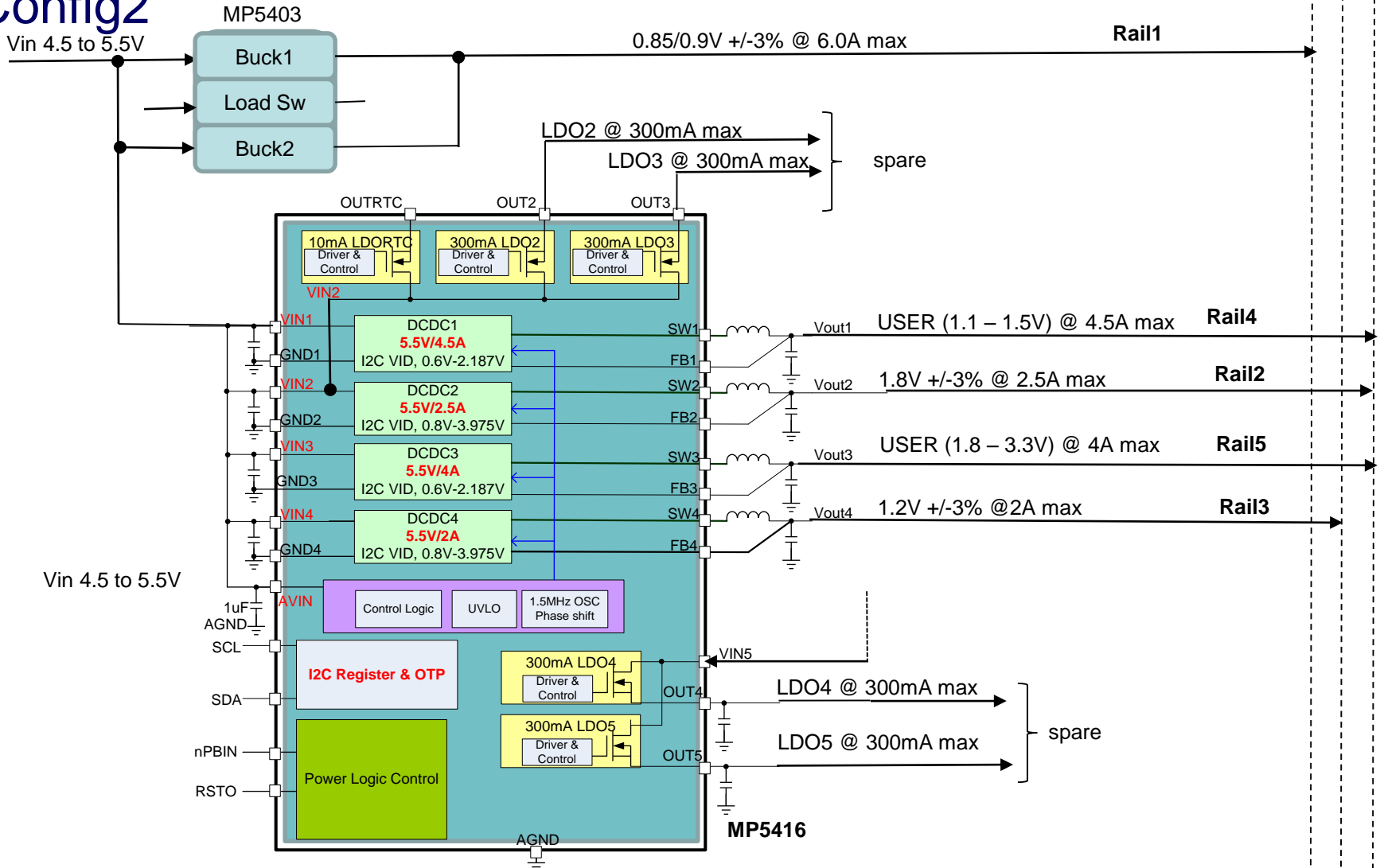


# Design Specifications – UC1-3 Always ON 5 Rails (PMICs Config2)

Rail#	Config2 Rails	Vout	max Load	MPS part#	Footprint
4	VCCO_PSDDR, DDR_VDD2, DDR_VDDQ, VCCO(0..)HDIO	USER (1.1-1.5V)	4A	PMIC MP5416	QFN-28(4mmx4mm)
5	VCCO_PSIO[0..2], VCCO(0..)HDIO	USER (1.1-1.5V)	4.5A		
2	VCC_PSAUX, VCC_PSDDR_PLL, VCC_PSADC, VCCAUX, VCCAUX_IO, VCCADC, DDR_VPP1, VCCO(0..)HDIO, VCCO(0..)HPIO	1.8V+/-3%	2.5A		
3	no MGT, VCC_PSPLL, VCC_VCU_PLL	1.2V+/-3%	2A		
1	VCCINT, VCCINT_VCU, VCCINT_IO, VCCBRAM, VCC_PSINTF, VCC_PSINTLP, VCC_PSINTFP_DDR	0.85/0.9V +/-5% 0.85/0.9V +/-5%	6.0A (combined)	mini PMIC MP5403	UTQFN-20 (2.5mmx3mm)



## Config2



Power on sequence 1 2 3



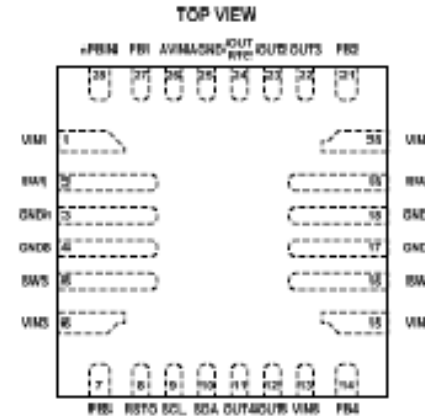
# MPS product selector – UC1-3 Always ON 5 Rails (PMICs)

5 RAILS (PMIC)	Voltage (V)	Tolerance	ZU2CG	ZU2EG (A)	ZU3CG	ZU3EG	ZU4CG	ZU4EG	ZU4EV	ZU5CG	ZU5EG	ZU5EV
Rail 1	0.85/0.9	+/-3%	PMIC - MP5416									
Rail 2	1.8	+/-3%*										
Rail 3	1.2	+/-3%*										
Rail 4	USER (1.1-1.5)		mini PMIC - MP5403									
Rail 5	USER (1.8-3.3)											

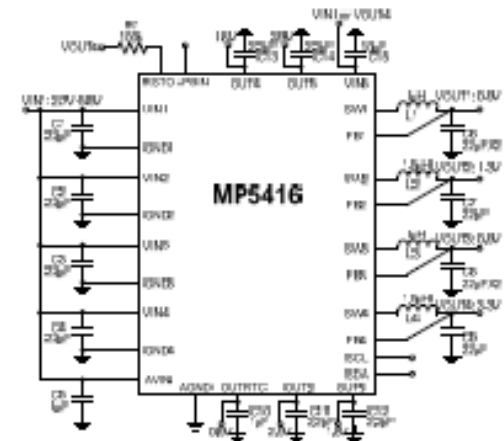
### FEATURES:

- **High Efficiency Step-Down Converters**
  - 4.5A / 2.5A / 4A / 2A Bucks
  - 2.7V to 5.5V Operating Input Range
  - Adjustable Switching Frequency
  - Programmable Forced PWM/Auto PFM/PWM Mode
  - Hiccup Over Current Protection
- **Low Dropout Regulators**
  - One RTC Dedicate LDO
  - Four Low Noise LDOs
  - Two Separate Input Power Supplies
  - 100mV Dropout at 300mA Load
- **System**
  - I2C Bus and OTP
  - Power On/off Button
  - Power On Reset Output
  - Flexible Power On/off Sequence via OTP
  - Flexible DC/DC, LDO On/off via OTP

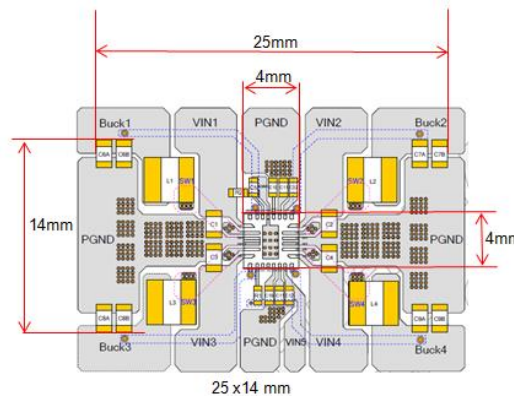
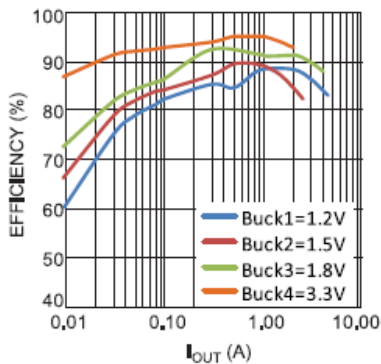
**Package: QFN28 - 4mmx4mm**



### Application Circuit



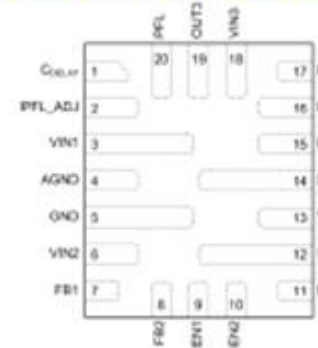
**Efficiency vs. Load Current**  
 $V_{IN}=5V$ , Auto PFM/PWM Mode



## FEATURES

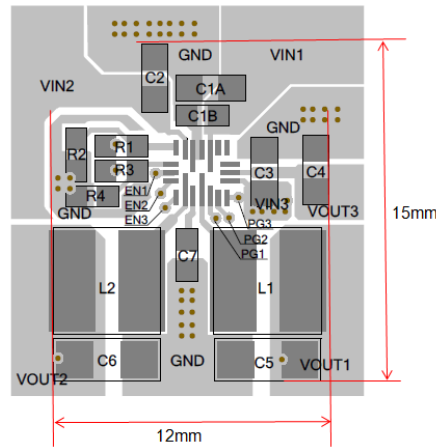
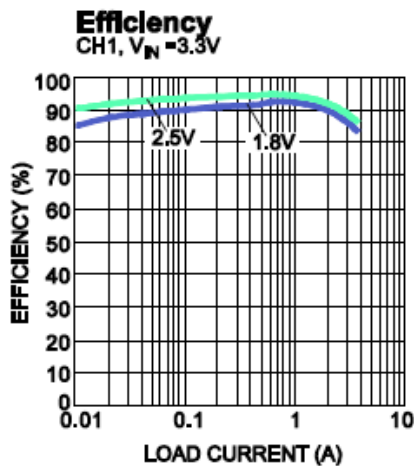
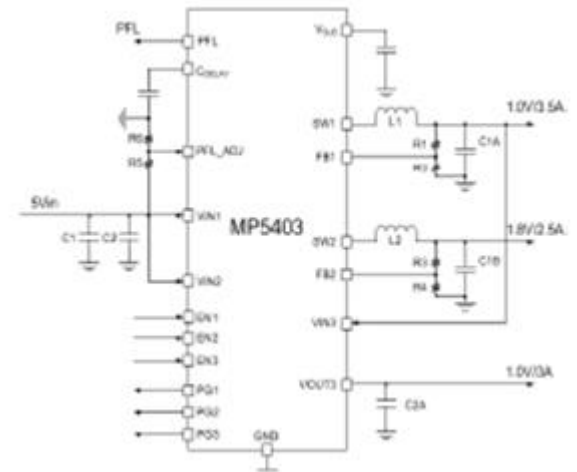
- Low  $I_q$ : 85 $\mu$ A for Two Switchers Total
- Two Buck Converters
  - 3.5A with 55m $\Omega$ /20m $\Omega$   $R_{DS(ON)}$
  - 2.5A with 60m $\Omega$ /22m $\Omega$   $R_{DS(ON)}$
  - 1.5MHz Switching Frequency
  - 180° Interleaving Operation
  - 100% Duty Cycle
- One Load Switch
  - 3A with 20m $\Omega$   $R_{DS(ON)}$
  - Soft Start and Output Discharge
  - Over-Current Protection (OCP)
- EN and Power Good for Power Sequencing
- Input Power Failure Indicator (PFL) with Adjustable Threshold and Delay
- Thermal Shutdown

**Package: QFN20-2.5mmx3mm**



## Application Circuit

Two Bucks and One Load Switch



- High Efficiency
- Cost effective
- Smallest Solution Size
- Minimum External Components
- Fast Transient Response and minimum ripple

Thank you

For additional information please contact  
MPS Reference Design Team  
at [referencedesign@monolithicpower.com](mailto:referencedesign@monolithicpower.com)

For general information  
<http://www.monolithicpower.com>