MPS智能电表解决方案与设计要点

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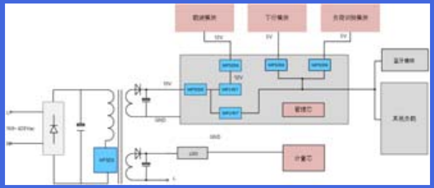
概览

- 智能电表电源设计新挑战
- **MPS** 多类型智能电表解决方案
- 详解**ACDC**开关电源设计
- 智能电表**EMC**设计与优化

智能电表电源的新挑战

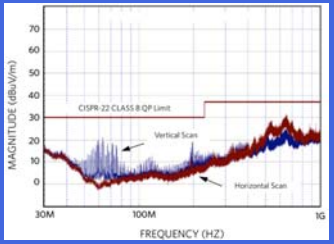
更大的功率
更小的体积

更复杂的电源系统



超高可靠性要求

严格的EMI标准



智能电表电源的新挑战

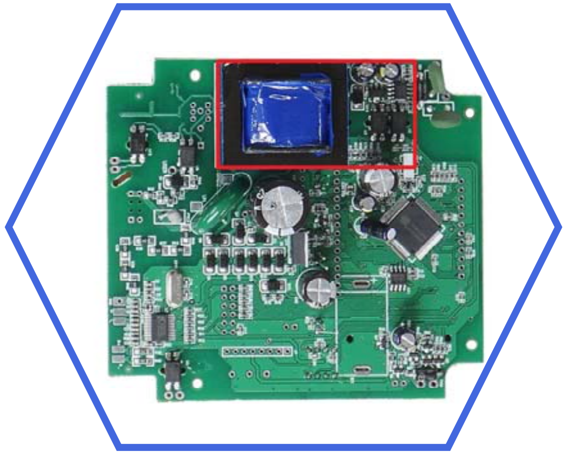
线性变压器方案

更大的功率

更小的体积

更高的电源质量

开关电源方案



如何设计一款稳定、优秀的开关电源？

智能电表电源的新挑战

传统电表

DCDC

更复杂的系统组成

未来智能电表

ACDC

容隔离

DCDC

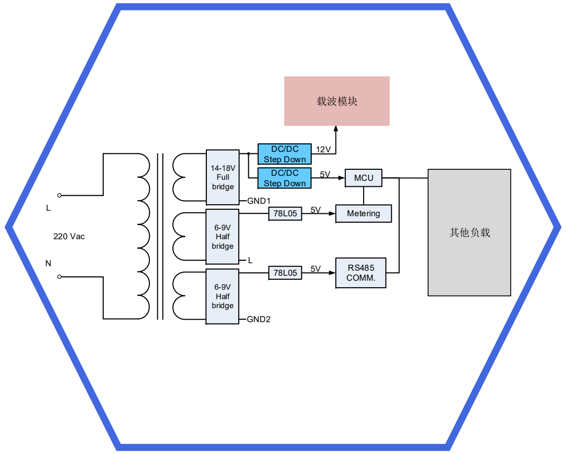
模拟
开关

负载
开关

MPS提供完整可靠的方案

智能电表电源的新挑战

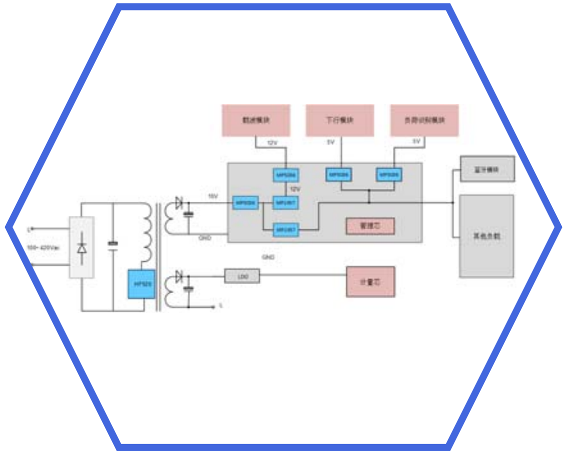
传统电表



更复杂的系统组成

更多的电源管理器件

未来智能电表

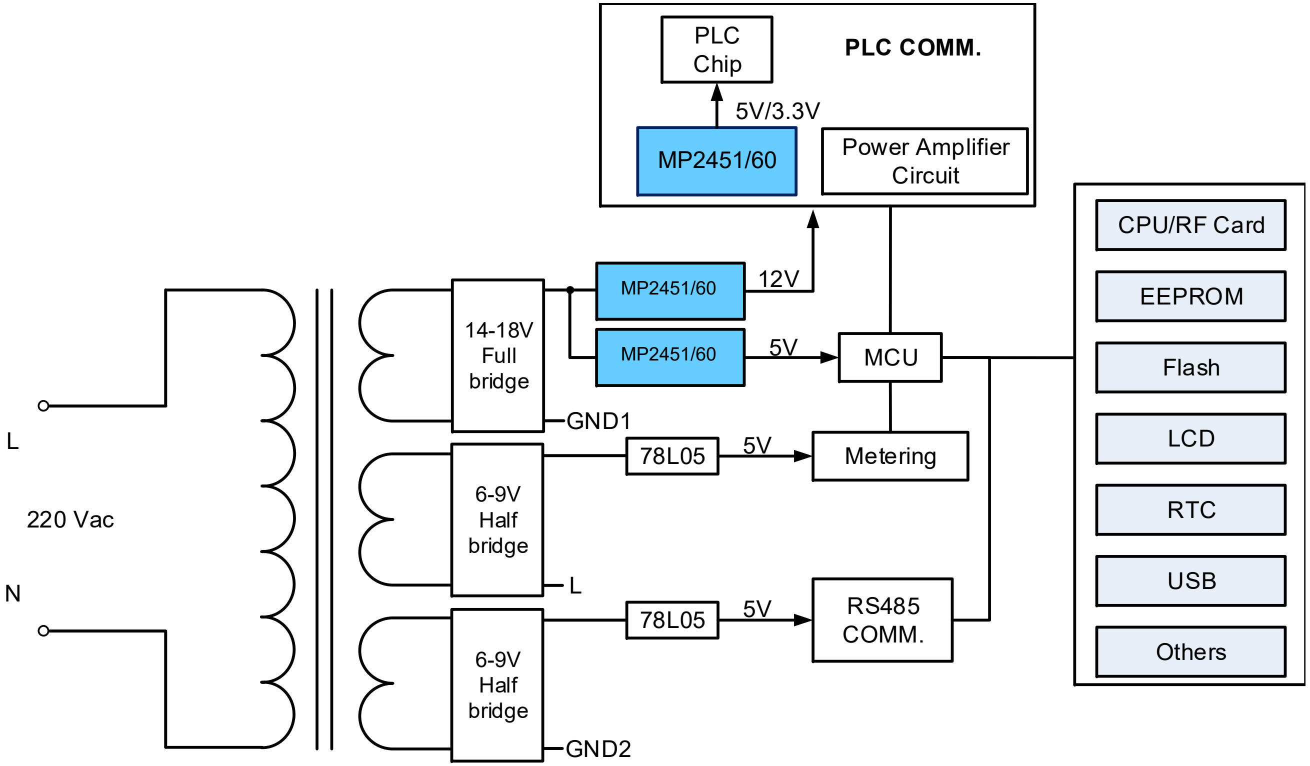


如何优化系统的**EMC**表现？

MPS智能电表解决方案

为客户提供可靠的系统方案

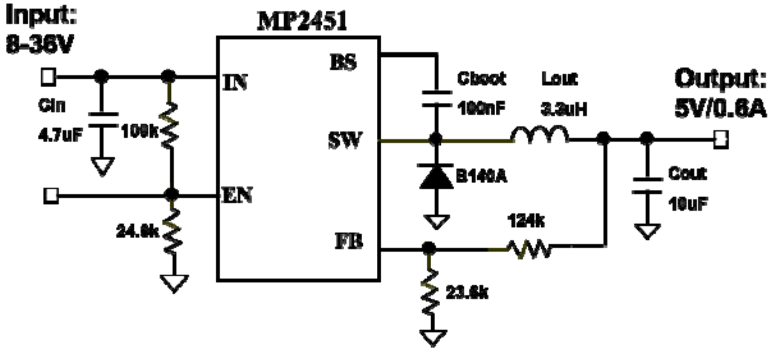
线性变压器单相表



推荐产品: **MP2451; MP2460**

MP2451

- 3.3V to 36V 宽电压输入
- 0.6A 输出电流能力
- 500mΩ 内置MOS
- 峰值效率达到90%
- 开关频率 2MHz， 帮助实现千分之一纹波
- 内置软启动控制
- 逐周期限流保护
- 输出电压可低至0.8V
- 在电表领域出货量大，应用成熟

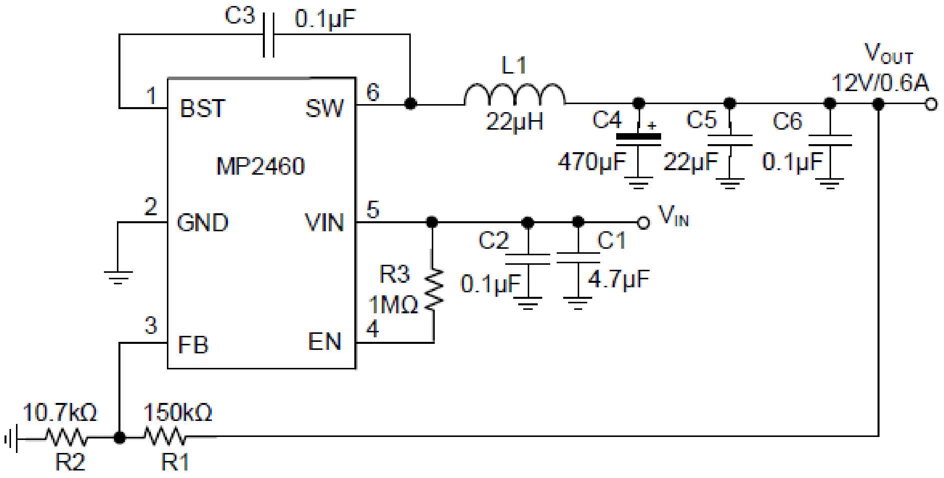


SOT23-6 封装

MP2460

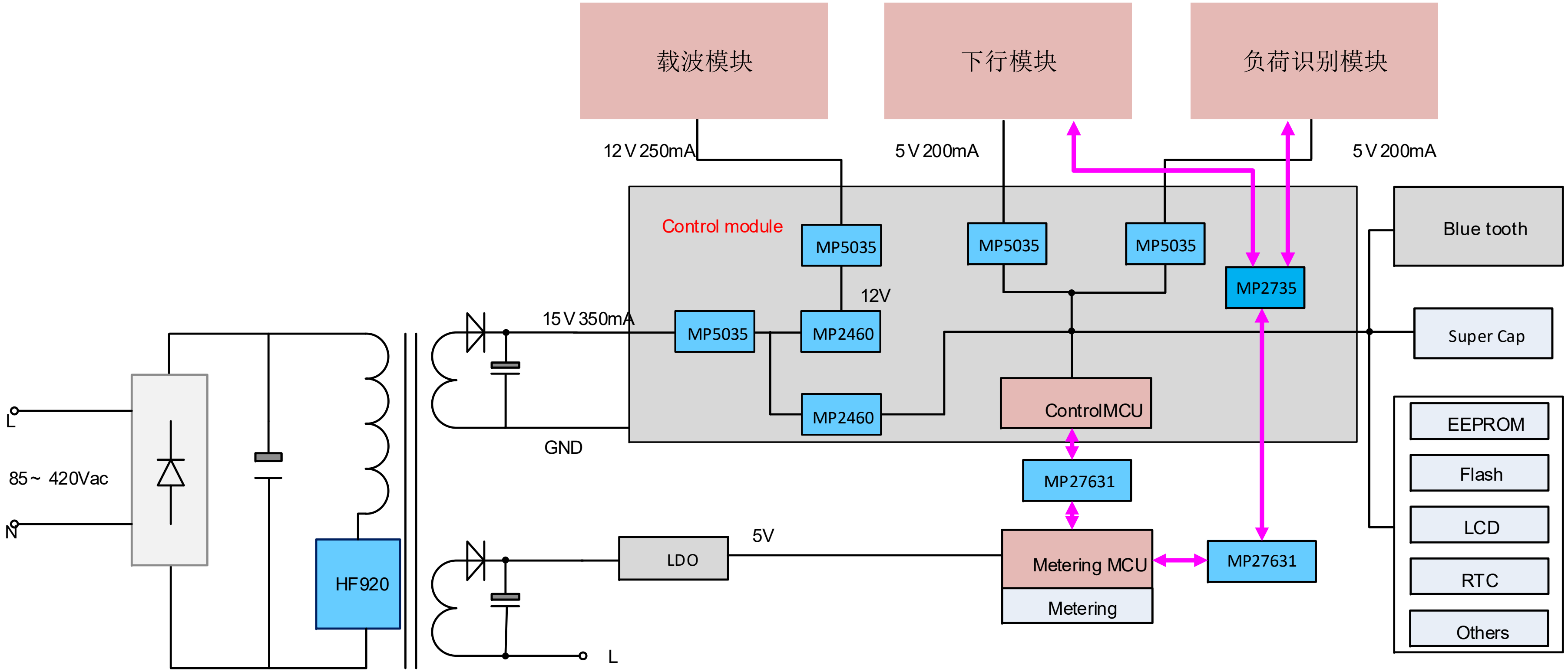
MP2451 迭代产品

- 满足输出千分之一纹波要求
- 同步整流省去外置肖特基
- 支持2%-98% 大占空比应用
- 专为电表设计的低压差模式
- 4.5V — 45V 宽范围输入电压
- 50V 最大耐压
- 自带轻载高效控制
- 峰值效率>90%
- 1.6MHz 定频开关频率
- 与MP2451 管脚兼容



SOT23-6 封装

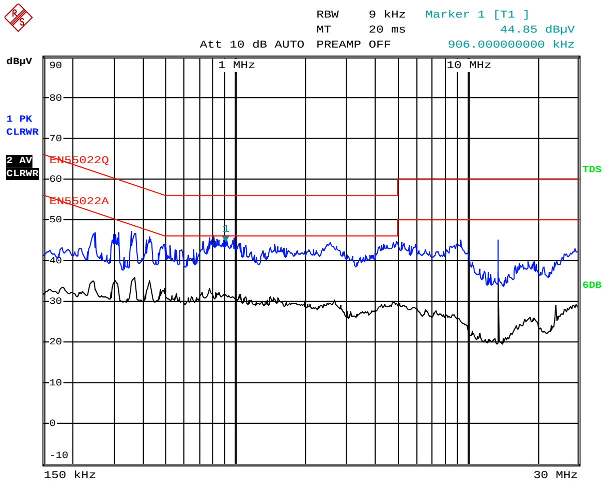
IR46单相智能表



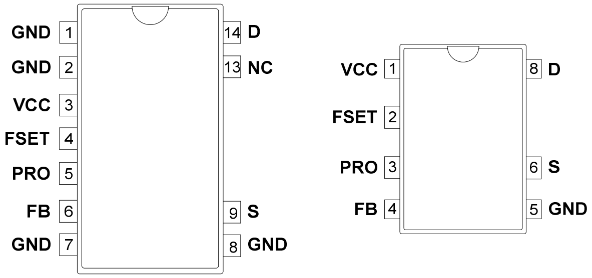
推荐产品: **HF920; MP2460; MP5035; MP27631; MP2735/6**

HF920

- 定频可编程工作频率, 最高支持150kHz
- 自带抖频控制，优化EMI表现
- 支持无共模电感应用，可实现较高的EMI余量
- 丰富的保护机制: OVP, OTP, OLP, UVLO, SCP
- 带输入过压保护，有助于提高抗浪涌特性
- 专为电表设计的抗强磁模式，有效提高抗强磁特性
- 900V耐压，<30mW 超低空载损耗
- 140ms 过载保护延迟，支持输出带2000uF电容启动
- 支持 SSR PSR 和 HV Buck 应用，量产经验丰富



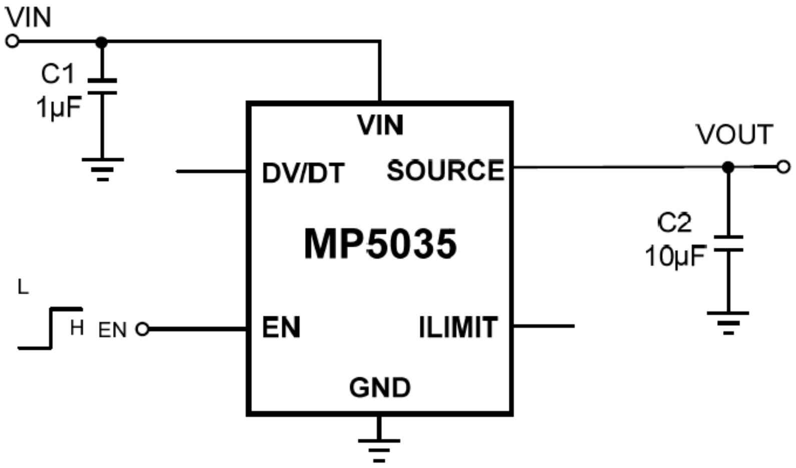
基于HF920 EVB的EMI表现



SOIC14 SOIC8 封装

MP5035

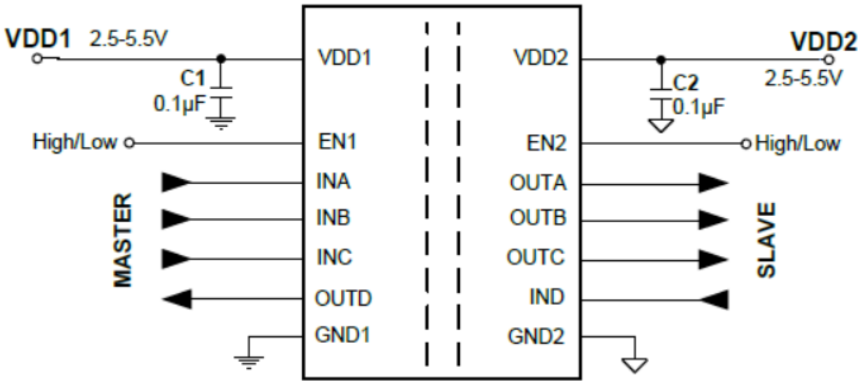
- 2.9V 到 22V 宽输入范围，支持5V、12V应用
- 26V 最大输入耐压
- 50mA-2A 限流点可调
- 内置43mΩ 功率MOS，超低输入输出压降
- 外置DV/DT 软启动引脚，支持输出带大电容启动
- 快速的过流和硬短路保护
- SOT23-6小体积封装



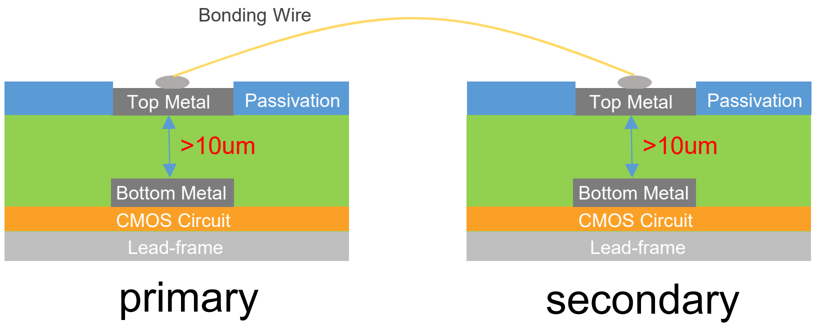
SOT23-6 封装

MP27631

- 支持20Mbps 通讯速率
- 2.7V至5.5V 输入电压范围，支持3.3/5V通讯
- 4通道（1进3出）设计，完美支持SPI接口
- 超低输入工作电流
- 超强的电磁抗干扰能力
- >±40kV/μs 工模抑制能力
- 25ns 低传输延迟
- 5kVRMS 交流绝缘耐压
- 宽体SOICW-16 封装



宽体 WSOC16 封装



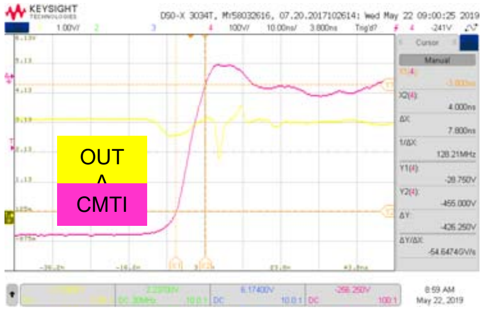
增强设计，理论上支持10KVrms 绝缘强度

MP27631

数字隔离器对比

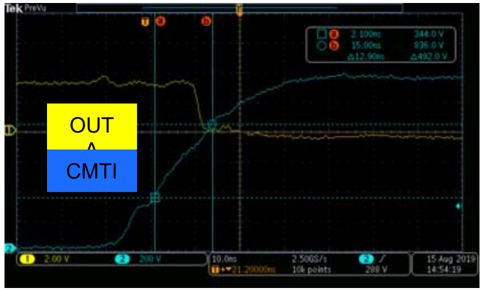
器件	MPS (MP27631)	R 公司产品	C 公司产品
CMTI	**>40KV/us**	38kV/us失效	20kV/us 失效
绝缘能力	**>7kV$_{\mathrm{RMS}}$**	4.8kV$_{\mathrm{RMS}}$失效	5kV$_{\mathrm{RMS}}$失效
ESD	**>8kV**	7kV失效	5kV失效
		未进行绝缘增强设计	未进行绝缘增强设计

MPS



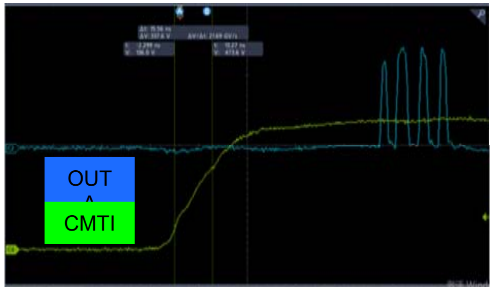
CMTI=40KV/us, OK

R 公司产品



CMTI=38KV/us, fails

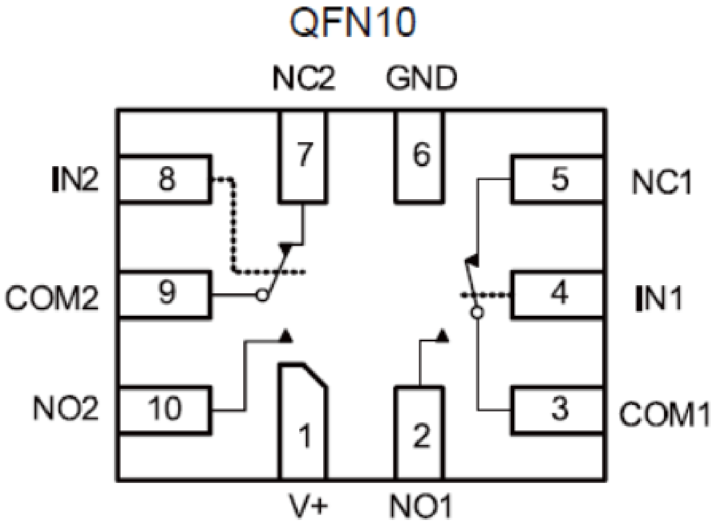
C 公司产品



CMTI=22KV/us, fails

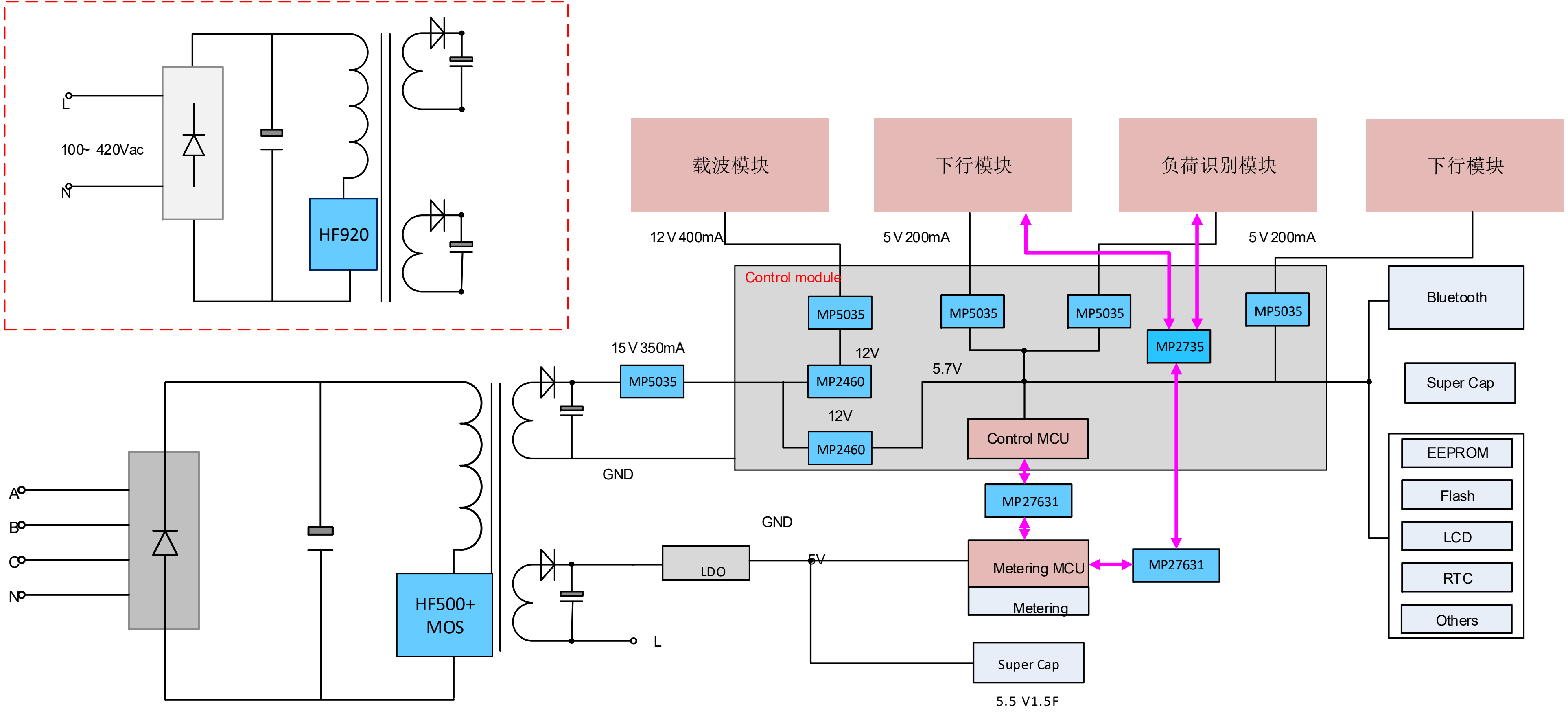
MP2735

- 1.65V 至 5.5V输入范围，支持1.8/3.3/5V应用
- 0.45Ω低导通阻抗，有助于提高信号质量
- 双通道设计，有效减小不同通道之间的串扰
- 1.4mm x 1.8mm QFN10 封装
- ESD 人体模型承受能力 ±4000V



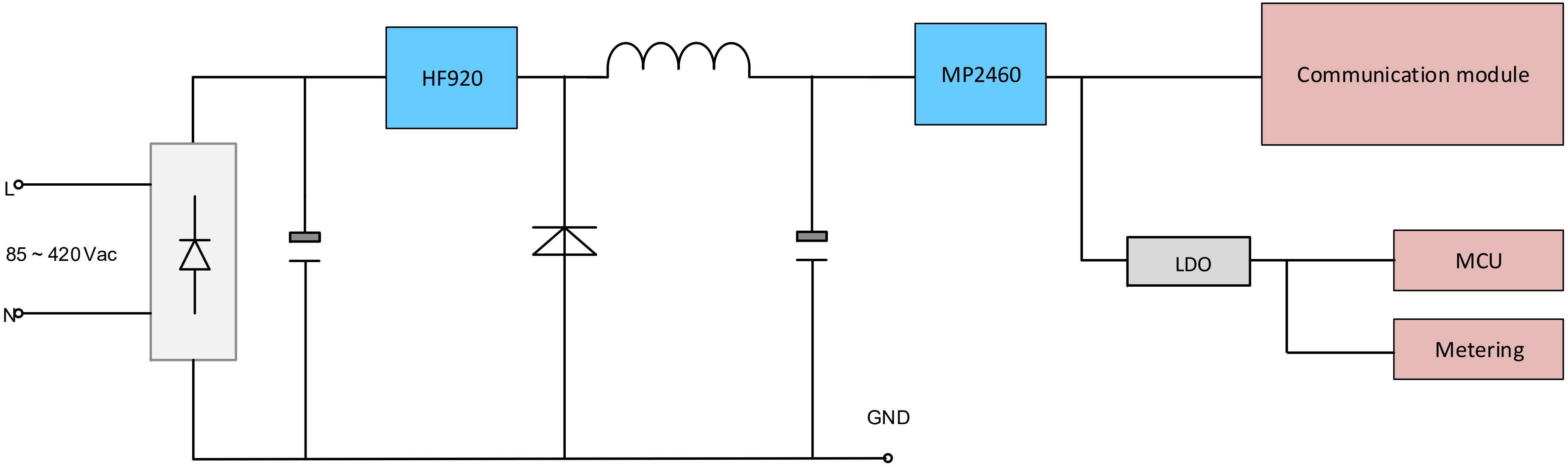
QFN1.4*1.8 封装

IR46三相智能表



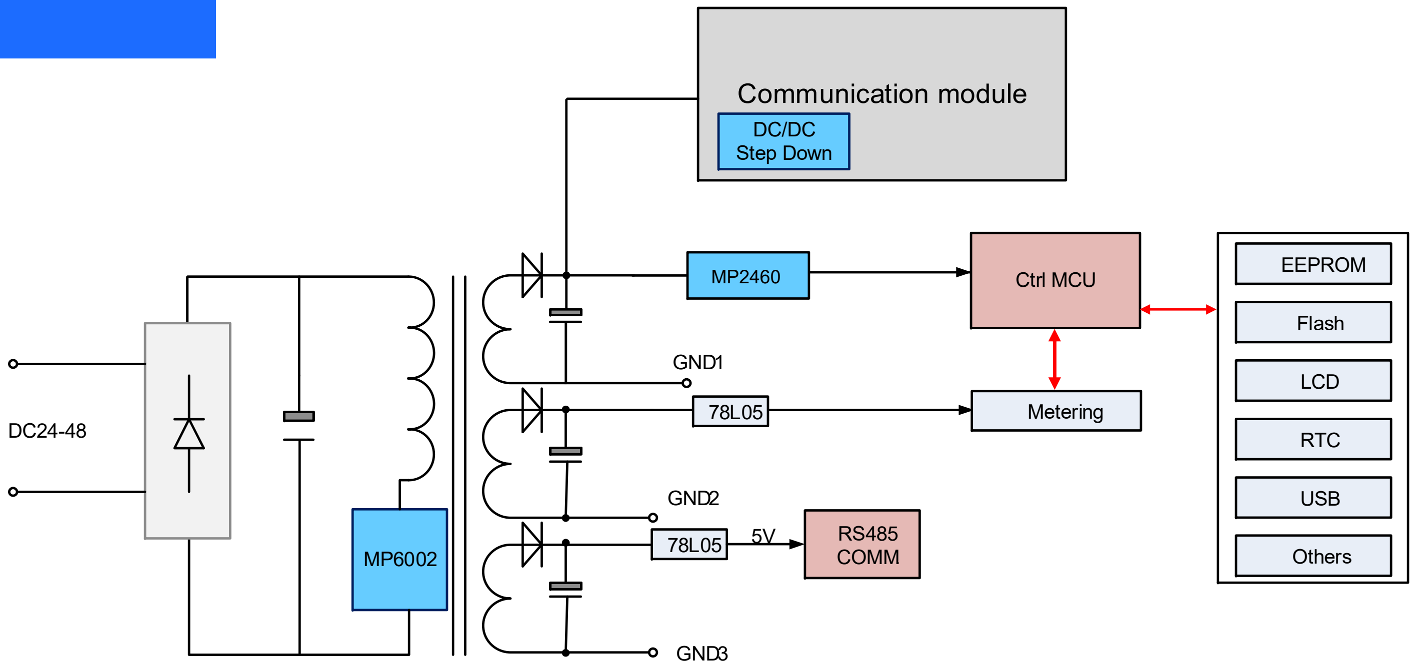
Products: HF500； HF920; MP2460; MP5035; MP27631; MP2735/6

简单单相表应用



HF920 支持SSR, PSR 反激和 BUCK应用

直流表应用



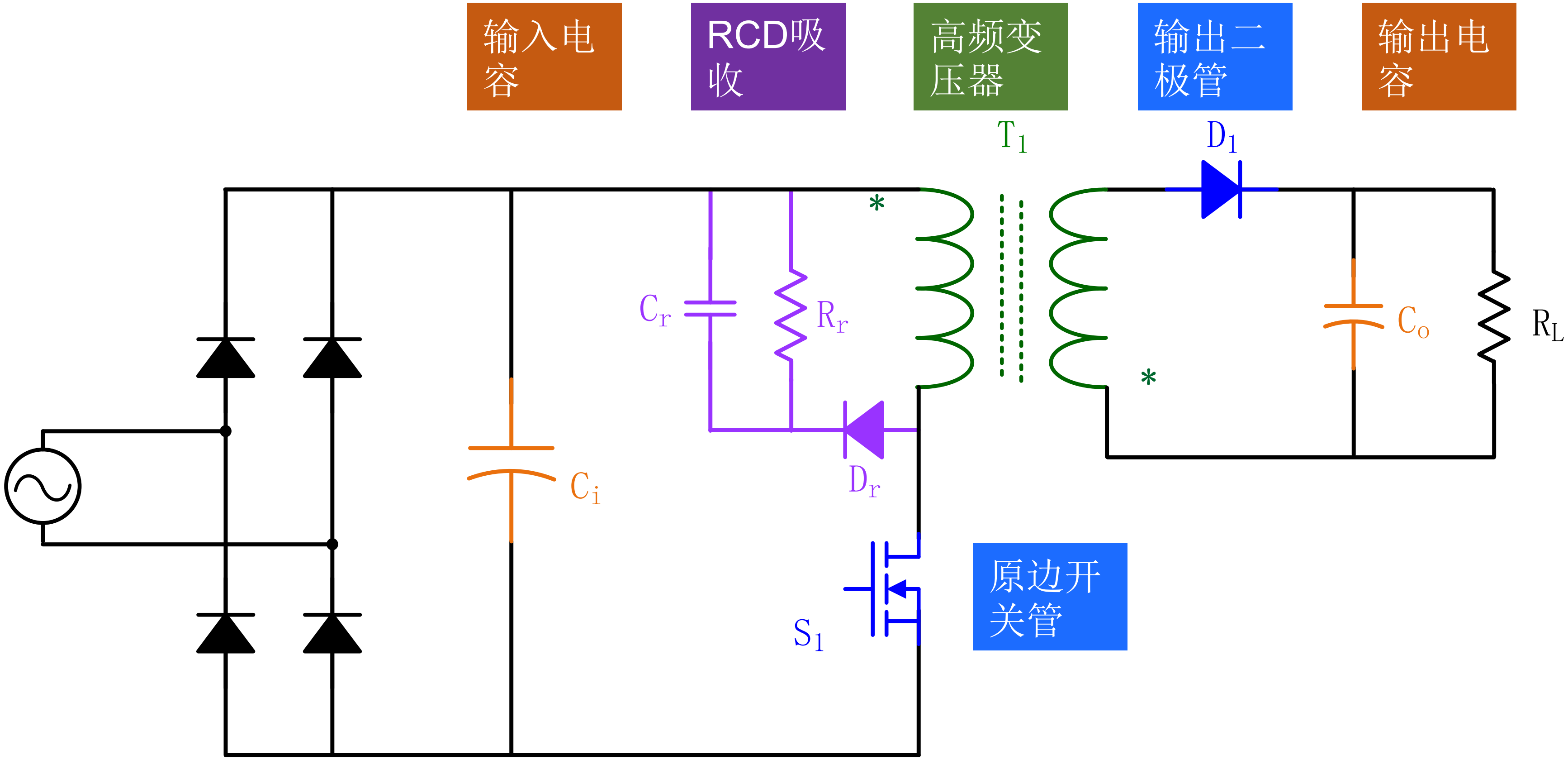
Input: DC10-36V

Input: DC36-72V

Input: DC30-50V

反激电源功率级设计

反激电源功率级设计 --- 反激电源基本结构



输入电容

RCD吸收

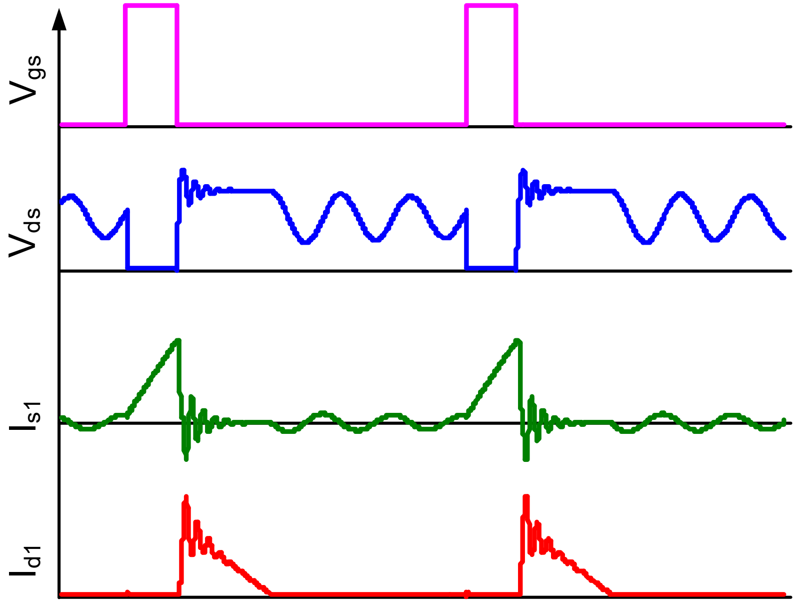
高频变压器

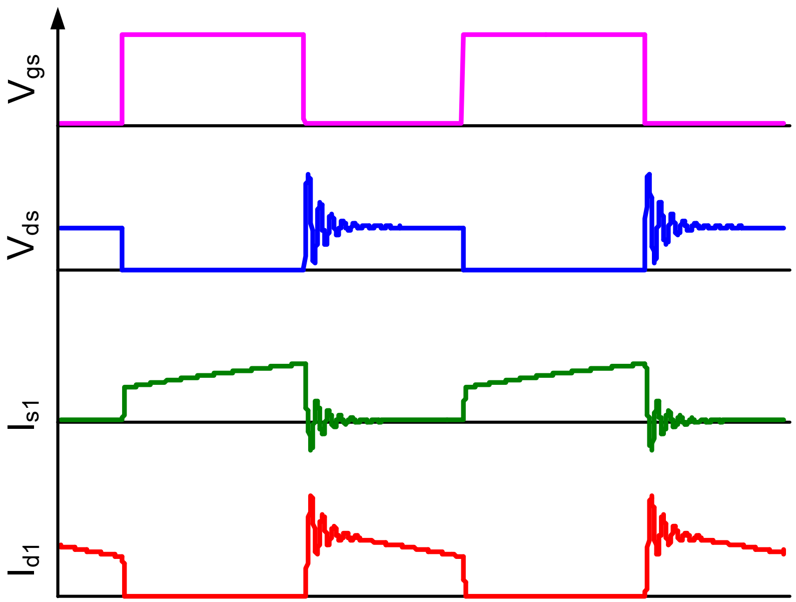
输出二极管

输出电容

原边开关管

反激电源功率级设计 --- 反激电源工作模式





DCM优点:

反激功率级是一阶系统，容易实现稳定

输出二极管可以实现零电压关断

CCM优点:

原边电流峰值较低，电流有效值较低

输出电压纹波较小

低输入电压工作在**CCM**，高输入电压下工作在**DCM**

反激电源功率级设计 --- 确定系统规格

系统规格：

- ➢ 输入交流电压范围：$V_{in\_ac\_min}$~$V_{in\_ac\_max}$
- ➢ 输入交流频率：f_{line}
- ➢ 主路输出电压、电流：V_{o1}，I_{o1}
- ➢ 辅路输出电压、电流：V_{o2}，I_{o2}
- ➢ 电源开关频率：f_w
- ➢ 预估电源工作效率：η
- ➢ 电源输出功率：$P_o=V_{o1}*I_{o1}+V_{o2}*I_{o2}$
- ➢ 电源输入功率：$P_{in}=P_o/\eta$

设计规格：

- ➢ $V_{in\_ac\_min}$~$V_{in\_ac\_max}=85V_{ac}-420V_{ac}$
- ➢ $f_{line}= 50Hz$
- ➢ V_{o1}，I_{o1}= 15V 400mA
- ➢ V_{o2}，I_{o2}= 9V 100mA
- ➢ 电源开关频率：f_w= 60kHz
- ➢ $\eta=80\%$
- ➢ $P_o=6.9W$
- ➢ $P_{in}=P_o/\eta=8.6W$

反激电源功率级设计

--- 反激电源基本结构

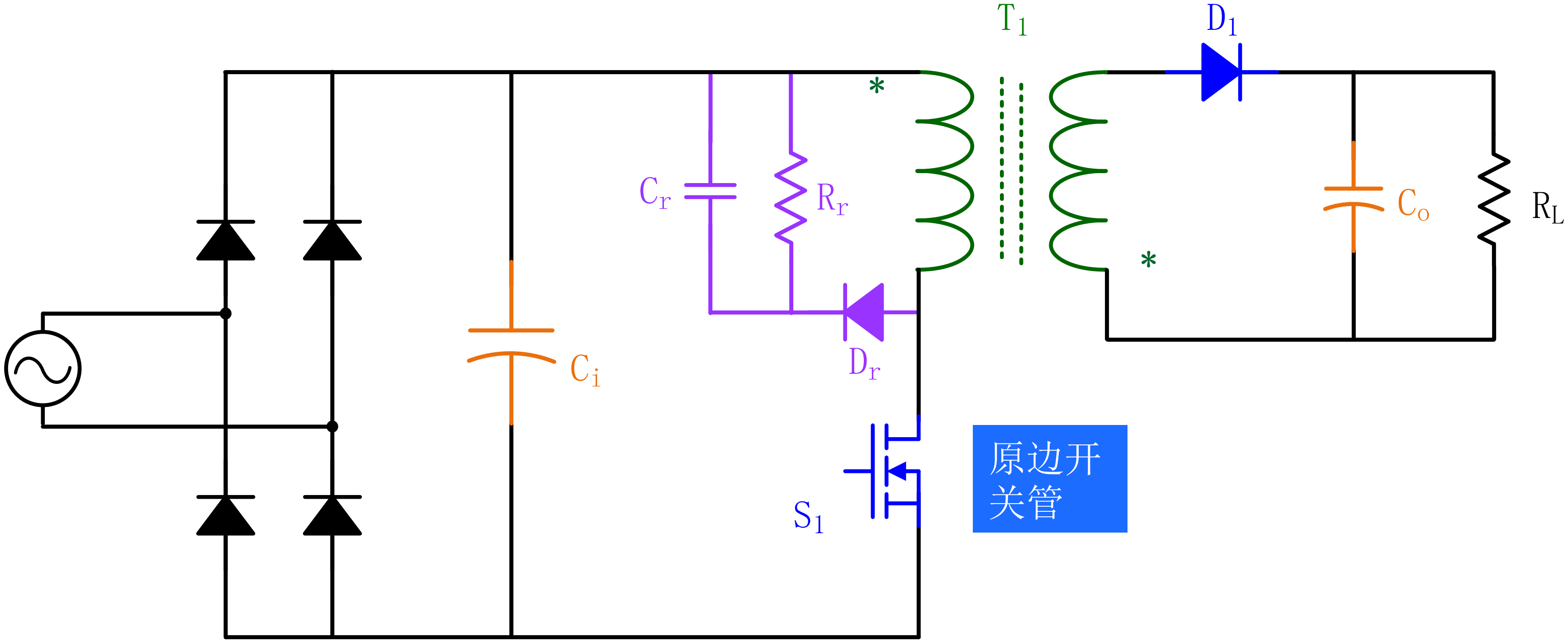
输入电容

RCD吸收

高频变压器

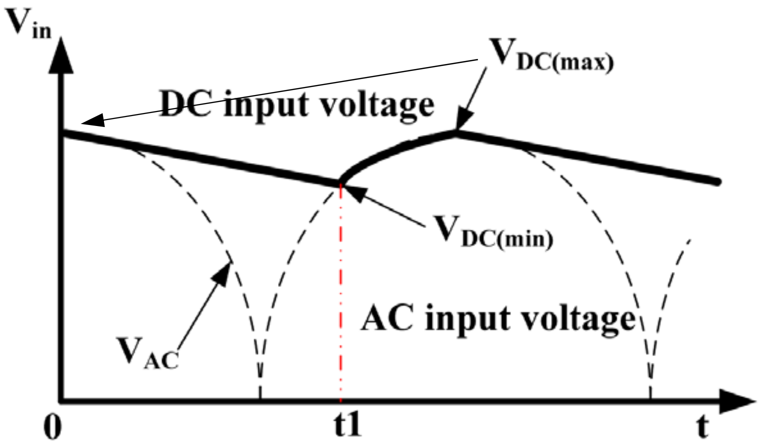
输出二极管

输出电容



原边开关管

反激电源功率级设计 --- 确定母线电容和电压极值



t_1时刻交流电压等于母线电容电压

$$V_{dc\_max} * \cos(2\pi * f_{line} * \boxed{t_1}) = \boxed{V_{dc\_min}}$$

0-t_1时间内，母线电容放出的能量：

$$P_{in} * \boxed{t_1} = \frac{1}{2} C_{in} * (V_{dc\_max}{}^2 - \boxed{V_{dc\_min}{}^2})$$

母线电容值：1-2uF/W

选取母线电容值：22uF

母线最高电压： $V_{dc\_max} = \sqrt{2} * 420 \approx 594\,V$

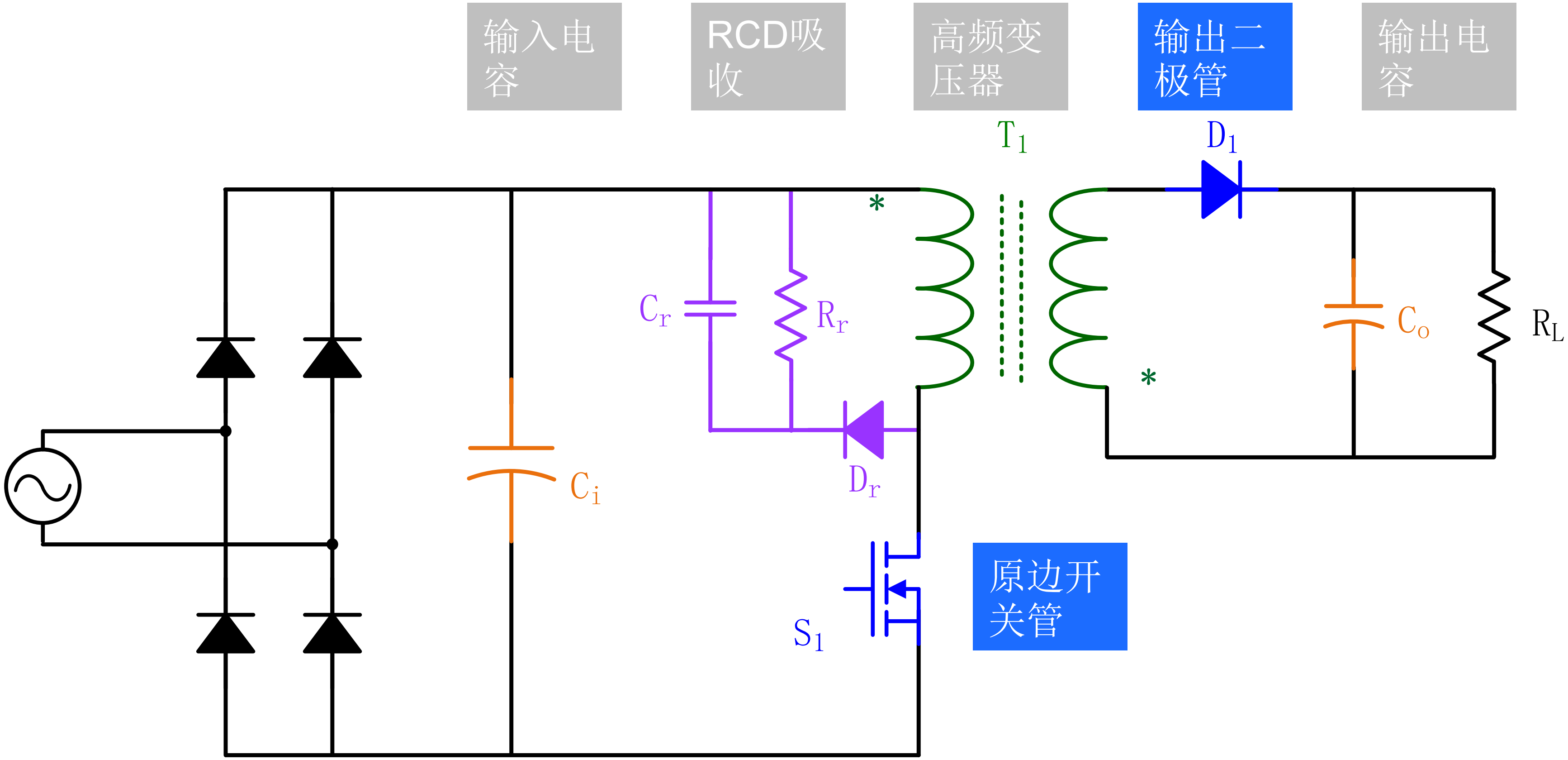
母线最低电压：

$$\begin{cases} \sqrt{2} * 85(V) * \cos(2\pi * 50(Hz) * t_1) = V_{dc\_min} \\ 8.6(W) * t_1 = \frac{1}{2} * 22(uF) * ((\sqrt{2} * 85\,V)^2 - V_{dc\_min}{}^2) \end{cases}$$

↓

$$V_{dc\_min} \approx 91\,V$$

反激电源功率级设计 --- 反激电源基本结构


输入电容

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输出二极管

输出电容

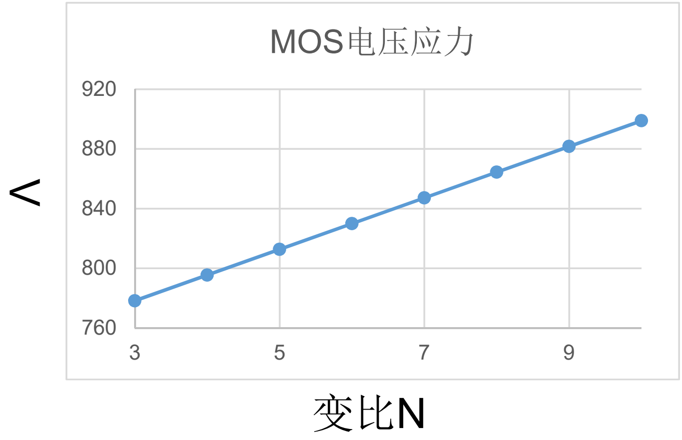
原边开关管

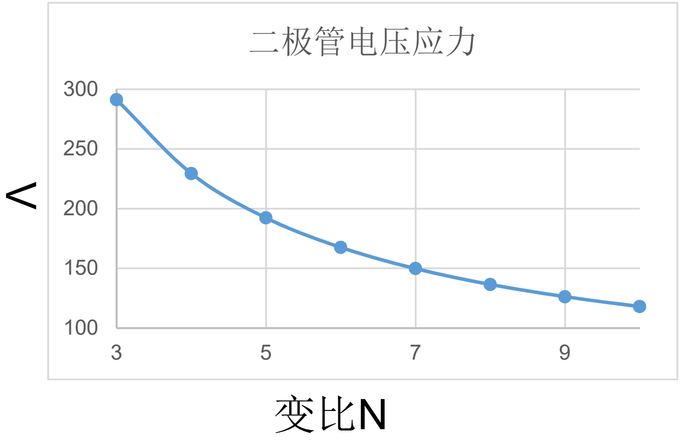
反激电源功率级设计 --- 变压器设计

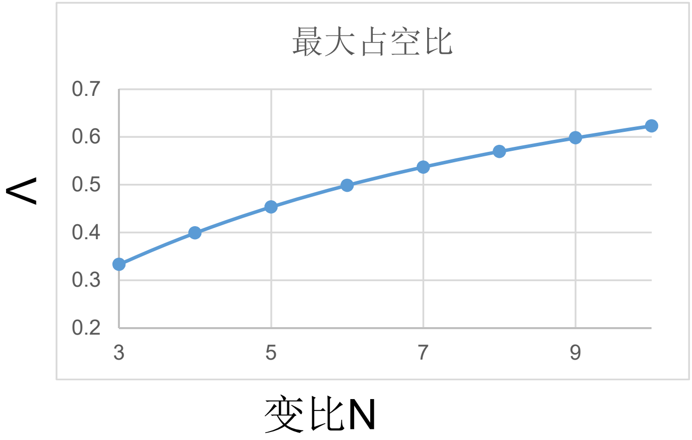
$$V_{MOS}=\frac{V_{dc\_max}+N*(V_{o1}+V_{f})+60\,V}{0.9}$$

$$V_{diode}=\frac{\frac{V_{dc\_max}}{N}+V_{o1}+20\,V}{0.8}$$

$$D_{max}=\frac{N*(V_{o1}+V_{f})}{N*(V_{o1}+V_{f})+V_{dc\_min}}$$



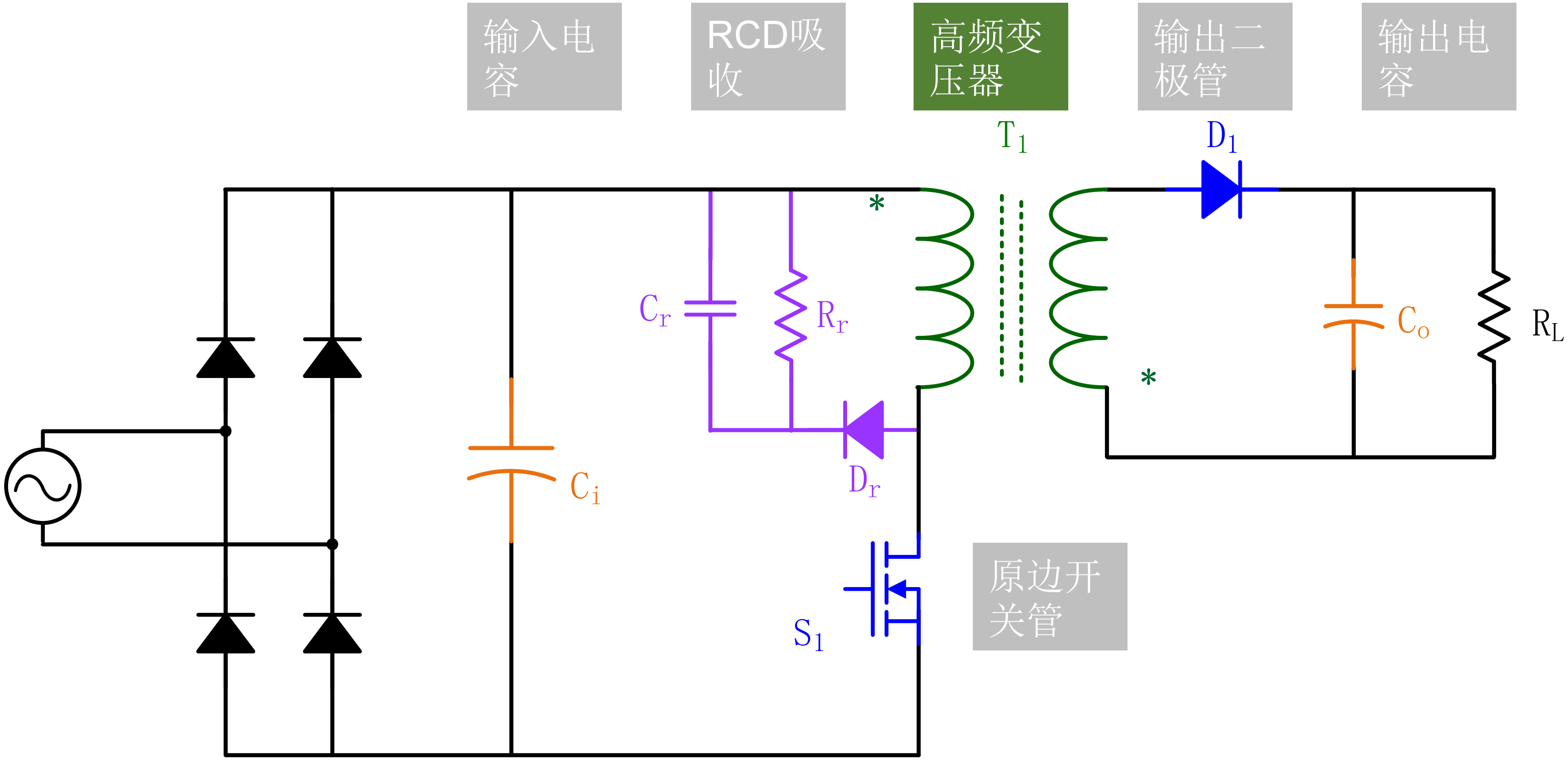




N	→	K	→	I_p	→	L_m	→	A_p	→	Nw
变比		电流纹波系数		原边电流峰值		励磁电感		磁芯		绕组匝数

反激电源功率级设计

--- 反激电源基本结构



输入电容

RCD吸收

高频变压器

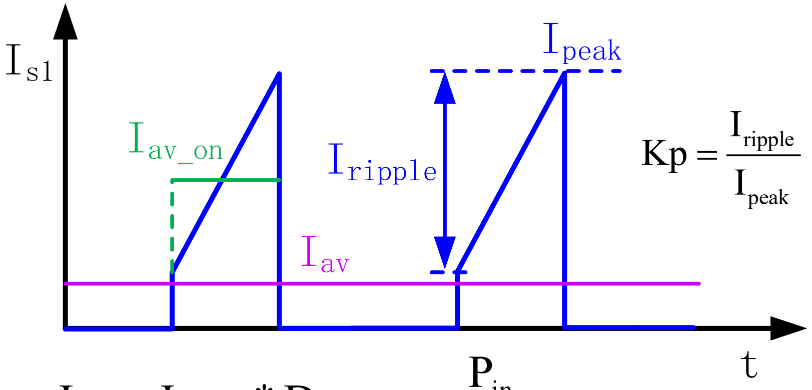
输出二极管

输出电容

原边开关管

反激电源功率级设计 --- 变压器设计

- 母线电压最低时，系统条件最“恶劣”
- 最低母线电压时，系统工作在CCM



$$Kp = \frac{I_{ripple}}{I_{peak}}$$

$$I_{av} = I_{av\_on} * D_{max} = \frac{P_{in}}{V_{dc\_min}}$$

$$I_{peak} = \frac{I_{av\_on}}{1 - 0.5K_p}$$

K_p通常取0.6-0.9

选择变压器变比：N=6

最大占空比：$D_{max} = \frac{N*(V_{o1}+V_f)}{N*(V_{o1}+V_f)+V_{dc\_min}}$ =50.5%

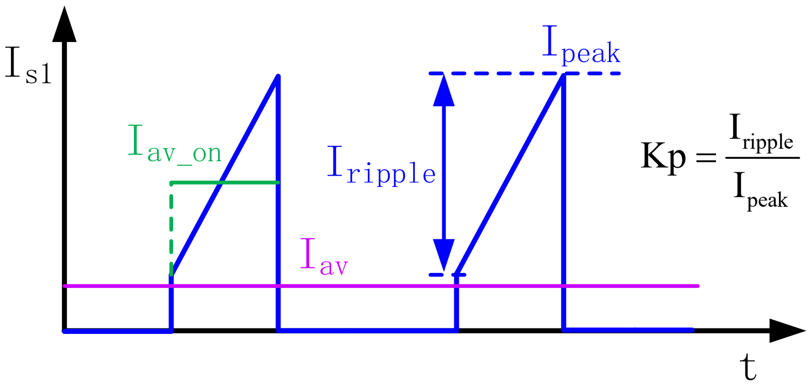
MOS开通平均电流：$I_{av\_on} = \frac{P_{in}}{V_{dc\_min} * D_{max}}$ =187.5mA

K_p取值0.85

MOS电流峰值：$I_{peak} = \frac{I_{av\_on}}{1 - 0.5K_p}$ =326.1mA

N	→	K_p	→	I_p	→	L_m	→	A_p	→	Nw
变比		电流纹波系数		原边电流峰值		励磁电感		磁芯		绕组匝数

反激电源功率级设计 --- 变压器设计



$$Kp = \frac{I_{ripple}}{I_{peak}}$$

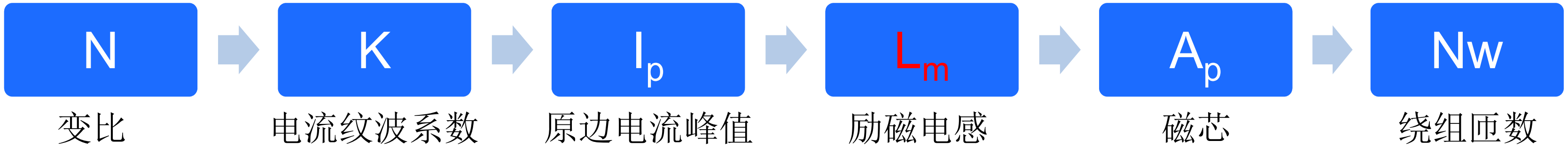
MOS打开，变压器原边绕组电压：

$$L_m \frac{\Delta I}{\Delta T} = V_m$$

$$L_m = \frac{V_{dc\_min}}{I_{ripple}} \frac{D_{max}}{F_w}$$

变压器原边励磁电感量：

$$L_m = \frac{V_{dc\_min}}{I_{ripple}} \frac{D_{max}}{F_w} \quad = 2.8mH$$

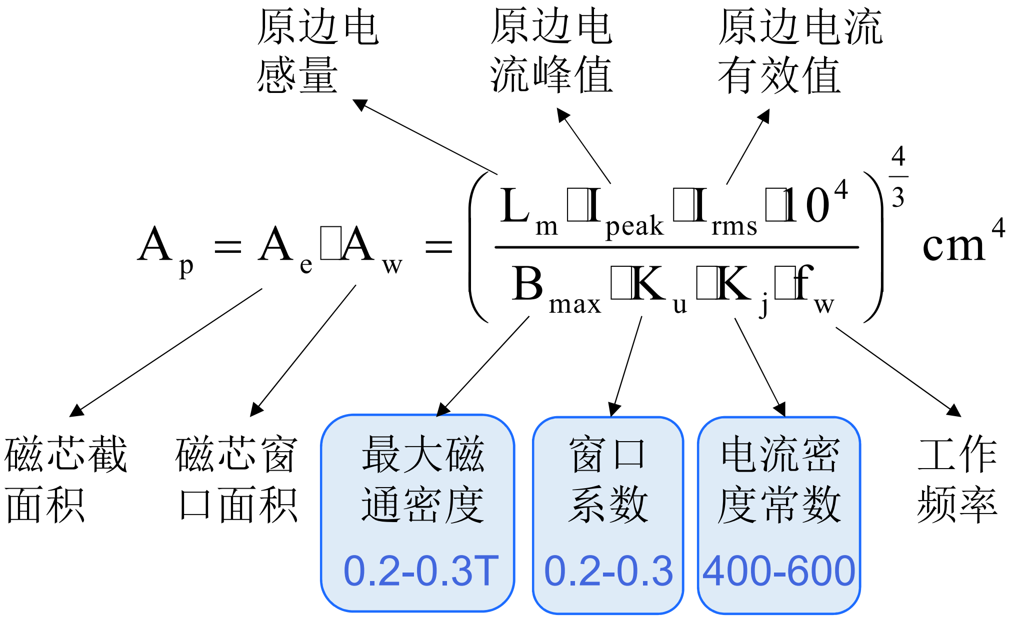


N → K → I_p → L_m → A_p → Nw

变比 电流纹波系数 原边电流峰值 励磁电感 磁芯 绕组匝数

反激电源功率级设计 --- 变压器设计

电压器所需磁芯的窗口面积积：A_p



$$A_p = A_e \cdot A_w = \left(\frac{L_m \cdot I_{peak} \cdot I_{rms} \cdot 10^4}{B_{max} \cdot K_u \cdot K_j \cdot f_w} \right)^{\frac{4}{3}} cm^4$$

原边电感量

原边电流峰值

原边电流有效值

磁芯截面积

磁芯窗口面积

最大磁通密度 0.2-0.3T

窗口系数 0.2-0.3

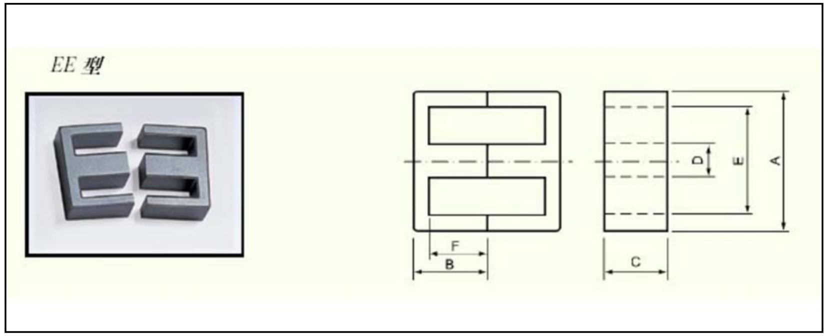
电流密度常数 400-600

工作频率

$$A_p = A_e \cdot A_w = \left(\frac{L_m \cdot I_{peak} \cdot I_{rms} \cdot 10^4}{B_{max} \cdot K_u \cdot K_j \cdot f_w} \right)^{\frac{4}{3}} cm^4$$

$A_p=230mm^4$

磁芯	骨架	Dimensions (mm)	Ap	Ae	Aw
		A * B * C	(mm⁴)	(mm²)	(mm²)
EE16	BE16-118	16*7.2*4.8	512.6	19.20	26.7



N → K → I_p → L_m → A_p → Nw

反激电源功率级设计 --- 变压器设计

由磁链：

$$\Phi = L_m \square I_{peak} = N_p \square B_{max} \square A_e$$

确定变压器原边匝数：

$$N_p = \frac{L_m \square I_{peak}}{B_{max} \square A_e}$$

确定变压器副边匝数：

$$N_s = \frac{N_p}{N}$$

确定变压器原边匝数：

$$N_p = \frac{L_m \square I_{peak}}{B_{max} \square A_e} \quad =180$$

15V主输出匝数：

$$N_{s1} = \frac{N_p}{N} \quad =30$$

9V辅输出匝数：

$$N_{s2} = \frac{N_{s1} V_{o2}}{V_{o1}} \quad =18$$

N → K → I_p → L_m → A_p → N_w

反激电源功率级设计 --- 变压器设计

电流趋肤深度：

$$\Delta d=\sqrt{\frac{1}{\pi \cdot f_w \cdot \mu \cdot \sigma}}$$

$$\mu = 4\pi * 10^{-7} H/m$$

$$\sigma = 6 * 10^{7} S/m$$

导线载流密度：

自然散热： $J = 4-7\ A/mm^2$

风冷散热： $J = 8-10\ A/mm^2$

电流趋肤深度：

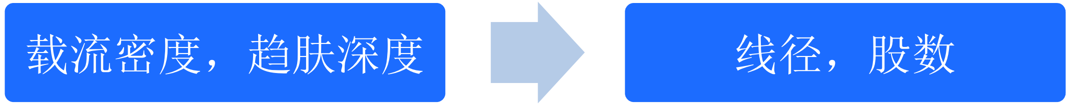
$$\Delta d=\sqrt{\frac{1}{\pi \cdot f_w \cdot \mu \cdot \sigma}} = 0.26mm$$

实际选择导线截面积:

$$S_p = \frac{I_{p\_rms}}{J} = 0.024mm^2$$

变压器原边选择线径0.18mm

同理，变压器副边线径分别为：0.25mm*2; 0.2mm



载流密度，趋肤深度

线径，股数

反激电源功率级设计 --- 输出电容

由最小输出纹波倒推输出电容大小

$$C_o \cdot \Delta V_1 = T_{on} \cdot I_o$$

$$\Delta V_2 = ESR \cdot (I_{peak} - I_o)$$

$$\Delta V = \Delta V_1 + \Delta V_2$$

↓

$$C_o = \frac{T_{on} \cdot I_o}{\Delta V - ESR \cdot (I_{peak} - I_o)}$$

假设给定目标输出纹波小于100mV

主路输出电容ESR 50mΩ，辅路ESR 10mΩ

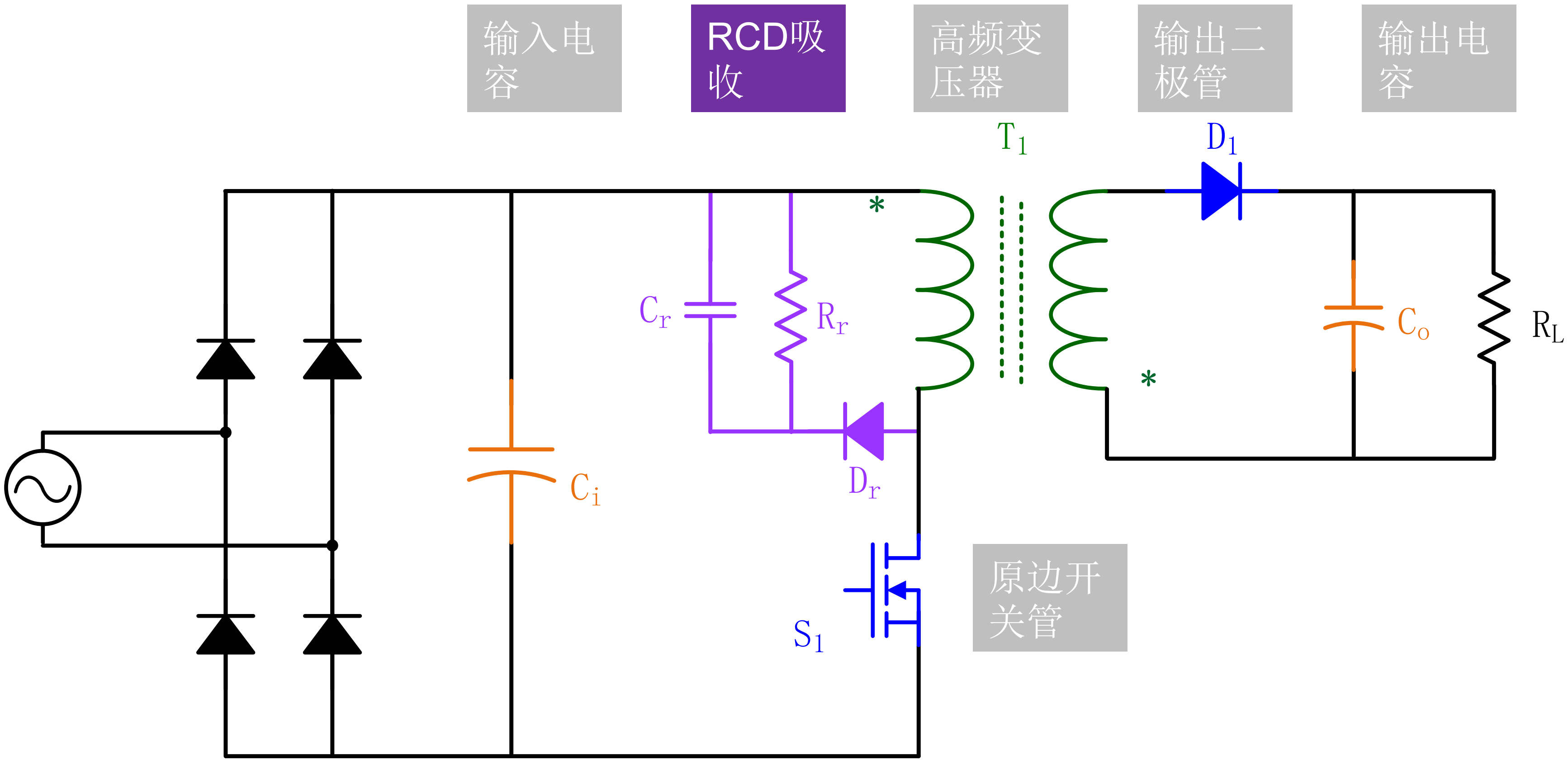
主路输出电容：

$$C_o = \frac{T_{on} \cdot I_o}{\Delta V - ESR \cdot (I_{peak} - I_o)}$$ =152uF

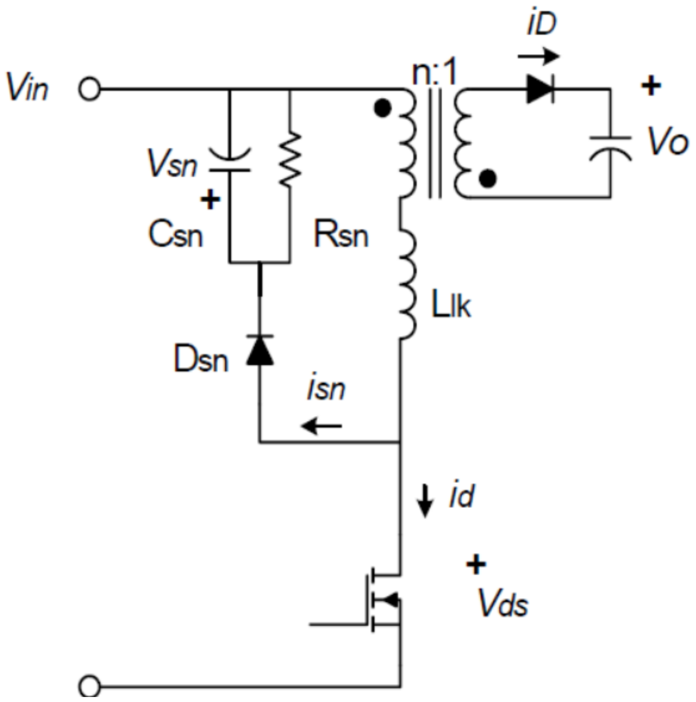
辅路输出电容：

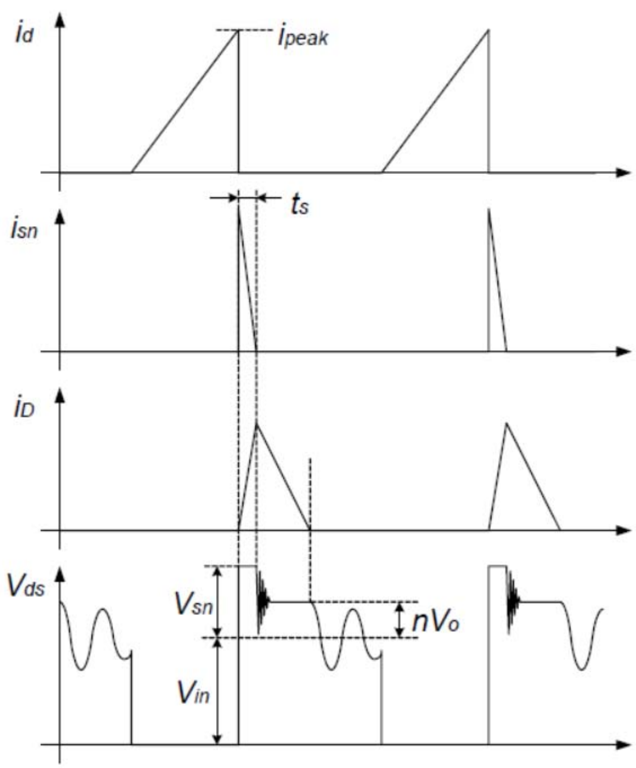
$$C_o = \frac{T_{on} \cdot I_o}{\Delta V - ESR \cdot (I_{peak} - I_o)}$$ =50uF

反激电源功率级设计 --- 反激电源基本结构



反激电源功率级设计 --- RCD





$$\frac{dI_{sn}}{dt} = -\frac{V_{sn} - nV_o}{L_{lk}}$$

$$t_s = \frac{L_{lk}}{V_{sn} - nV_o} \cdot I_{peak}$$

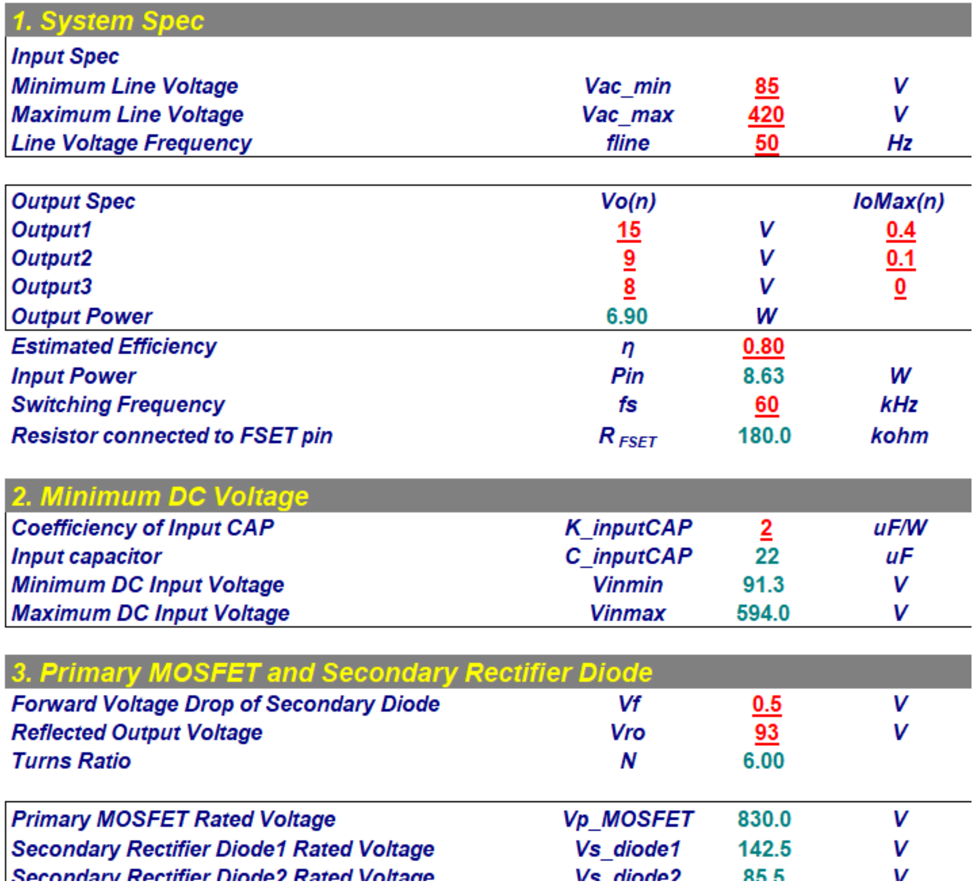
$$P_{sn} = V_{sn} \frac{I_{peak} \cdot t_s}{2} fw$$

$$P_{sn} = \frac{1}{2} L_{lk} I_{peak}^{2} \frac{V_{sn}}{V_{sn} - nV_o} fw$$

$$R_{sn} = \frac{V_{sn}^{2}}{P_{sn}}$$

$$\Delta V_{sn} = \frac{V_{sn}}{C_{sn} R_{sn} f_w}$$

反激电源功率级设计 --- 计算工具



1. System Spec

Input Spec			
Minimum Line Voltage	Vac_min	85	V
Maximum Line Voltage	Vac_max	420	V
Line Voltage Frequency	fline	50	Hz

Output Spec	Vo(n)		IoMax(n)
Output1	15	V	0.4
Output2	9	V	0.1
Output3	8	V	0
Output Power	6.90	W	
Estimated Efficiency	η	0.80	
Input Power	Pin	8.63	W
Switching Frequency	fs	60	kHz
Resistor connected to FSET pin	R_{FSET}	180.0	kohm

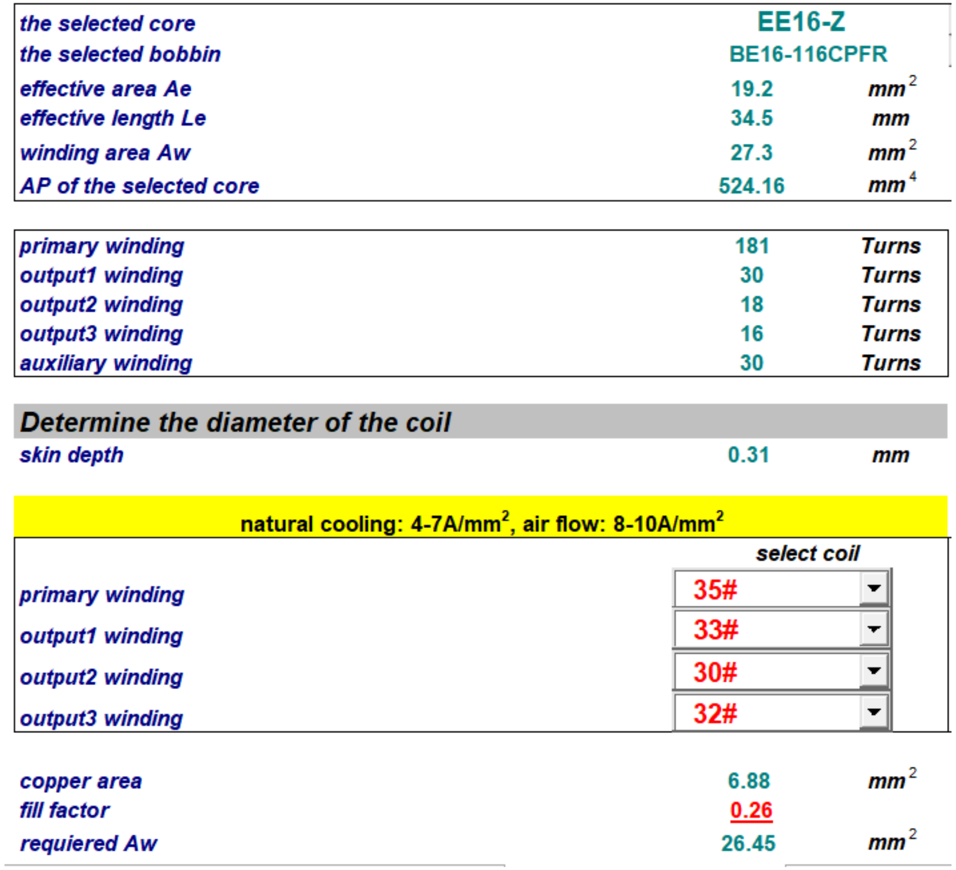
2. Minimum DC Voltage

Coefficiency of Input CAP	K_inputCAP	2	uF/W
Input capacitor	C_inputCAP	22	uF
Minimum DC Input Voltage	Vinmin	91.3	V
Maximum DC Input Voltage	Vinmax	594.0	V

3. Primary MOSFET and Secondary Rectifier Diode

Forward Voltage Drop of Secondary Diode	Vf	0.5	V
Reflected Output Voltage	Vro	93	V
Turns Ratio	N	6.00	

Primary MOSFET Rated Voltage	Vp_MOSFET	830.0	V
Secondary Rectifier Diode1 Rated Voltage	Vs_diode1	142.5	V
Secondary Rectifier Diode2 Rated Voltage	Vs_diode2	85.5	V



the selected core	EE16-Z	
the selected bobbin	BE16-116CPFR	
effective area Ae	19.2	mm^2
effective length Le	34.5	mm
winding area Aw	27.3	mm^2
AP of the selected core	524.16	mm^4

primary winding	181	Turns
output1 winding	30	Turns
output2 winding	18	Turns
output3 winding	16	Turns
auxiliary winding	30	Turns

Determine the diameter of the coil

skin depth	0.31	mm

natural cooling: 4-7A/mm^2, air flow: 8-10A/mm^2

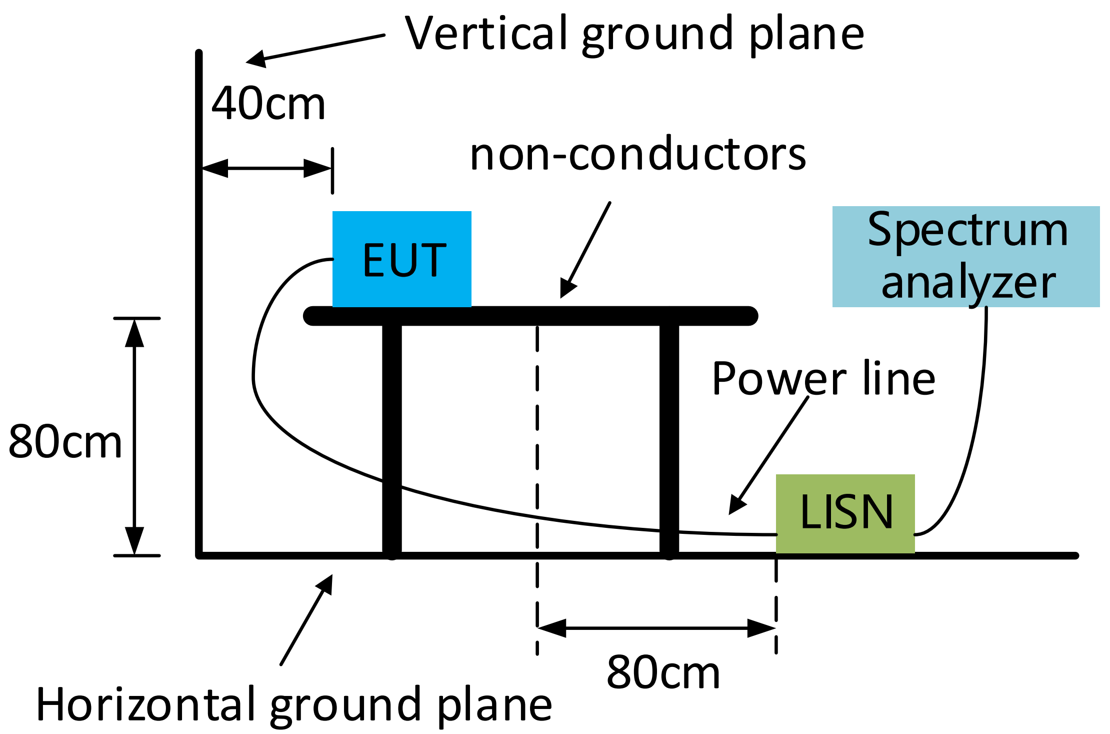
	select coil
primary winding	35#
output1 winding	33#
output2 winding	30#
output3 winding	32#

copper area	6.88	mm^2
fill factor	0.26	
requiered Aw	26.45	mm^2

智能电表EMI优化

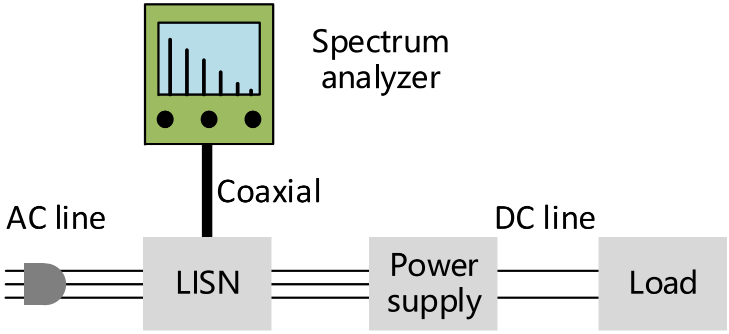
反激电源的传导问题和DCDC的辐射问题

EMI传导测试台



LISN(Line Impendence Stabilization Network) 提供稳定的输入阻抗

频谱分析仪

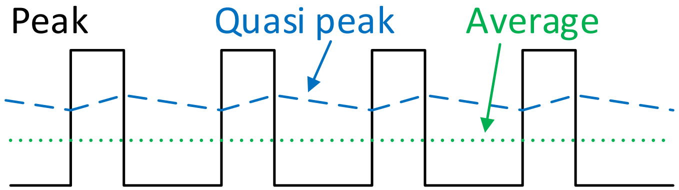


横坐标对应噪声频率

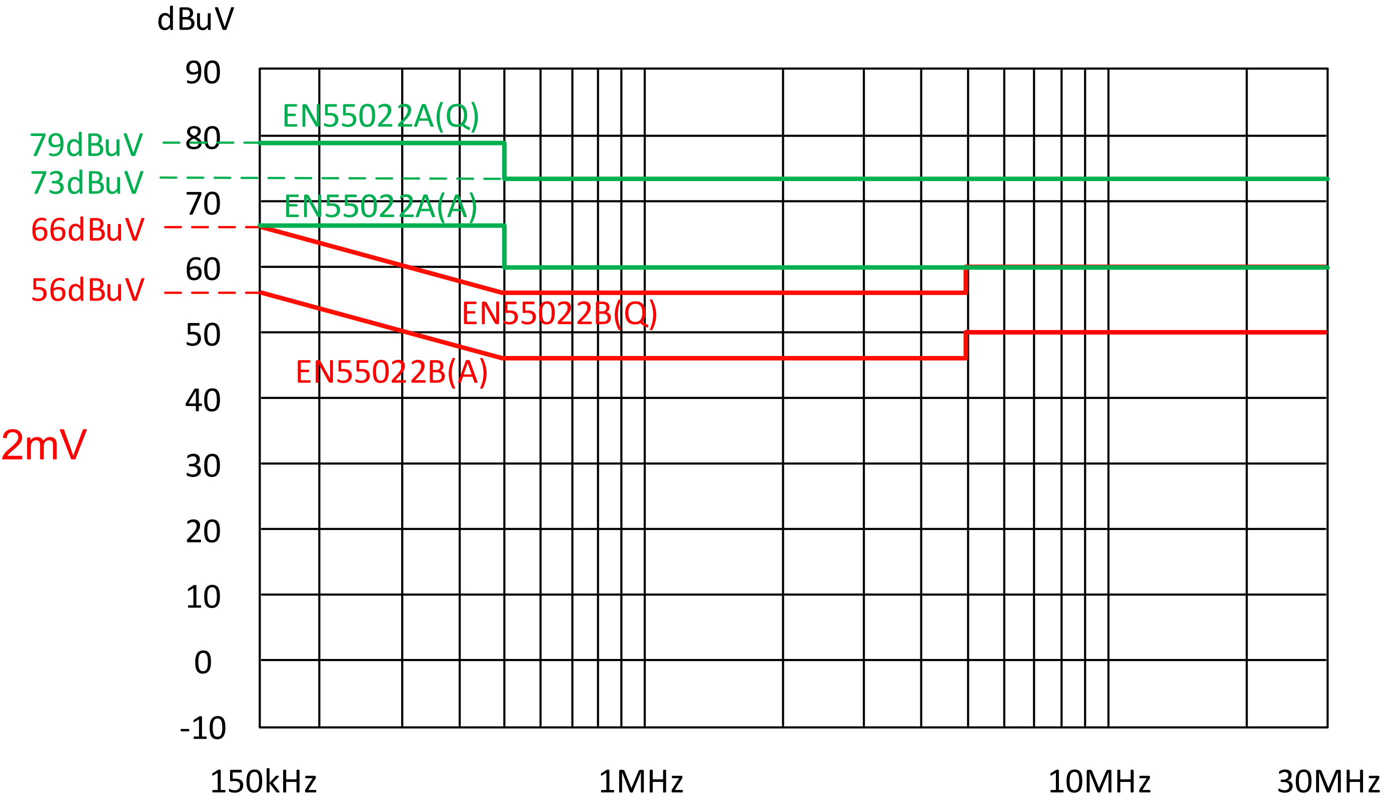
纵坐标对应噪声幅值(单位 dBuV)

$\text{dBuV} = 20\log(uV)$

测量模式：峰值模式；准峰值模式；平均值模式



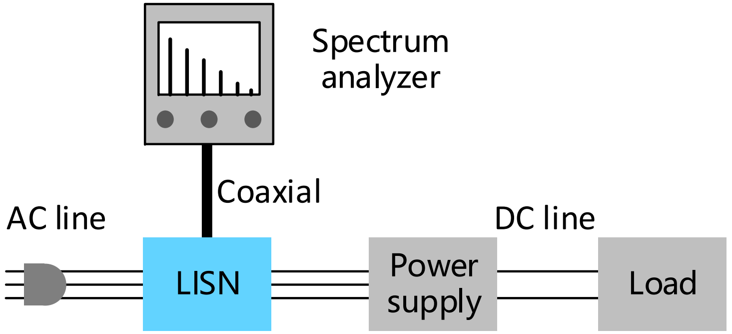
传导测试标准

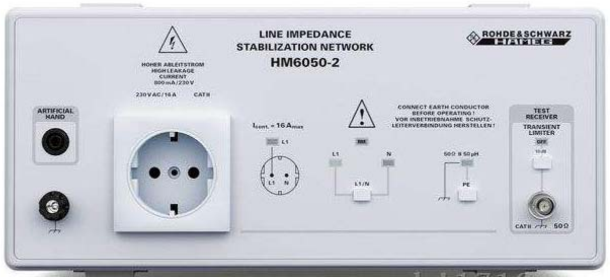


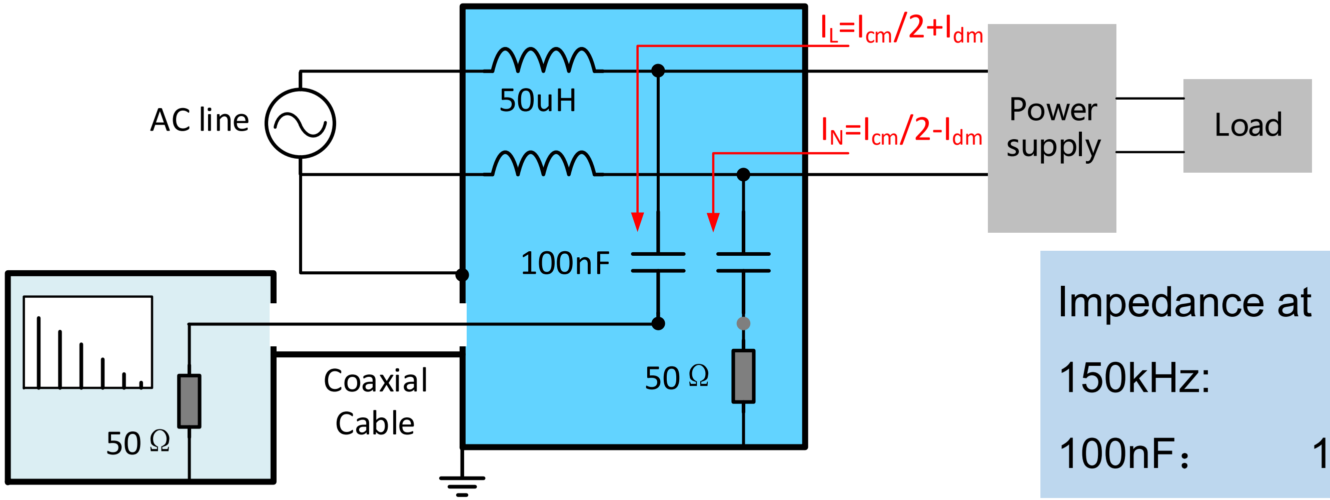
66dBuV≈2mV

电表传导测试采用CISPR 22 Class B= EN 55022 Class B

LISN (Line Impendence Stabilization Network)







Impedance at

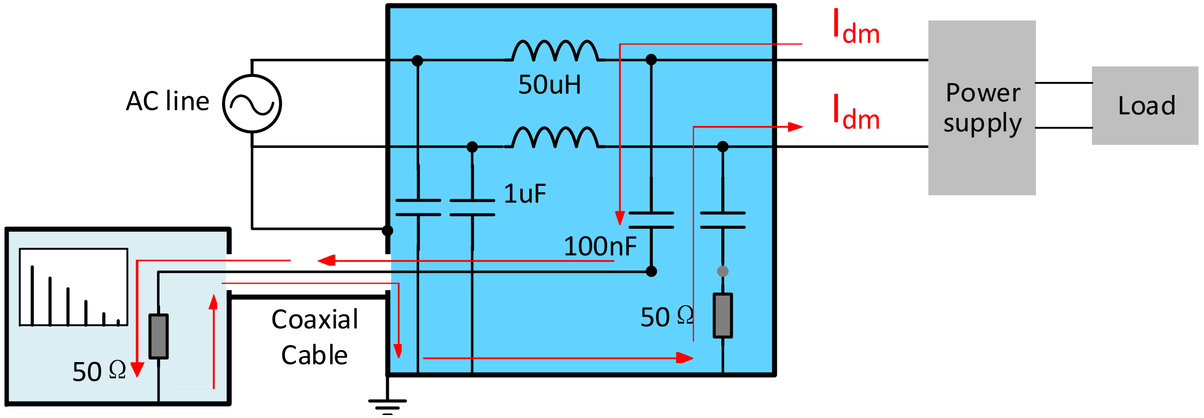
150kHz:

100nF： 10.6Ω

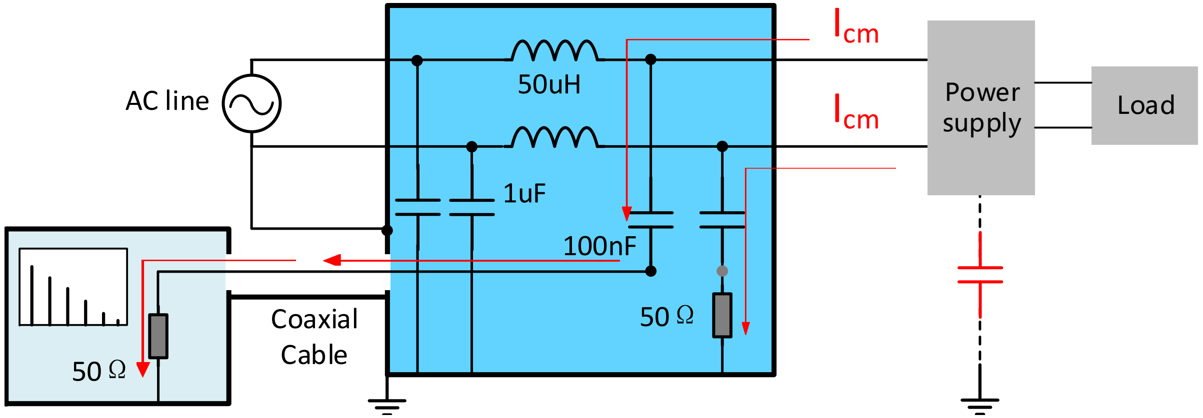
50uH： 47Ω

高频时等效阻抗为50Ω

LISN (Line Impendence Stabilization Network)

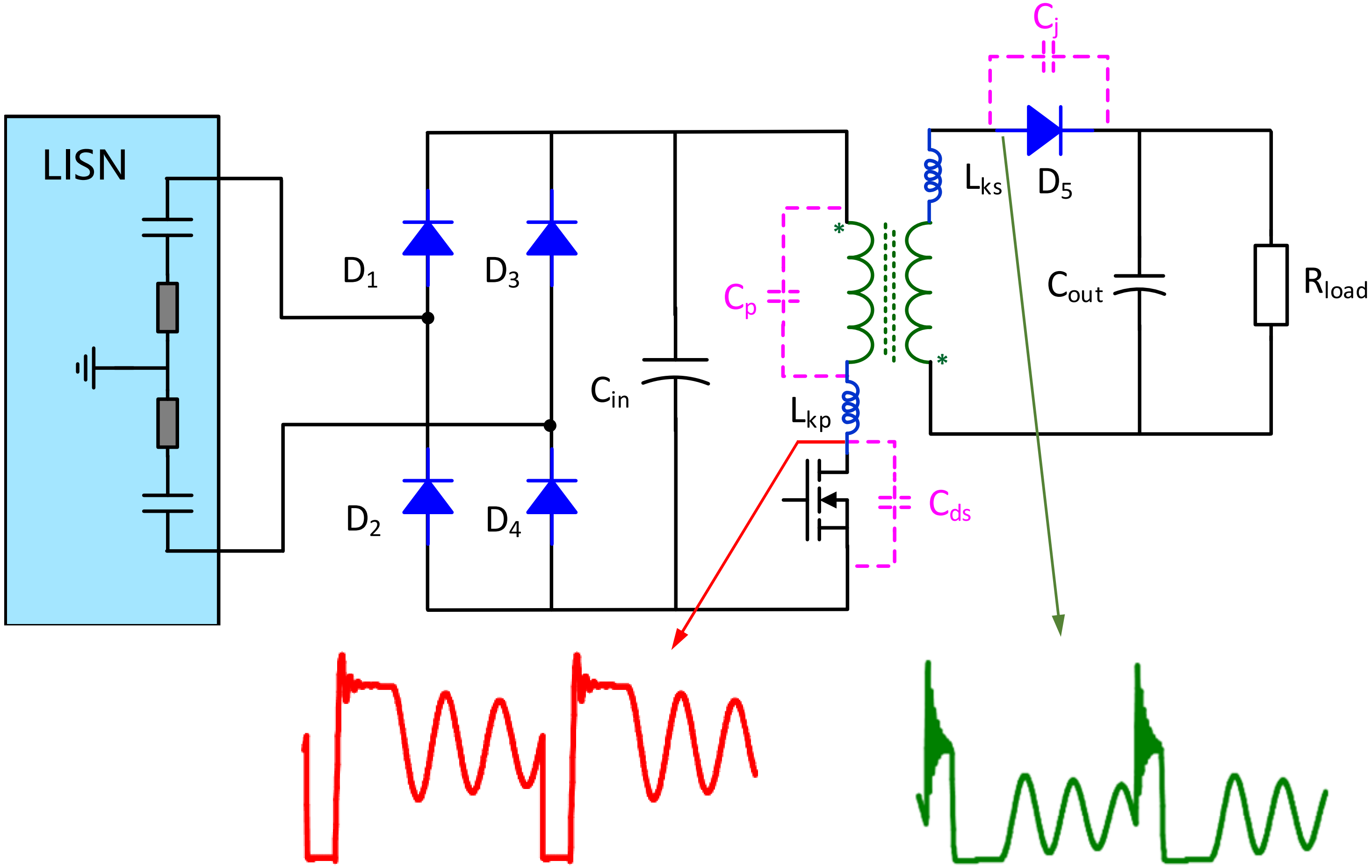


对差模噪声，路径阻抗是100Ω

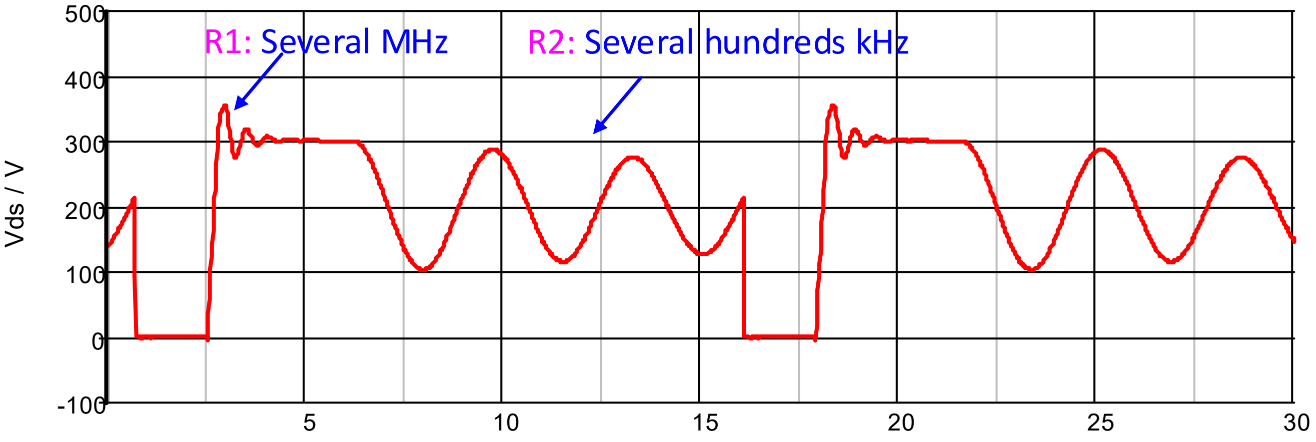


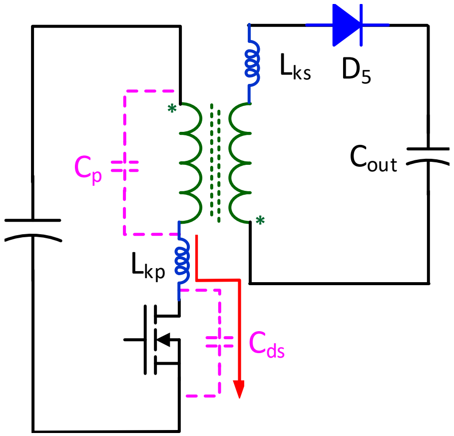
对共模噪声，路径阻抗是25Ω

反激电源噪声源

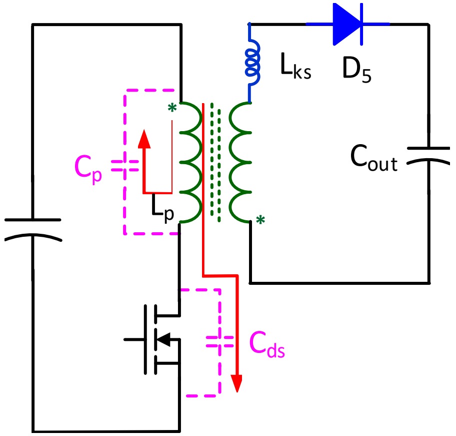


原边电压震荡



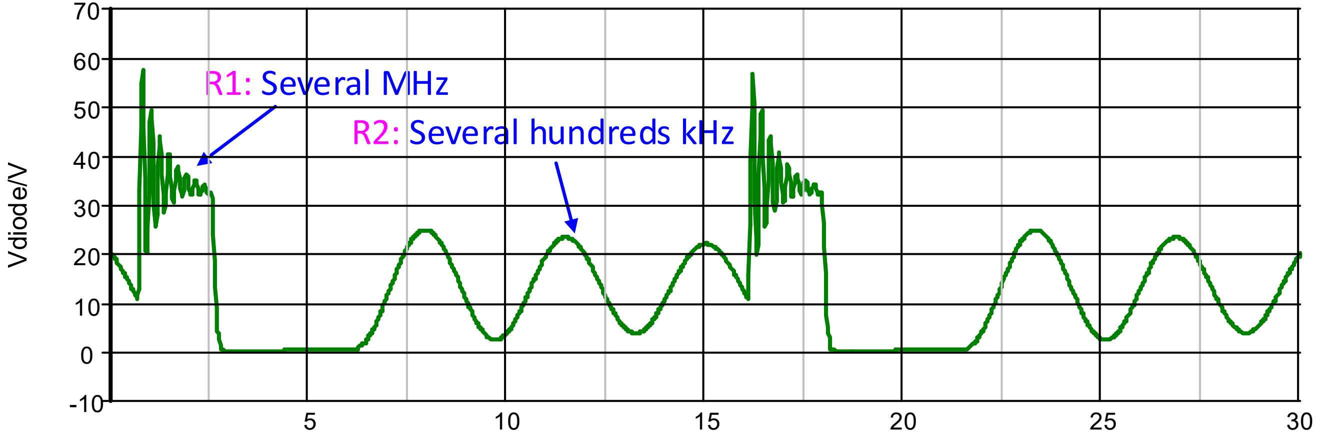


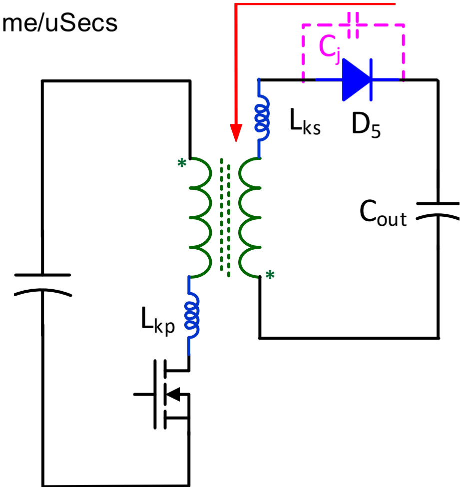
$$f_{MOS} = \frac{1}{2\pi\sqrt{L_{kp}C_{ds}}}$$



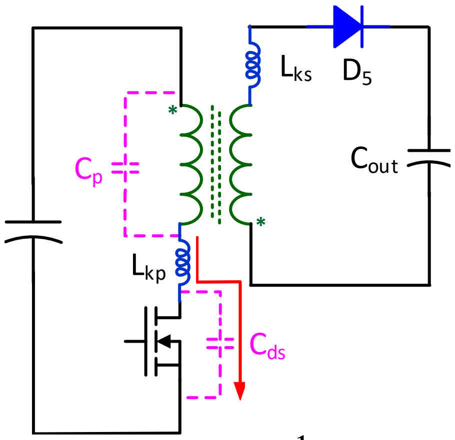
$$f_{MOS} = \frac{1}{2\pi\sqrt{L_p(C_{ds} + C_p)}}$$

输出二极管电压震荡



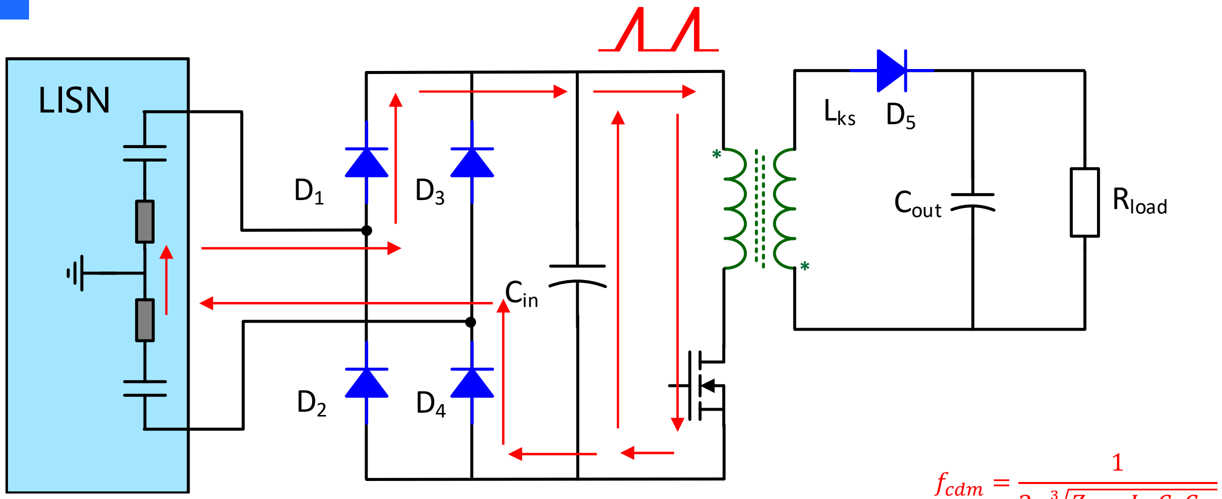


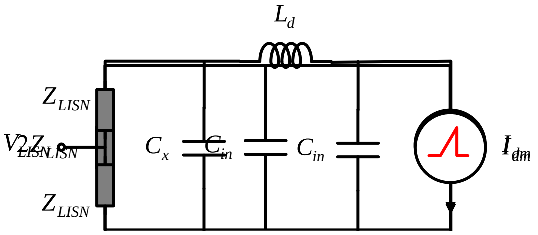
$$f_{Diode}=\frac{1}{2\pi\sqrt{L_{ks}C_j}}$$



$$f_{Diode}=\frac{1}{2\pi\sqrt{L_{kp}C_{ds}}}$$

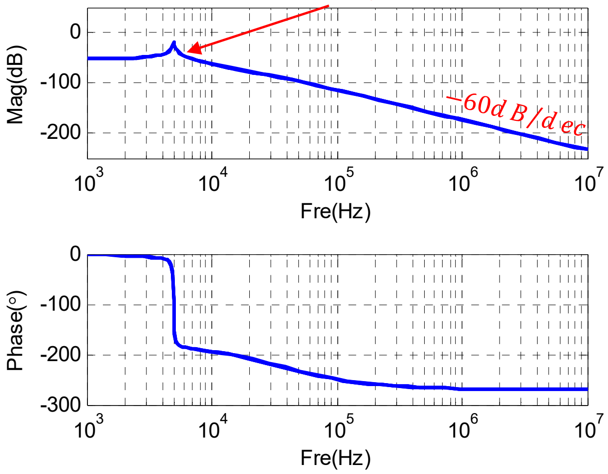
差模噪声路径



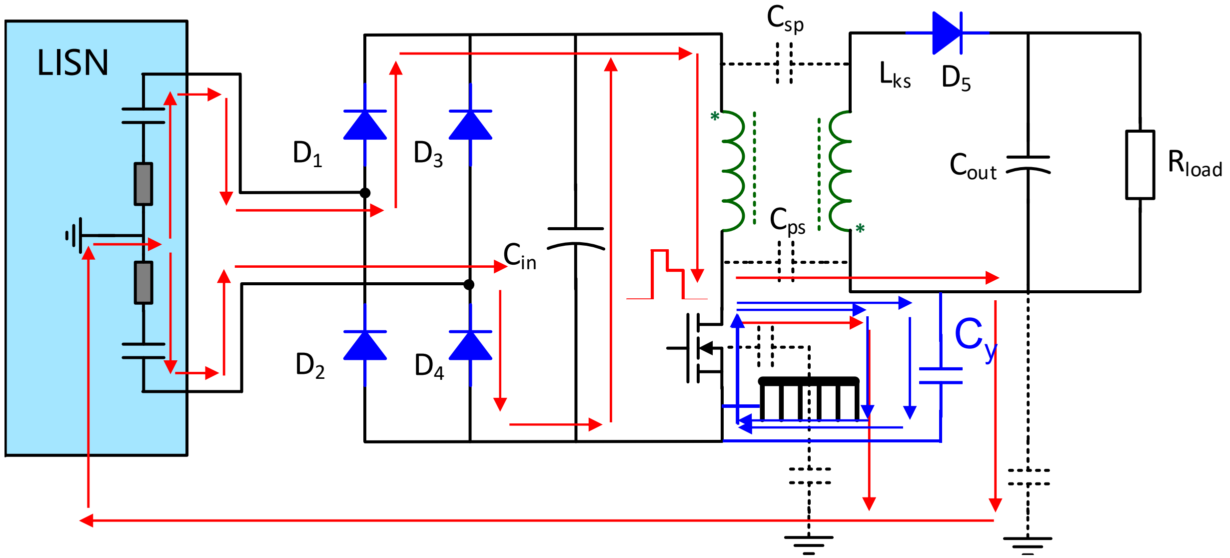


$$\frac{V_{LISN}}{I_{dm}}=\frac{50}{2Z_{LISN}L_dC_xC_{in}s^3+L_dC_{in}s^2+2Z_{LISN}(C_x+C_{in})s+1}$$

$$f_{cdm}=\frac{1}{2\pi\sqrt[3]{Z_{LISN}L_dC_xC_{in}}}$$

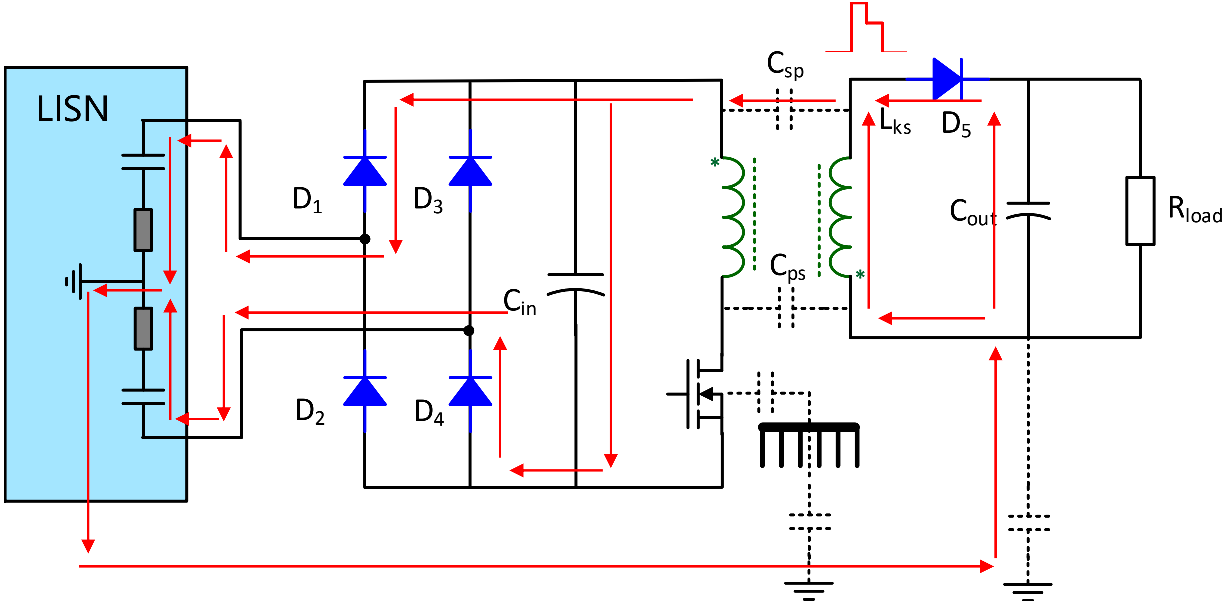


共模噪声路径

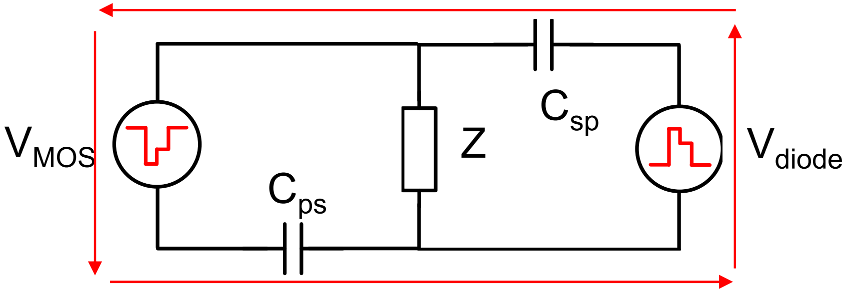


- ➢ Decrease dv/dt of MOS by increase driver resistor or add Cds
- ➢ Add Y capacitor to provide additional path
- ➢ Ground heat sink to provide additional path
- ➢ Add CM inductor to block the noise path
- ➢ Decrease parasitic Cps of transformer

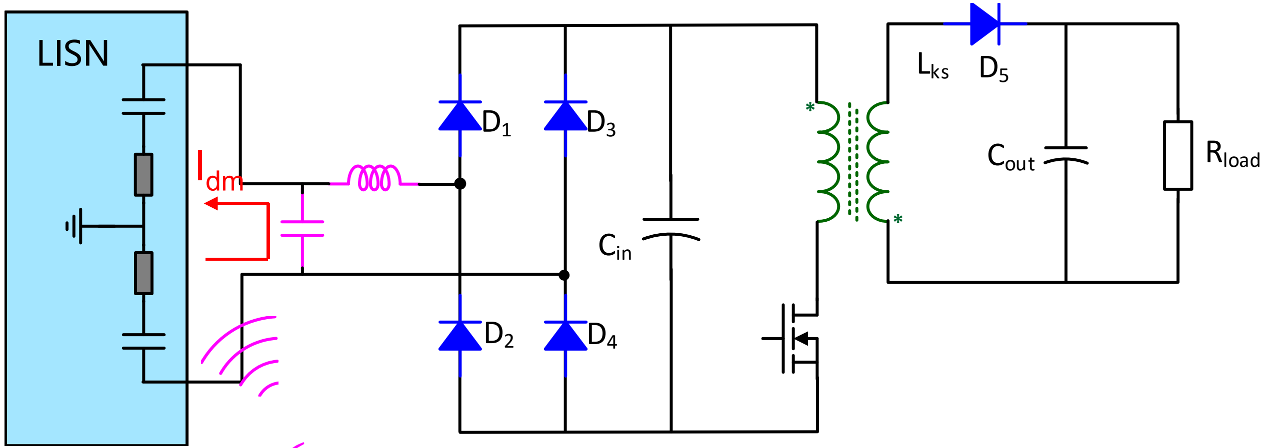
共模噪声路径

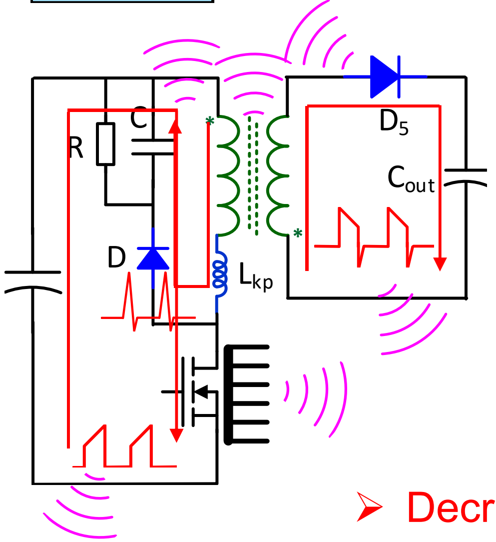


- 副边二极管产生的共模噪声与原边MOS产生的共模噪声方向相反



空间耦合路径

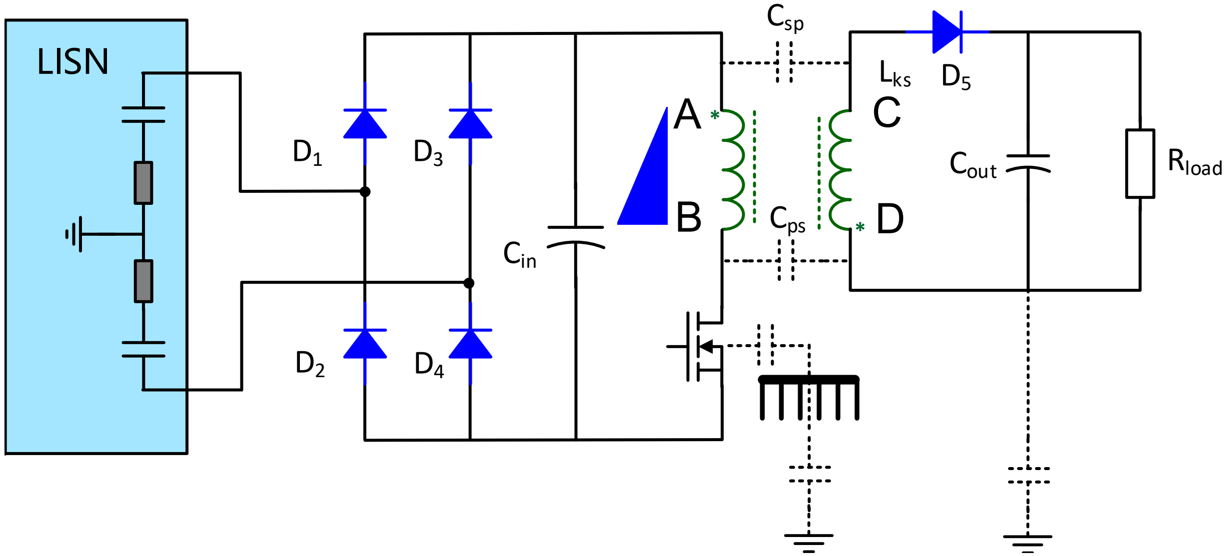


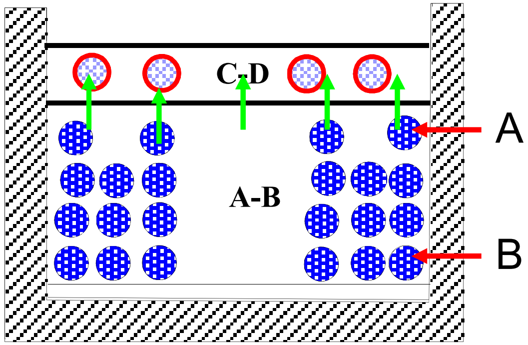


1. Caused by MOS, heat sinker and Diode dv/dt
2. Caused by input current loop, CCM is worse
3. Caused by output current loop, CCM is worse
4. Caused by RCD current loop
5. Caused by transformer core

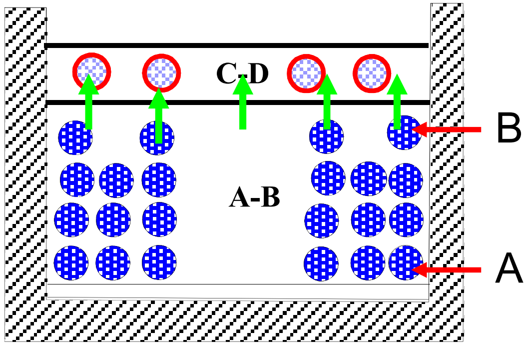
- Decrease receiving and transmitting loop area
- Ground transformer core and heat sinker

变压器绕法的影响



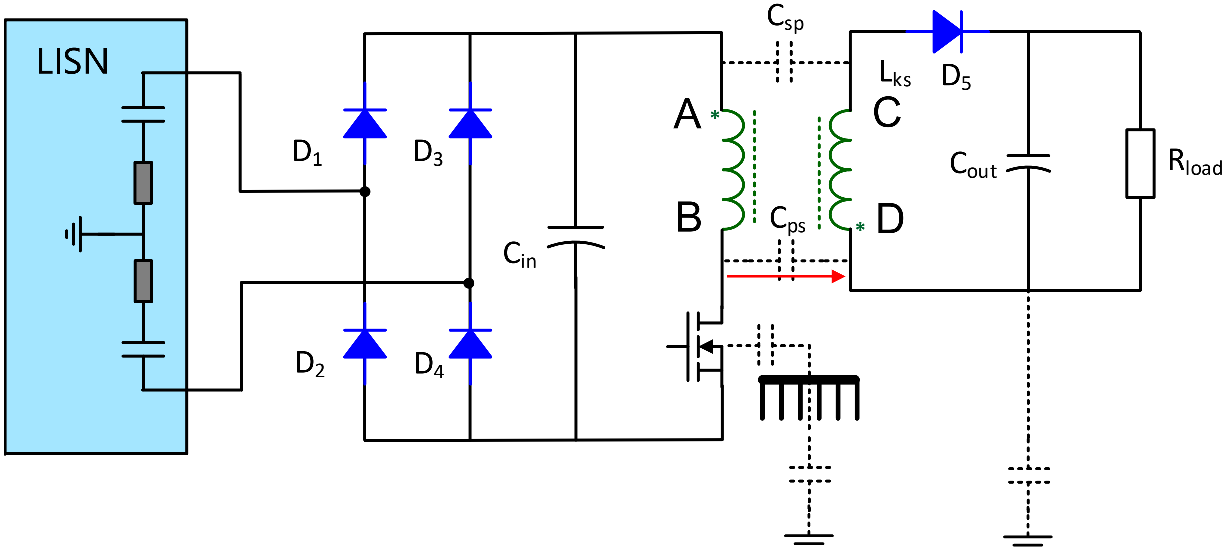


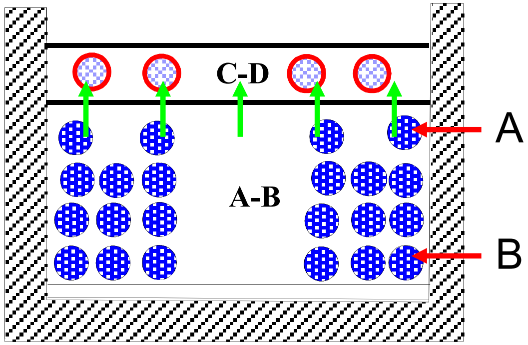
效果好



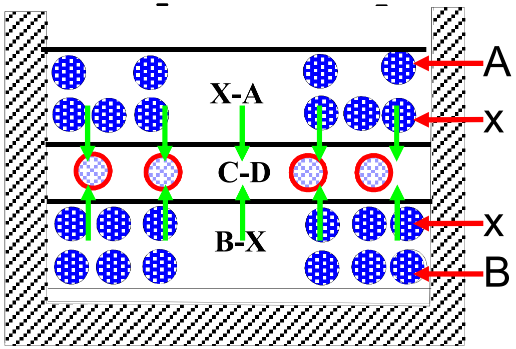
效果差

变压器绕法的影响



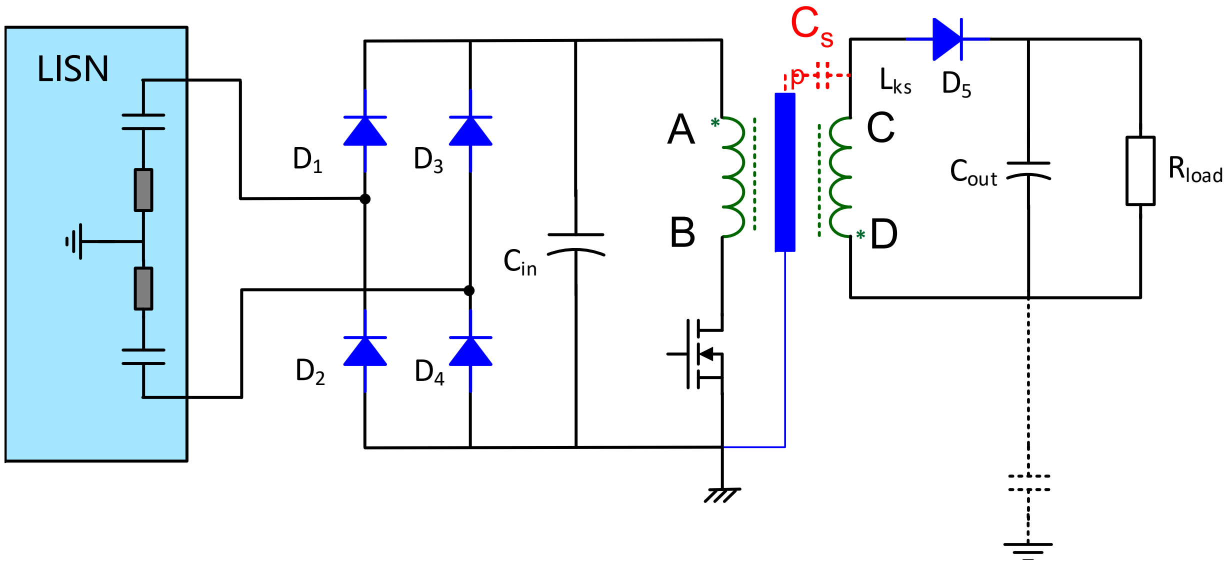


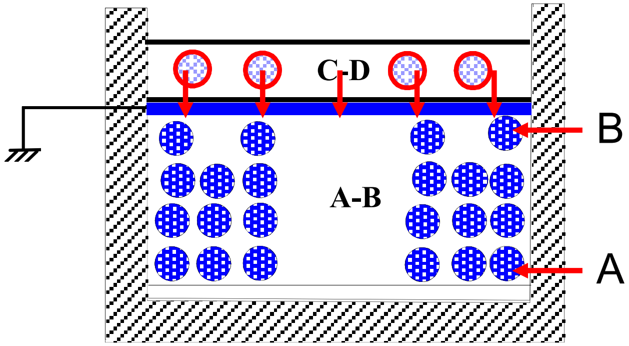
效果好



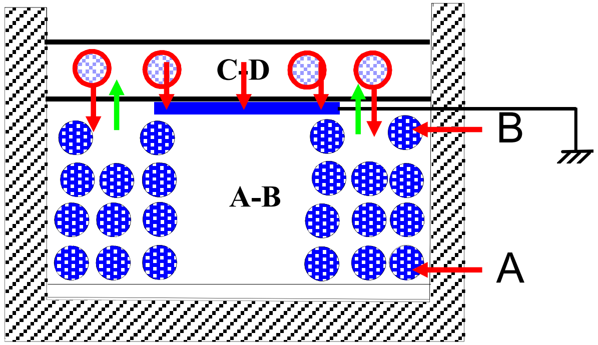
效果差

变压器绕法的影响



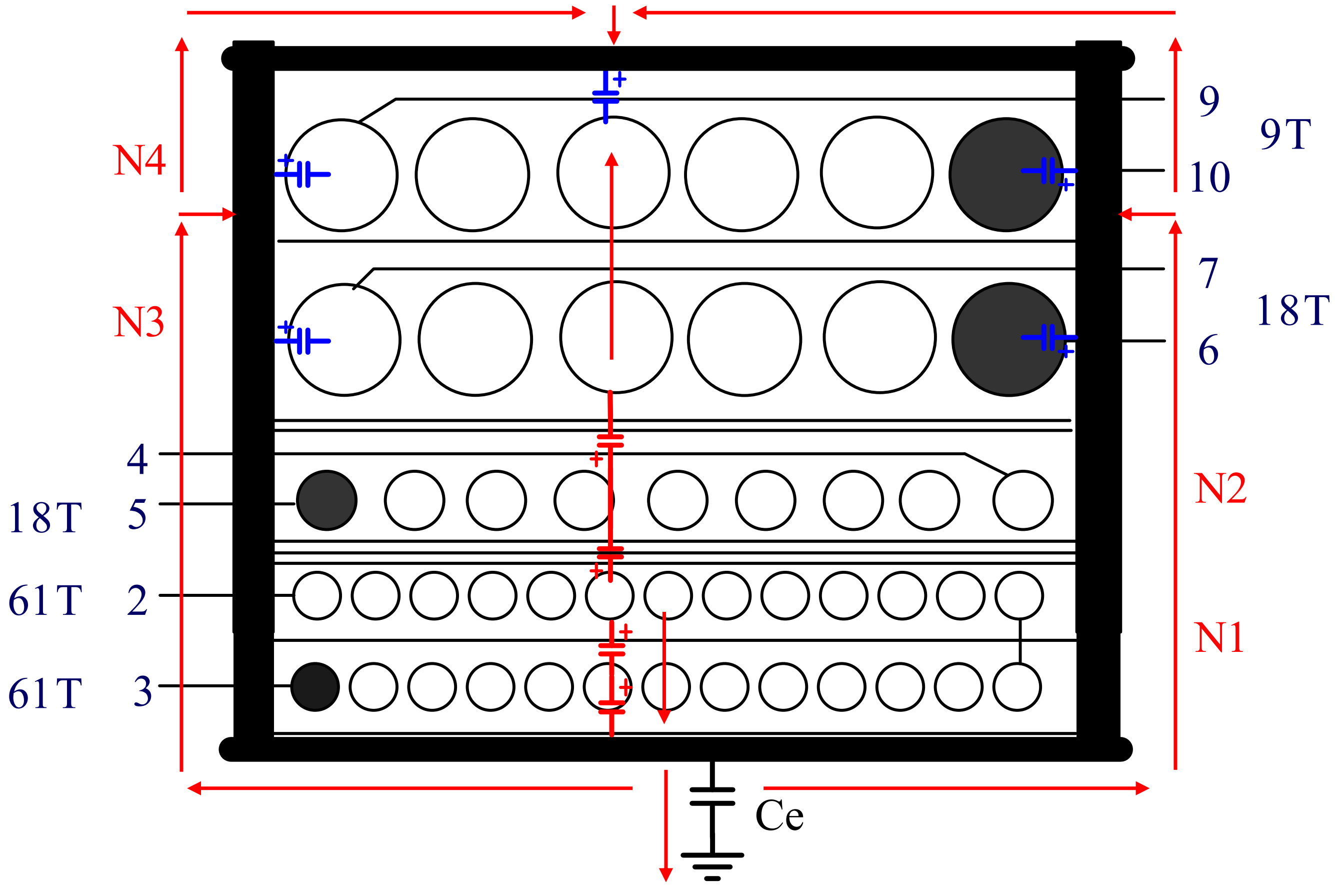


效果好

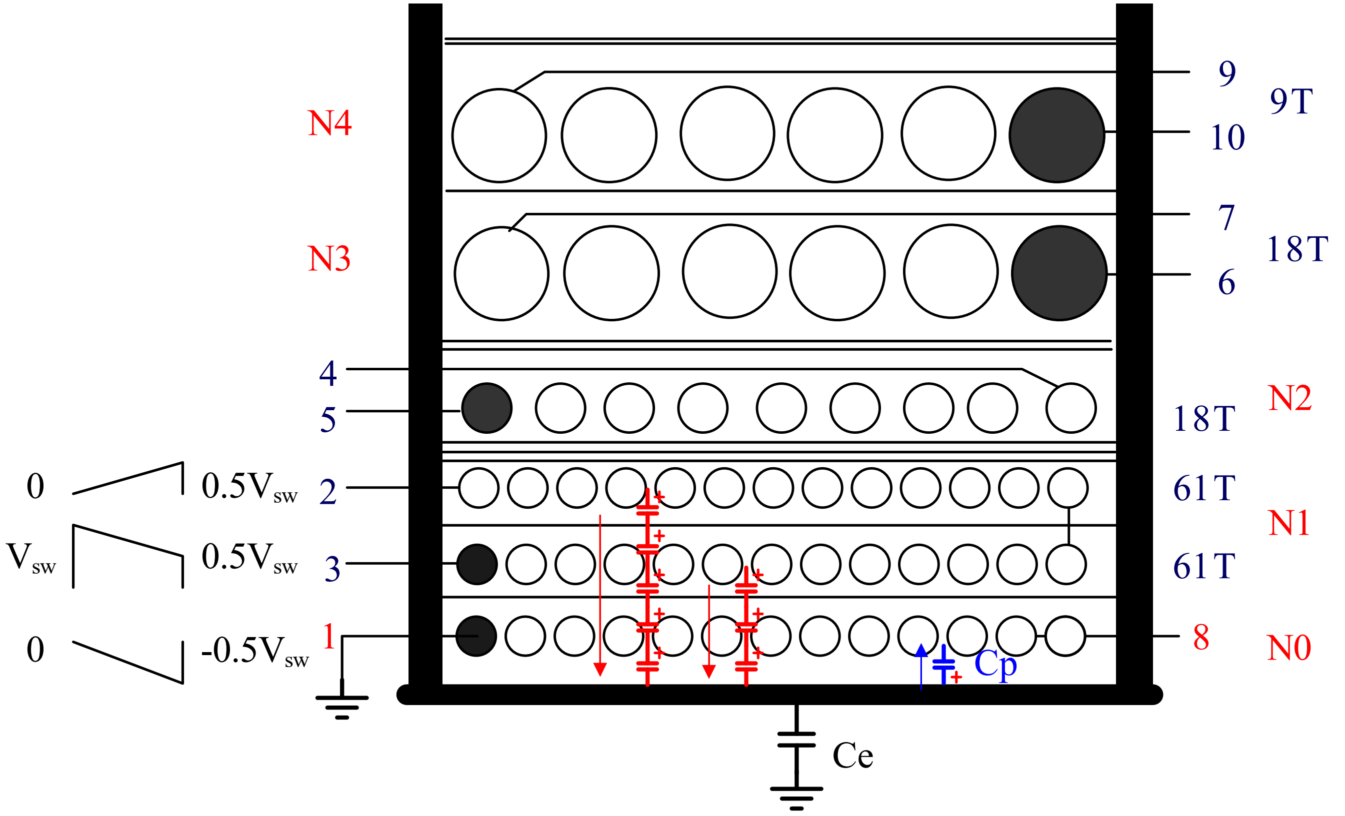


效果更好

变压器中的共模噪声路径



变压器补偿绕组



粗略假设层与层之间寄生电容大小相等

从N1绕组流向变压器磁芯的电流:

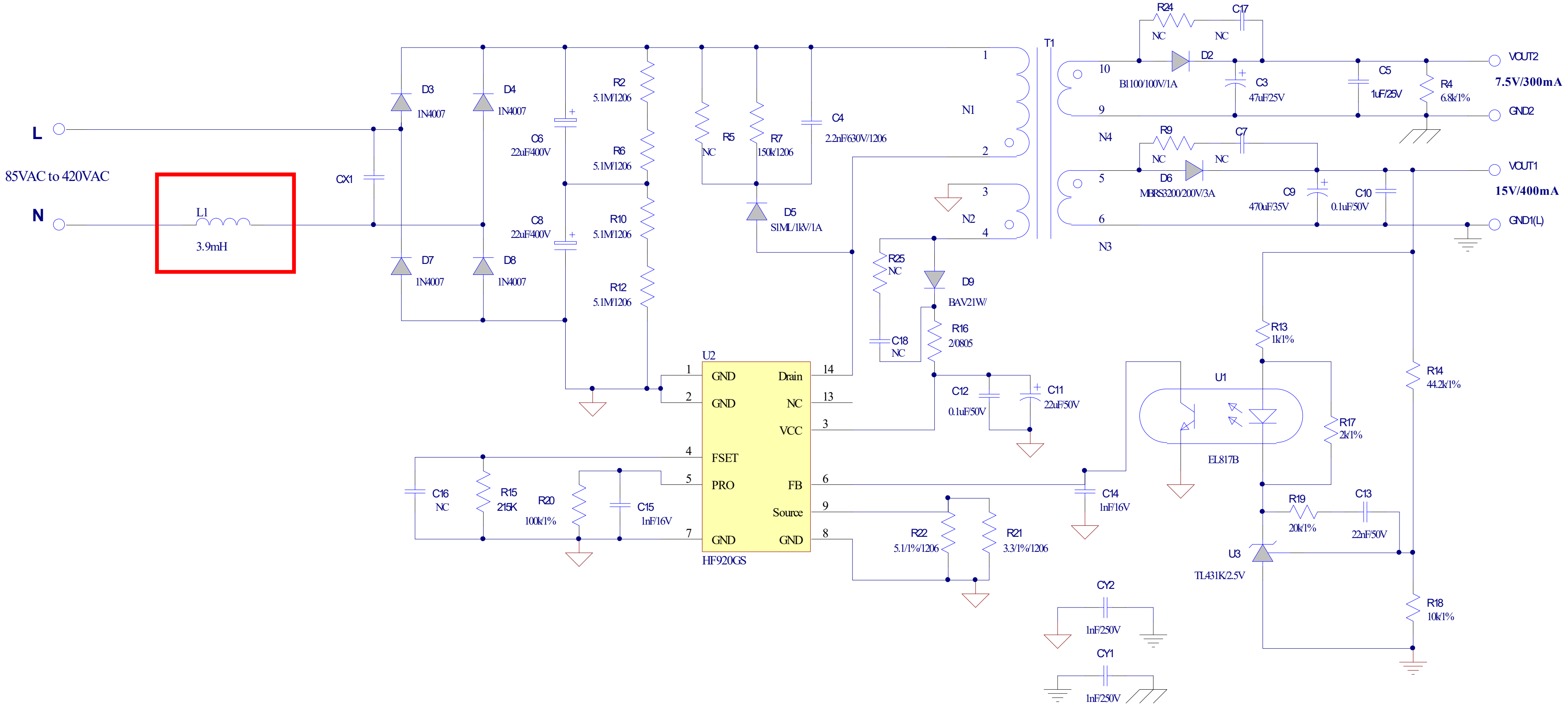
$$\frac{C_P}{5}\frac{\frac{1}{2}\frac{V_{SW}}{2}}{\Delta T}+\frac{C_P}{3}\frac{\frac{1}{2}\left(\frac{V_{SW}}{2}+V_{SW}\right)}{\Delta T}=\frac{3}{10}C_P\frac{V_{SW}}{\Delta T}$$

从变压器磁芯流回N0绕组的电流:

$$C_P\frac{\frac{1}{2}\frac{V_{SW}}{2}}{\Delta T}=\frac{1}{4}C_P\frac{V_{SW}}{\Delta T}$$

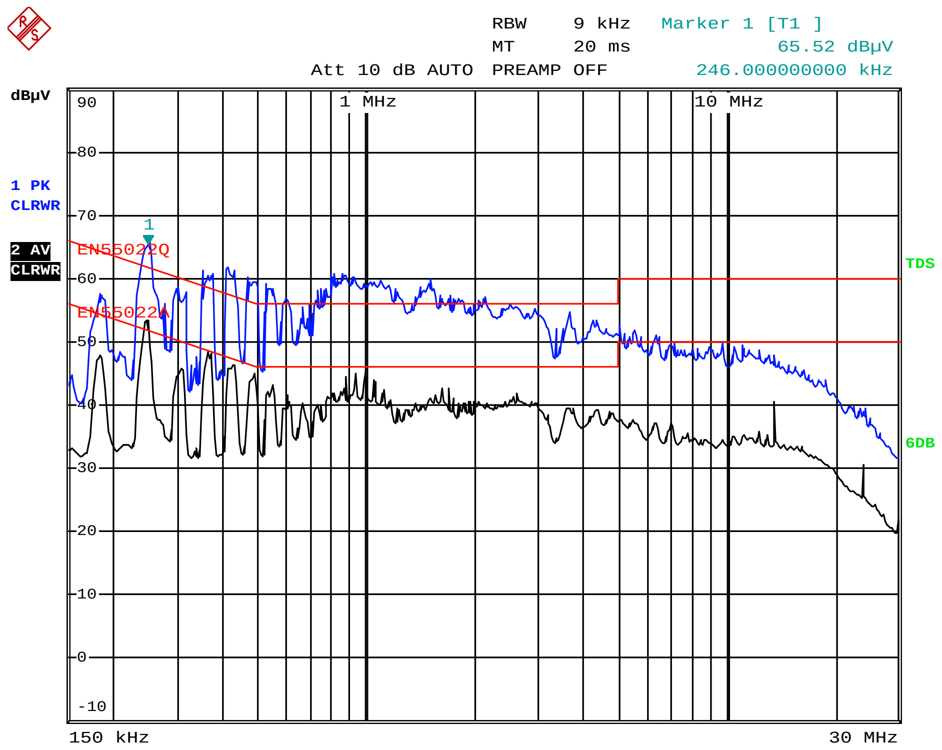
N1流出电流和流回到N0的电流接近

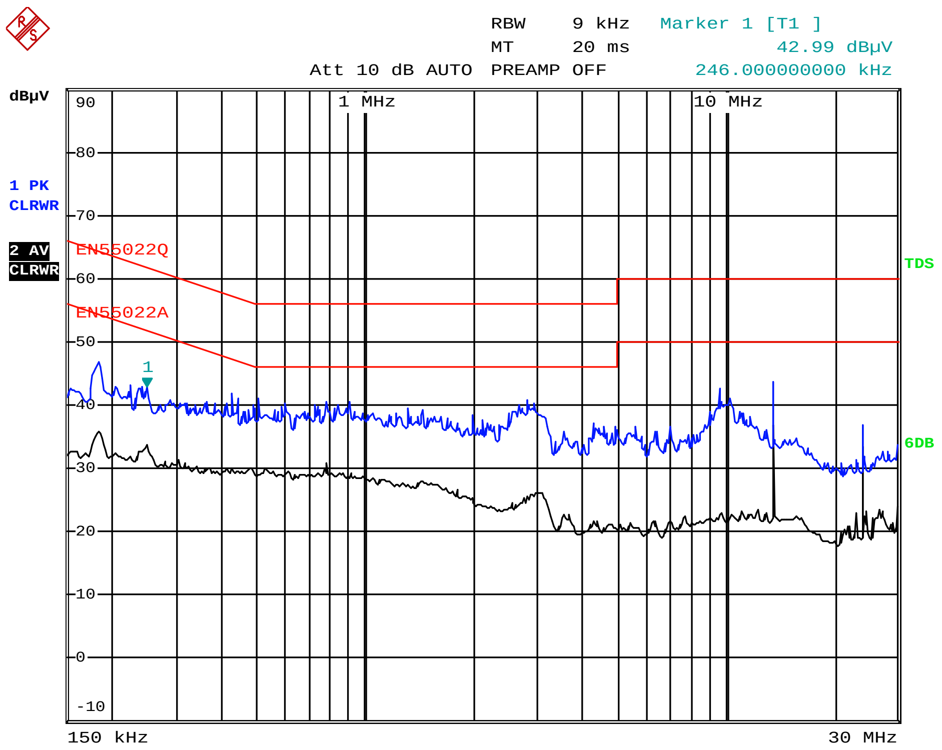
基于HF920的实验验证



N线上加差模电感，抑制差模，将部分差模转换为共模

采用普通顺序绕法变压器





N线传导结果好于L线，两者之间的差异由共模噪声产生

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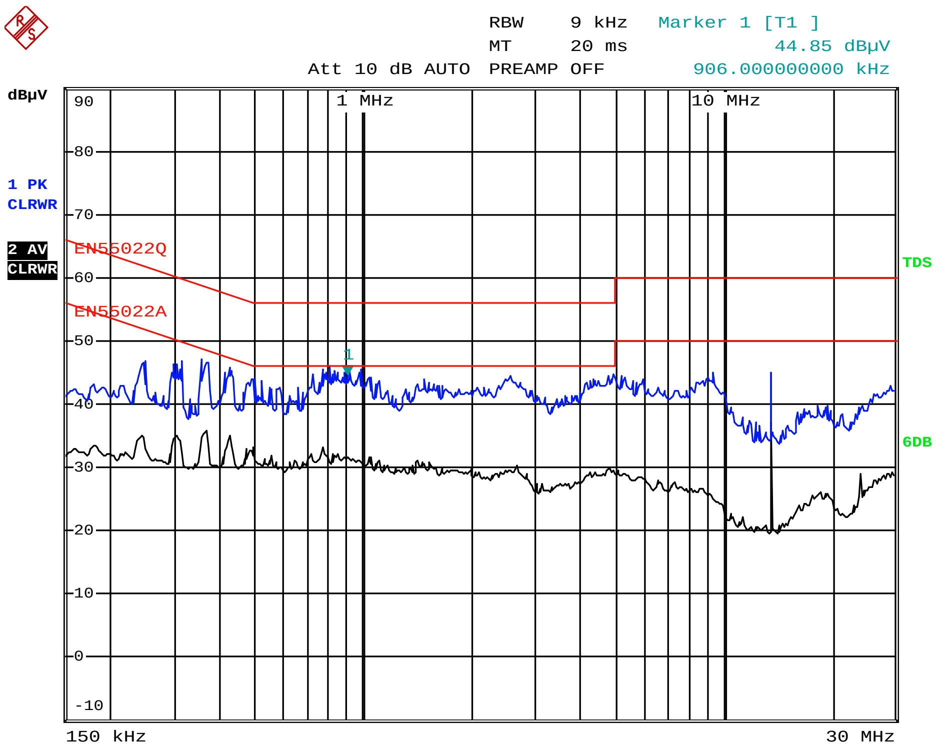
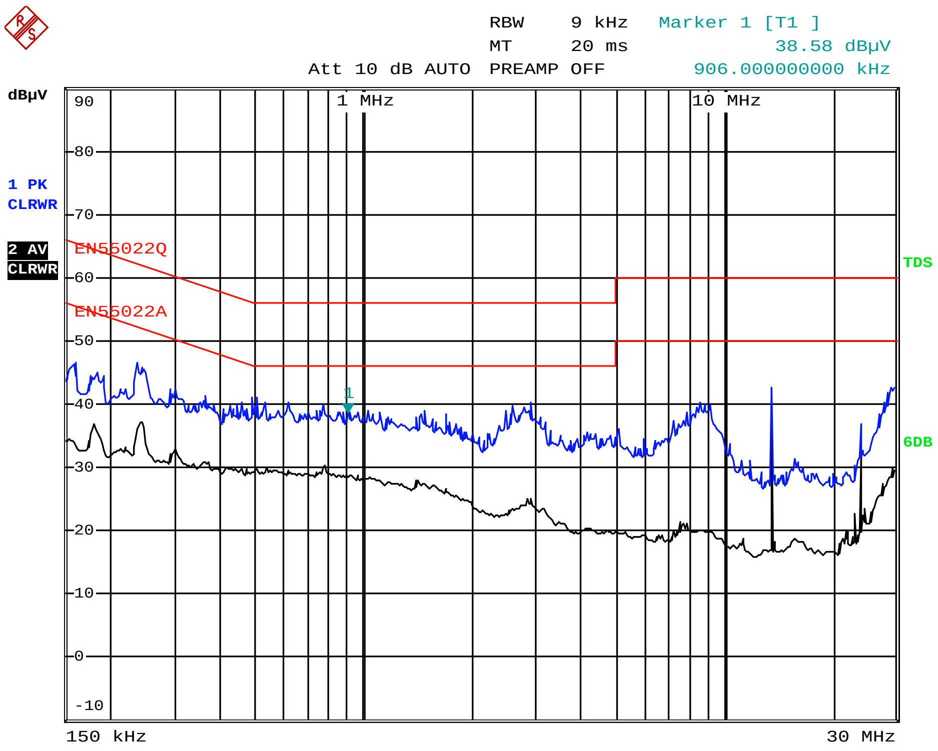
顺序绕法变压器加补偿层



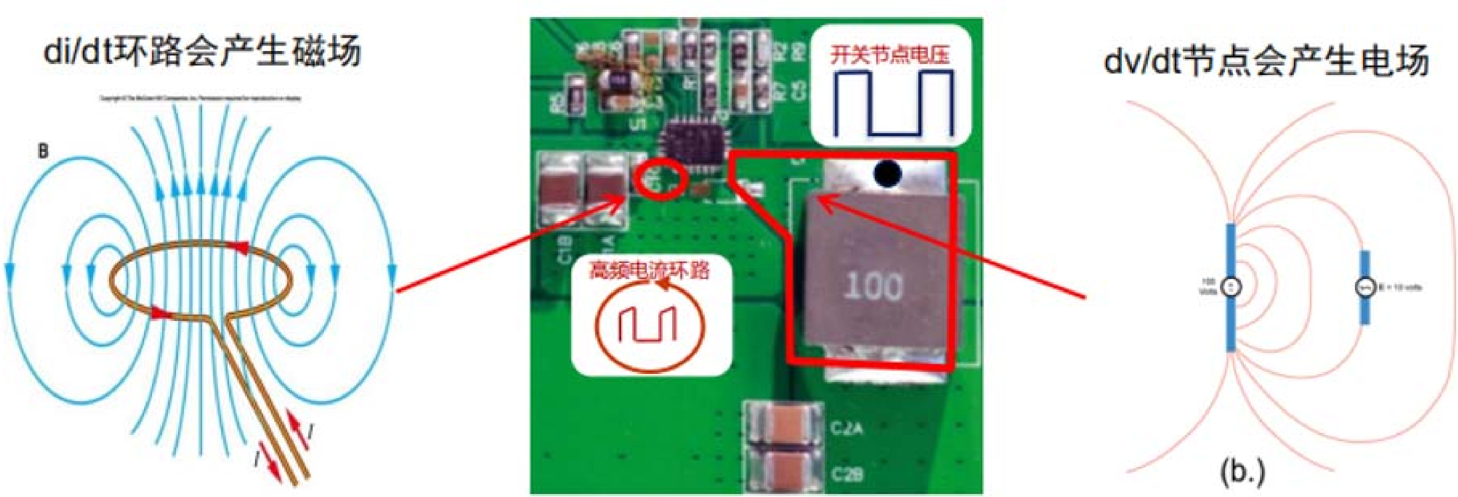


补偿层阻断共模路径，L和N线传导得到有效抑制

Date: 8.JUN.2019 02:10:54

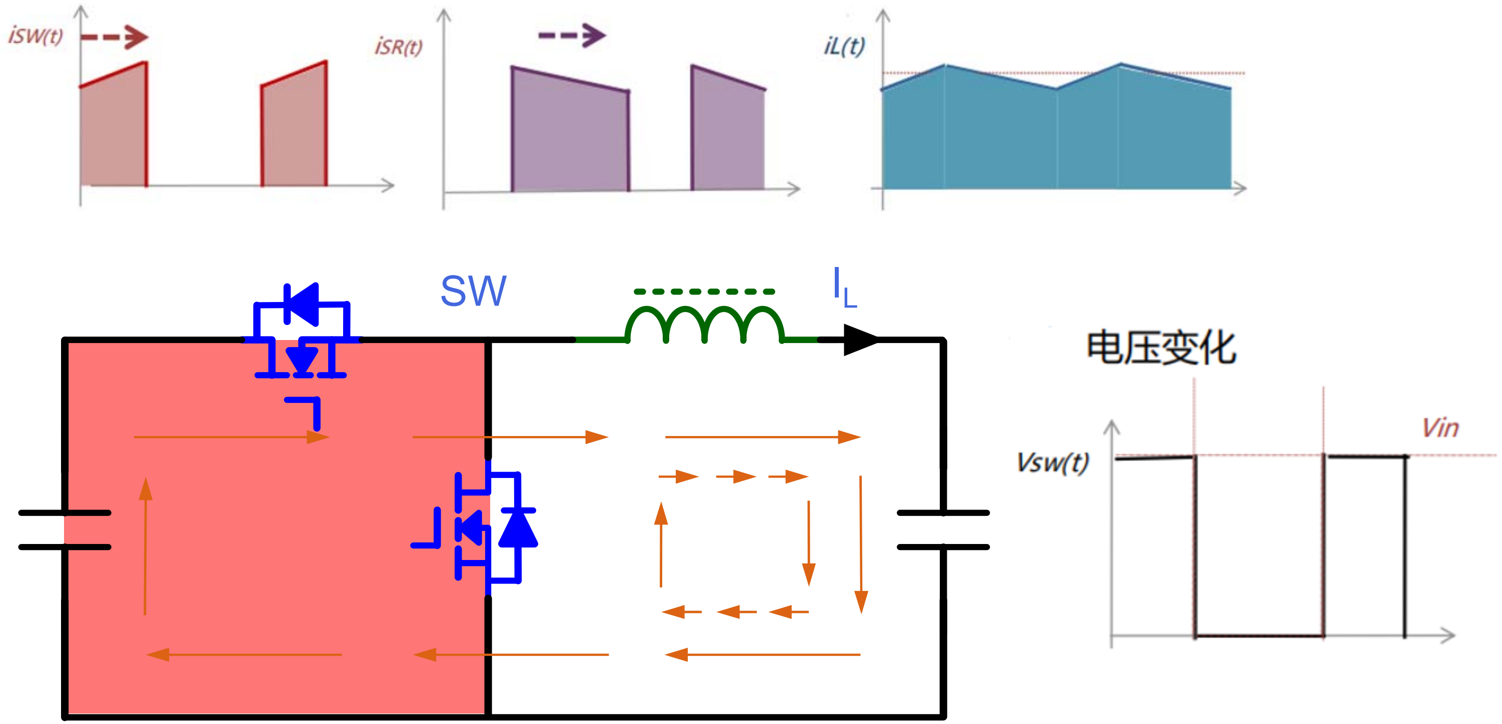
DCDC噪声源

DCDC 两大噪声源



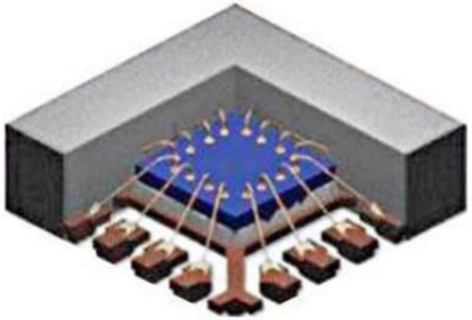
高频电流回路和高频电压节点共同产生高频噪声

BUCK的噪声源

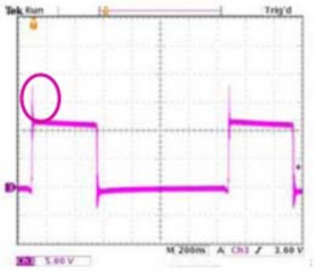


SW和电感电压跳变带来DV/DT噪声；电流环路带来DI/DT噪声

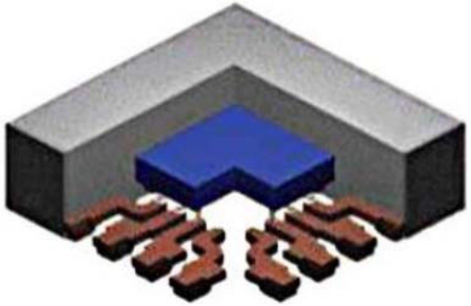
芯片设计优化EMI



Parasitic inductance from wire bond is bad for EMI



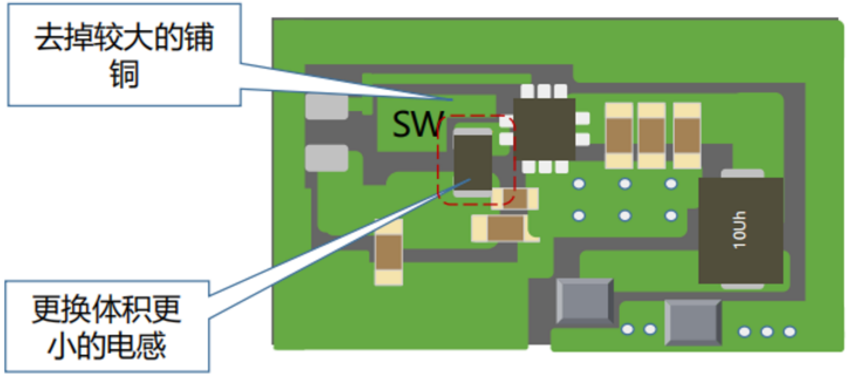
VS.



First in the World:
Mesh Connect Technology Eliminated
Eliminated wire bond and better EMI

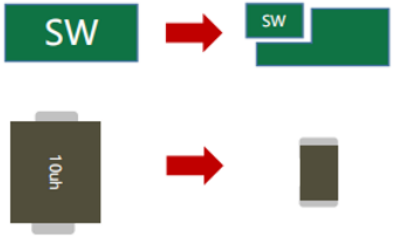
no more ringing or overshoot!

减小电压跳变节点



去掉较大的铺铜

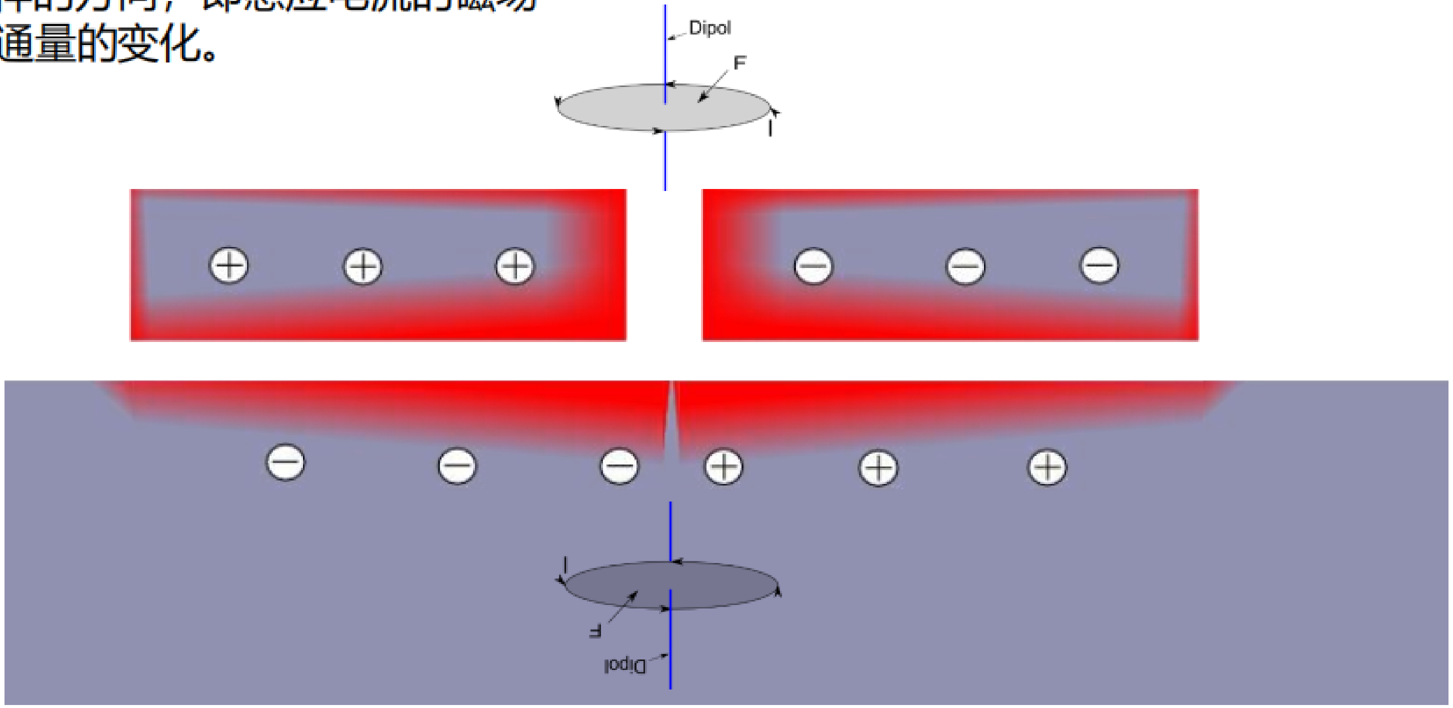
更换体积更小的电感



高频电流环路噪声源的抑制

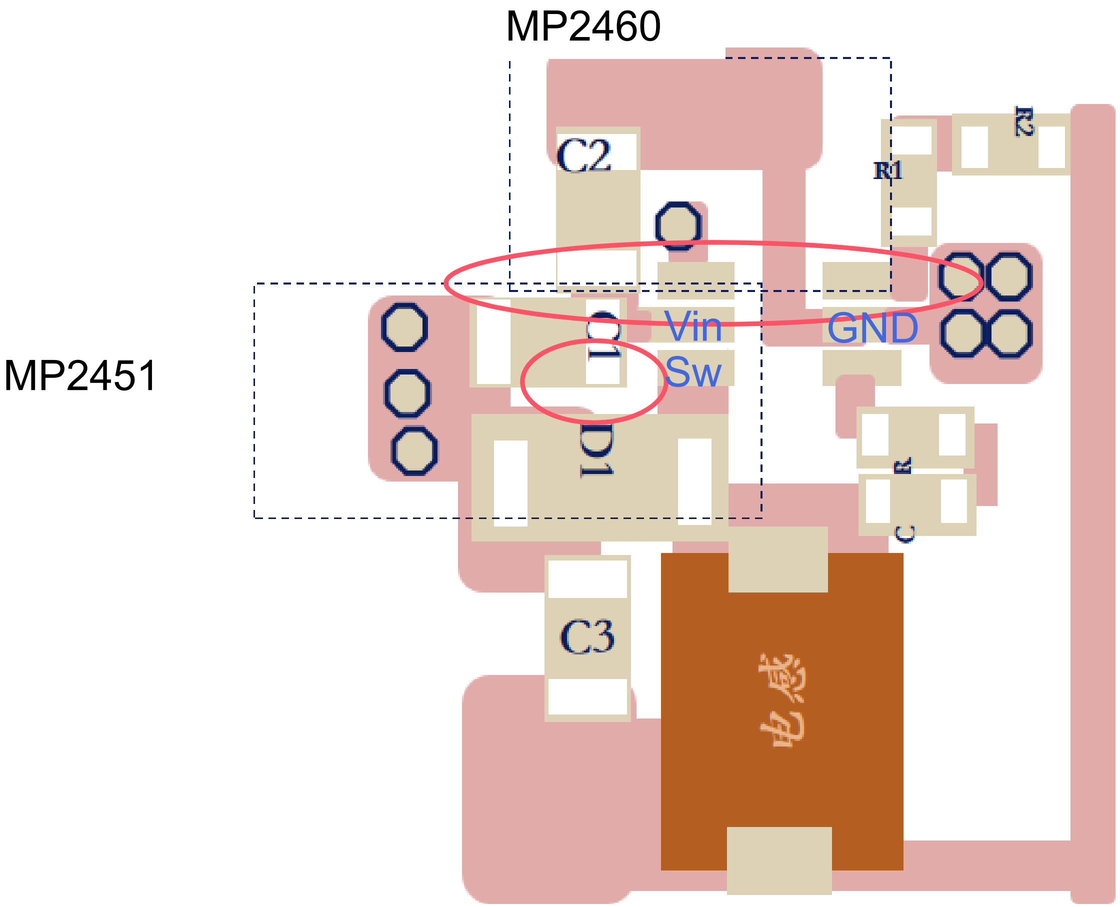
高频电流环路底层完整PCB铺铜

楞次定律：感应电流具有这样的方向，即感应电流的磁场总要阻碍引起感应电流的磁通量的变化。



完整的地平面可以感应出电流，并形成相反的磁场来抵消高频环路带来的磁场。

PCB 布板推荐



Thank you!