EMI Considerations in Flyback Transformer Design

反激变换器变压器EMI设计的通用方法

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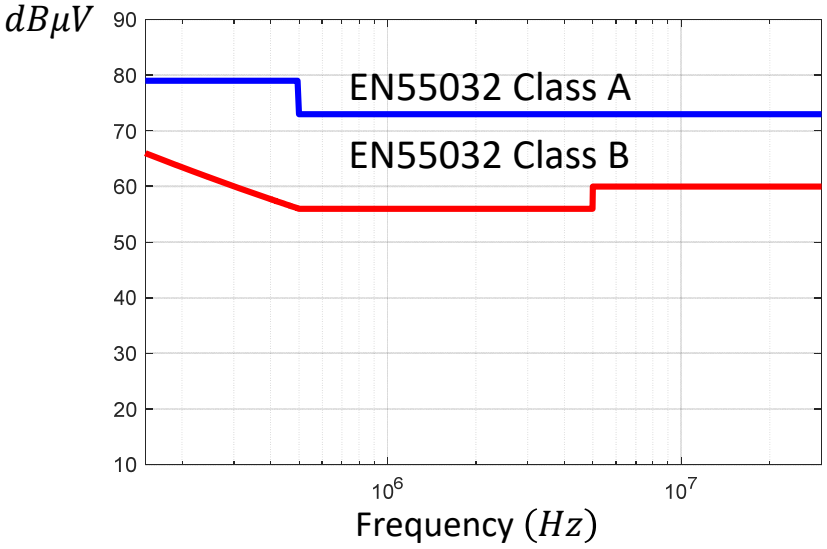
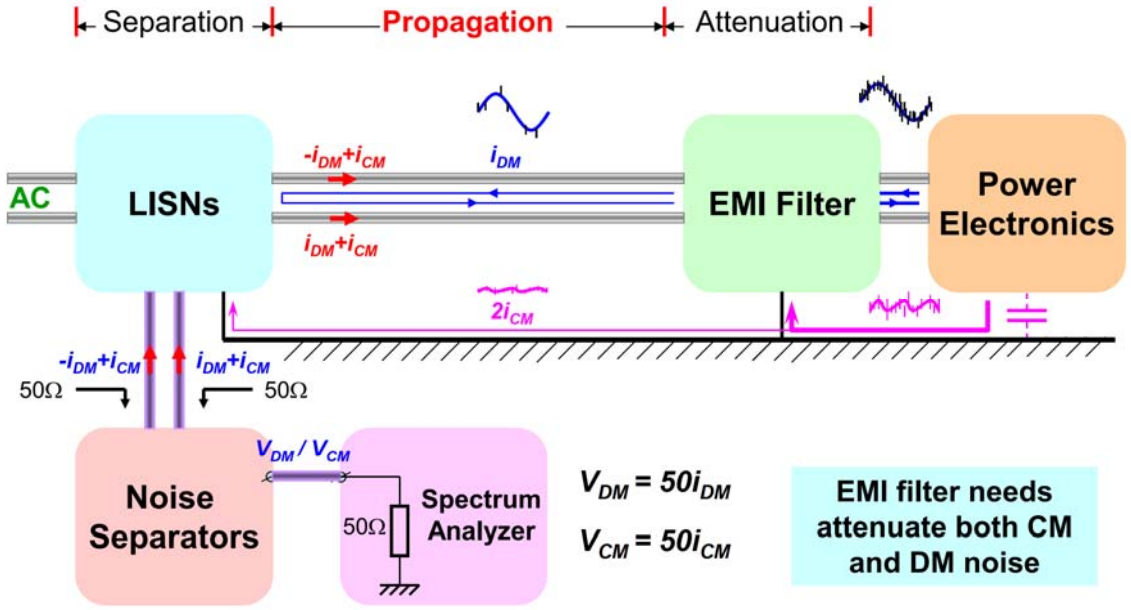
Conducted EMI Noise and Standard

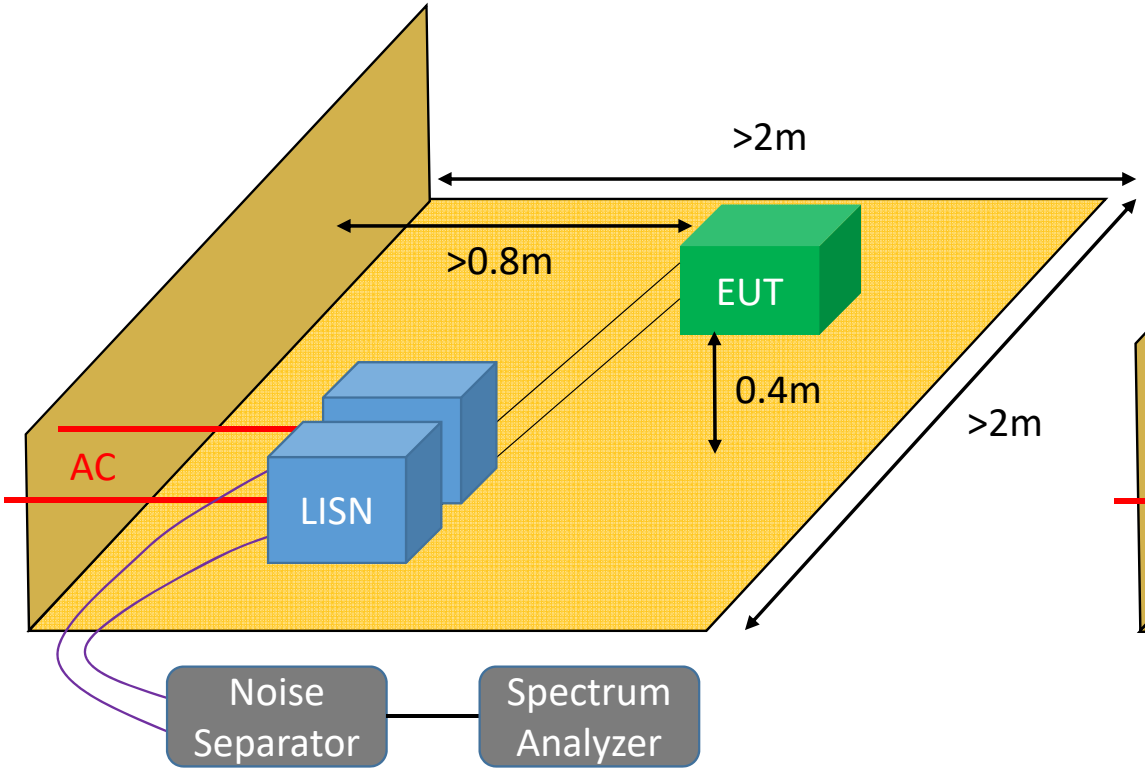
- Conducted Electromagnetic Interference (EMI)
  - The switches in a converter operate at high frequencies and generate high dv/dt nodes in the circuit, which leads to undesired noise flowing in the circuit.
- Conducted EMI: Common Mode (CM) and Differential Mode (DM) Noise.
- Standards such as CISPR22 or EN55032 regulate the conducted EMI (150kHz to 30MHz).



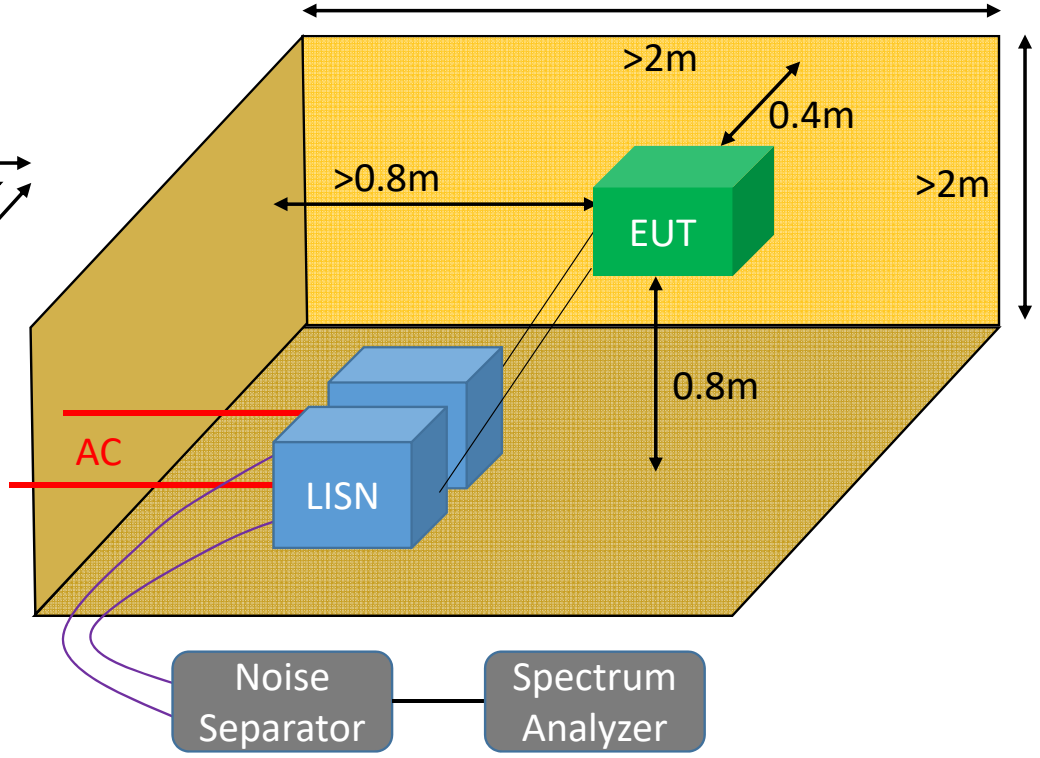


Conducted EMI Measurement Setup (EN55022/32)

Vertical Reference Ground Plane

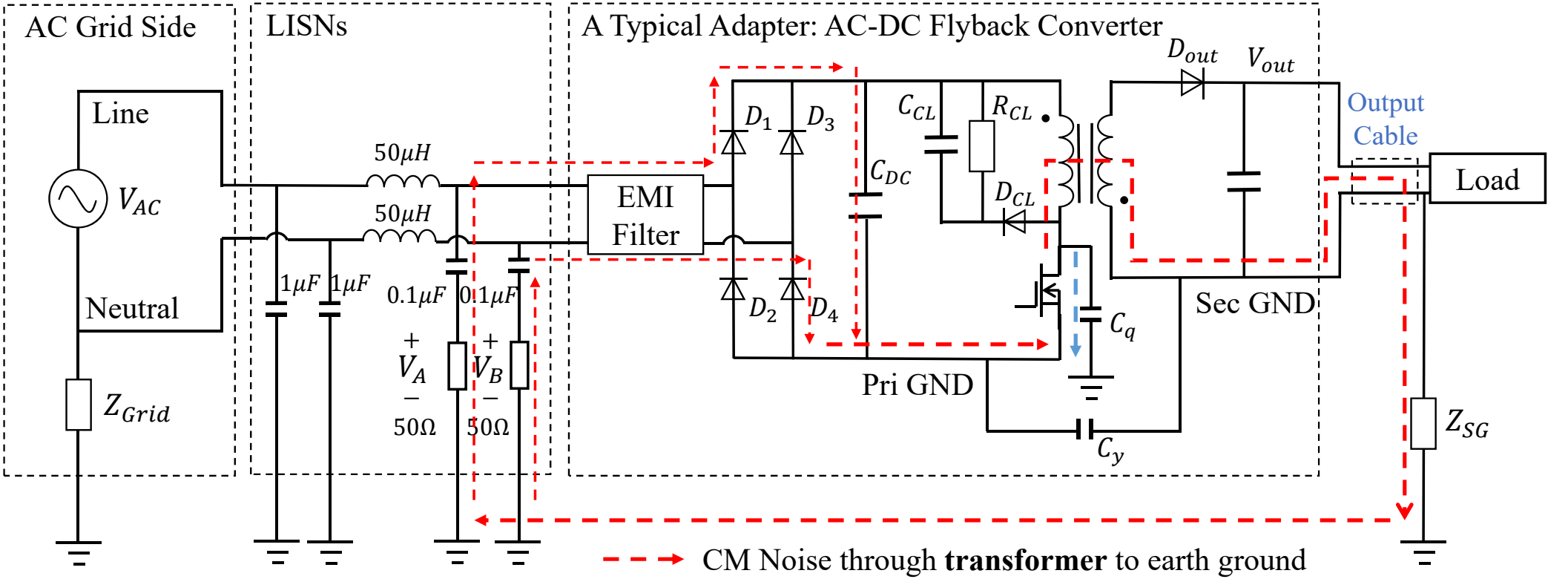


Horizontal Reference Ground Plane



Note: The distance between the reference ground plane and the EUT shall be 0.4m.

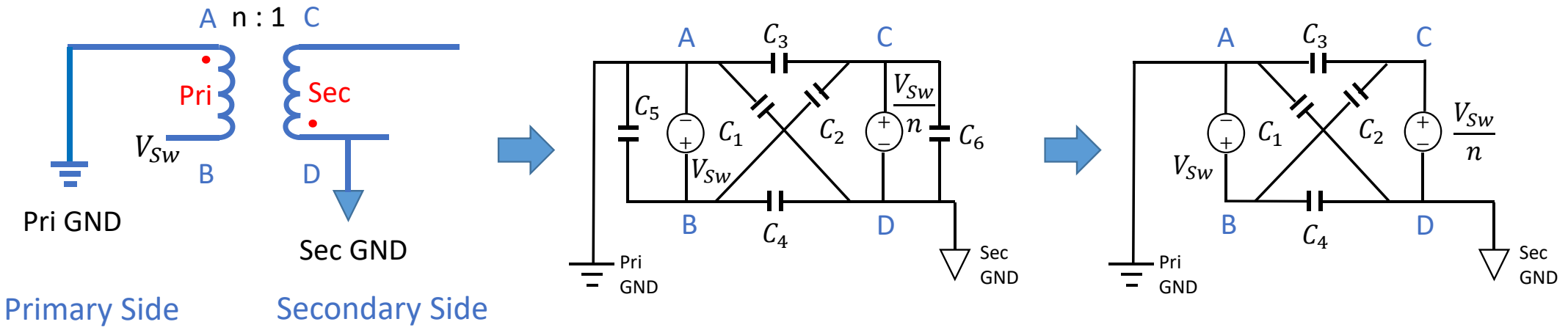
Common Mode (CM) Noise Path in a Flyback AC/DC Converter



$$V_{CM} = \frac{1}{2}|V_A + V_B| \qquad Z_{SG}: Parasitic\ capacitance\ from\ the\ output\ to\ the\ earth$$

Note: To analyze and reduce CM noise, the transformer is a critical component.

Conventional CM Noise Model of a Two-Winding Transformer

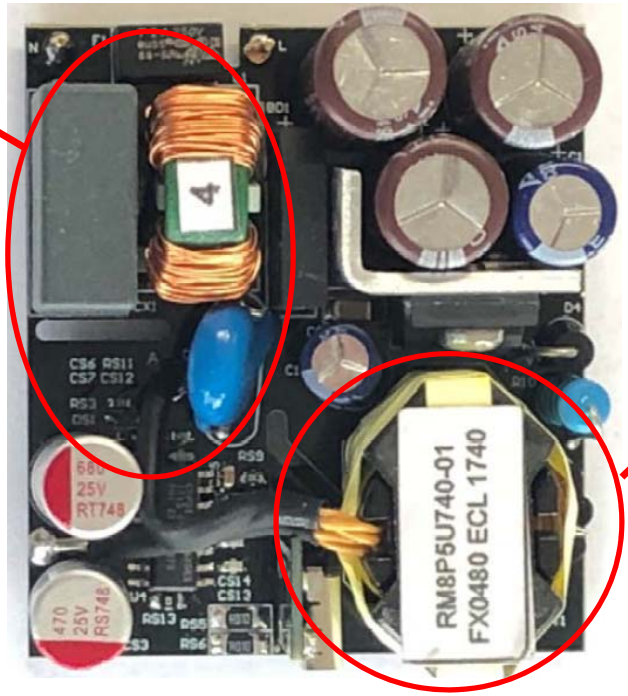


- Based on the conventional model, a two-winding transformer's parasitic capacitances can be modeled with 4 capacitors.

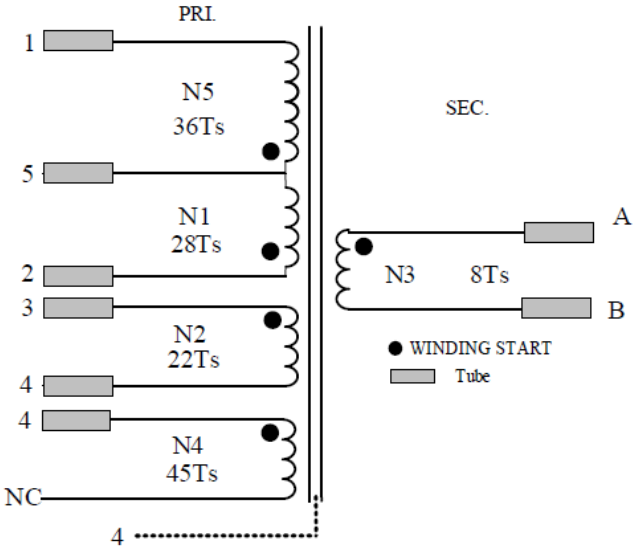
Transformer in Real Application

EVB, HFC0500+MP6908

EMI Filters

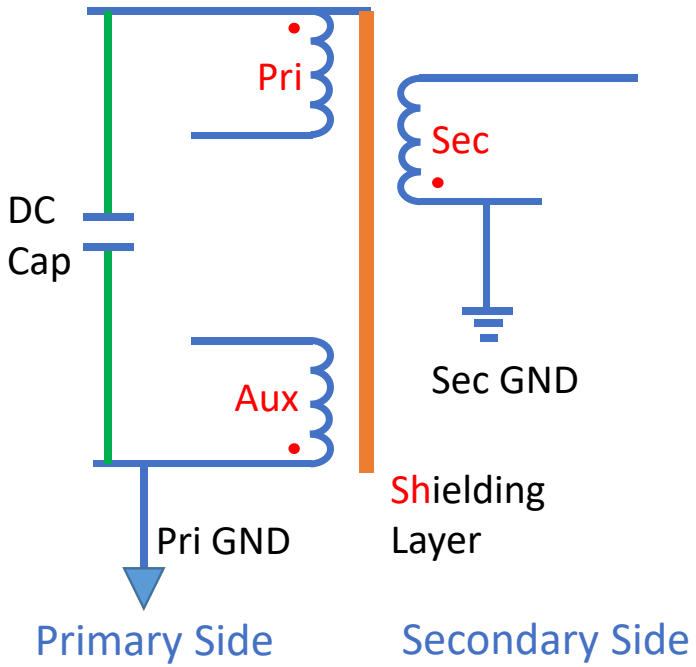


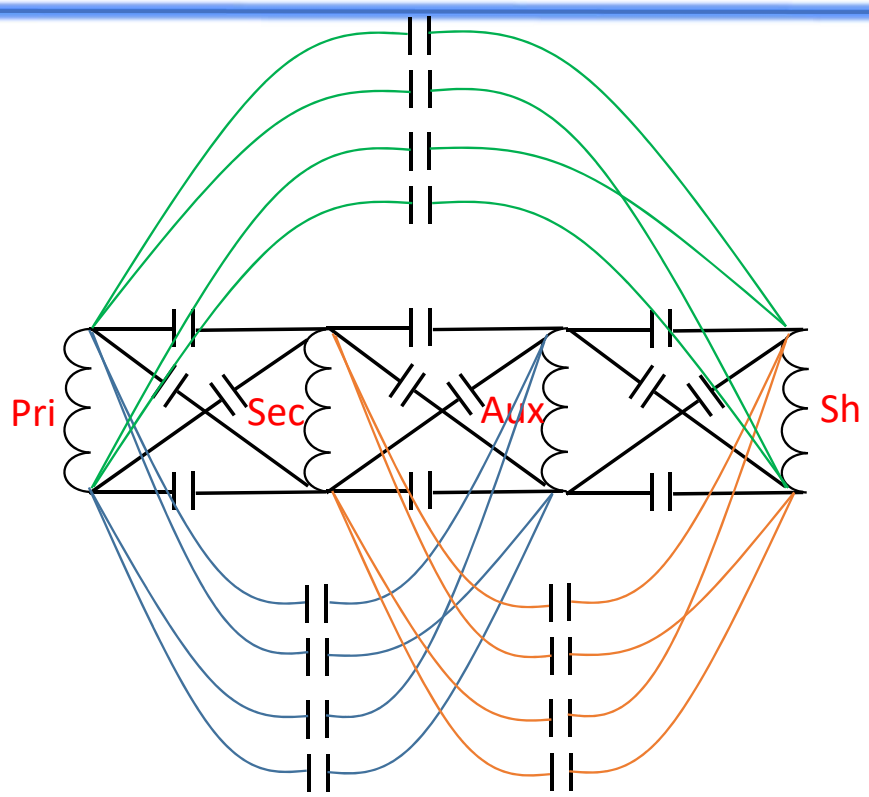
Transformer



Note: In practice, besides the primary and secondary winding, transformer has other windings such as auxiliary and cancellation winding, which results in a complex structure.

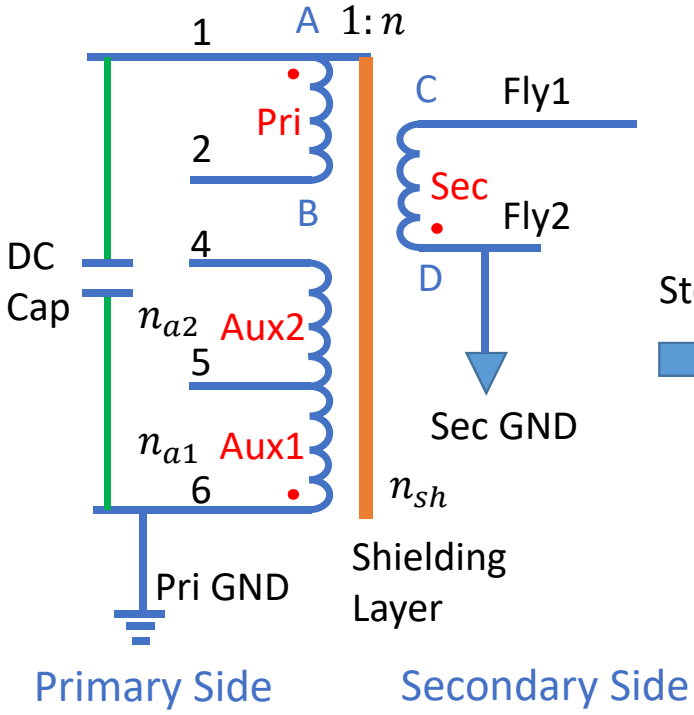
Extend Conventional Model to Multi-winding Transformers



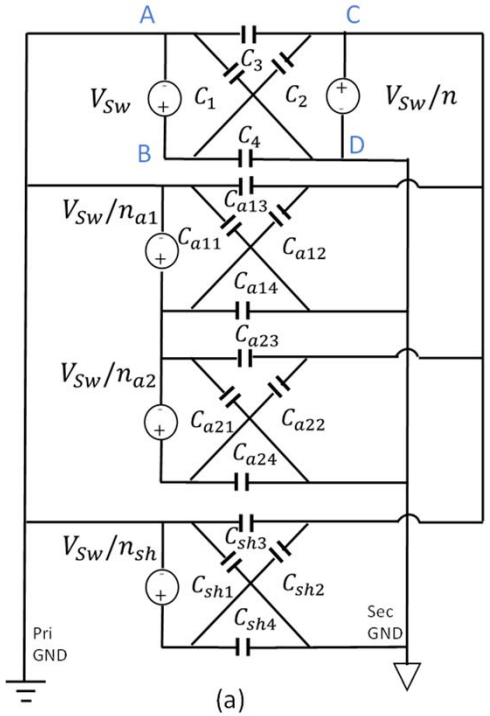


- For a multi-winding transformer, since each two winding have four parasitic capacitances, the model becomes very complicated.
- A simple and accurate transformer model needs to be proposed.

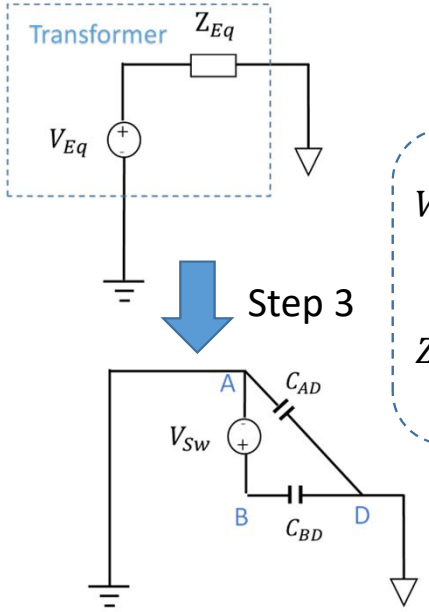
Two-Capacitor Model of Multi-Winding Transformer



Step 1



Step 2



$$V_{Eq} = \frac{C_{BD}}{C_{BD} + C_{AD}} \cdot V_{SW}$$

$$Z_{Eq} = \frac{1}{j\omega(C_{BD} + C_{AD})}$$

Step 1: Obtain a model with all winding voltages and inter-winding capacitances based on transformer circuit.
Step 2: Apply Thevenin's Theorem between Pri and Sec GND and obtain the expressions of V_{Eq} and Z_{Eq}.
Step 3: The model can be further converted to the form with primary winding voltage and two capacitors.

Apply Substitution Theory for Noise Sources

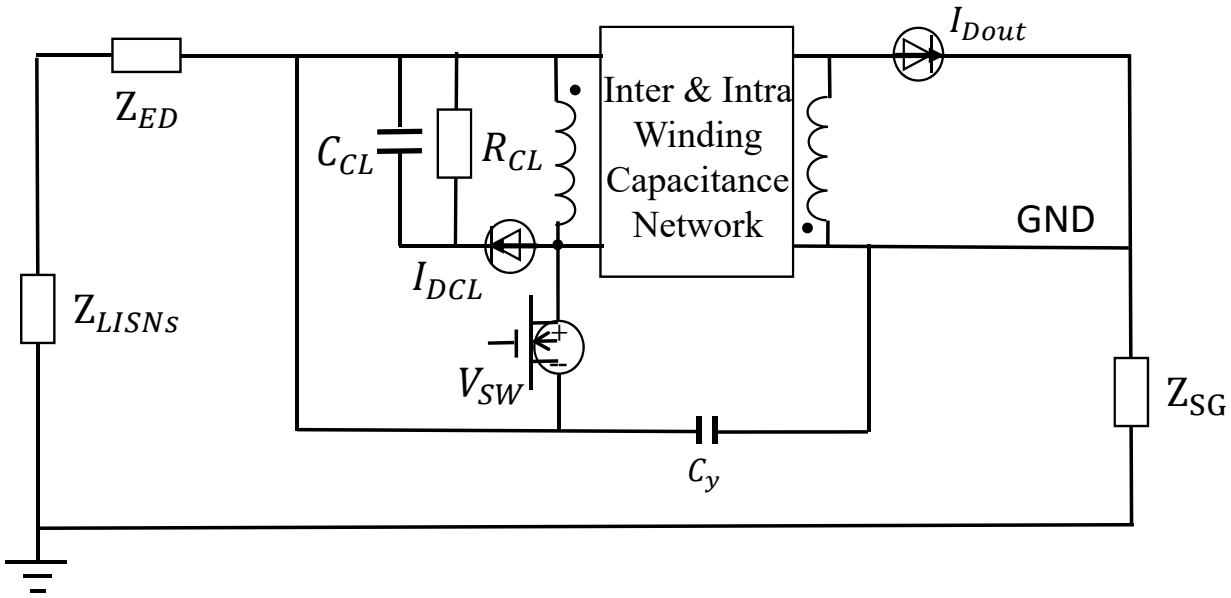
MOSFET Voltage: V_{SW}

Snubber Diode Current: I_{DCL}

Secondary Diode Current: I_{Dout}

Impedance of EMI Filter: Z_{ED}

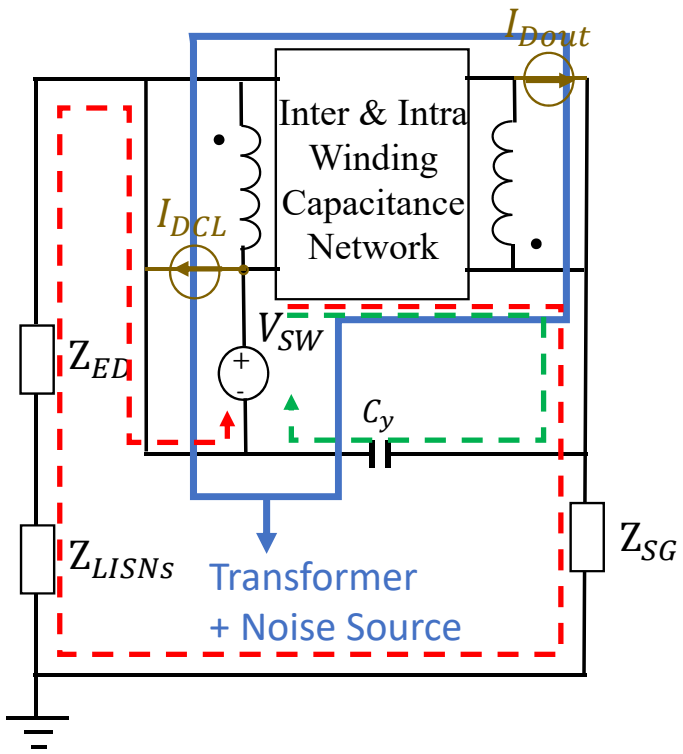
CM Impedance of LISN: $Z_{LISNs} = 25\Omega$

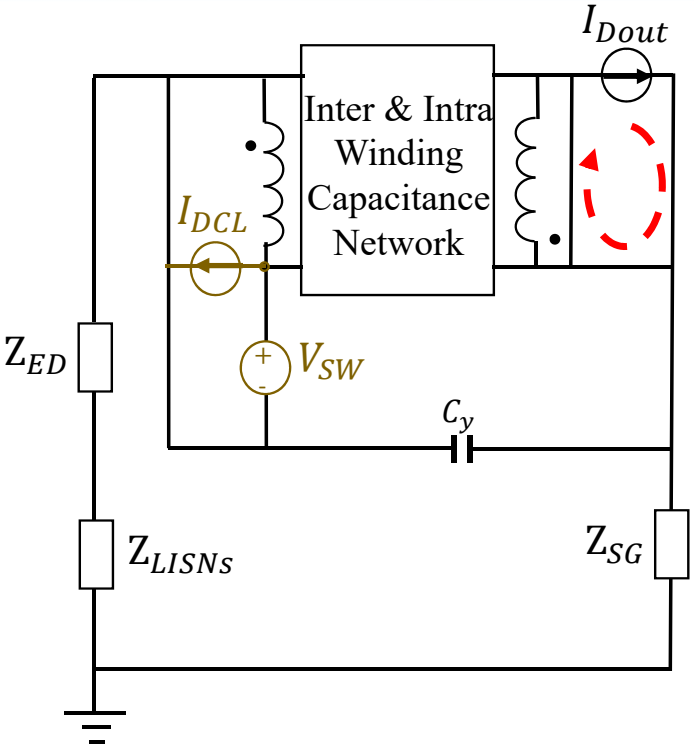


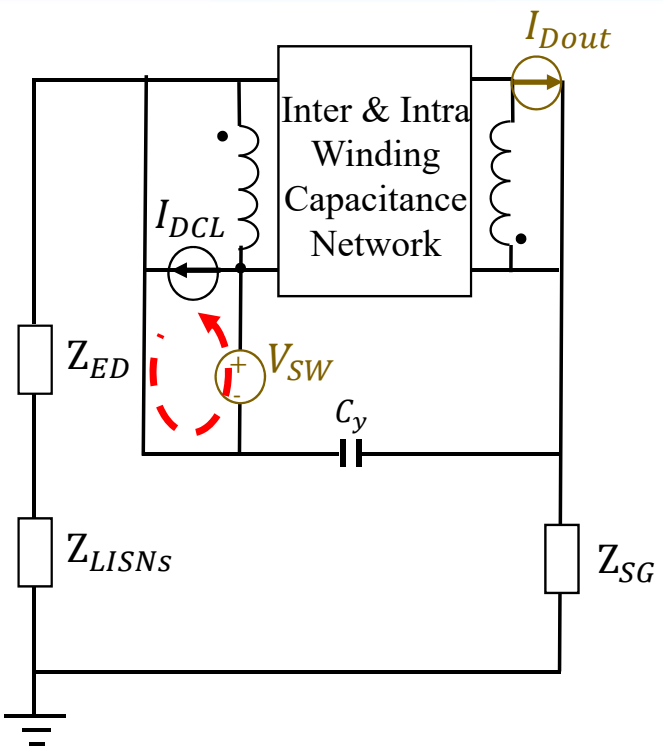
Based on substitution theorem, all the voltages and currents of a network do not change if the nonlinear switching devices in the network are replaced with voltage or current sources which have the exact same voltage or current waveforms as the original components to be replaced [1].

[1] S. Wang, P. Kong and F. C. Lee, "Common Mode Noise Reduction for Boost Converters Using General Balance Technique," in *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1410-1416, July 2007.

Apply Superposition Theory to Analyze Each Noise Source







V_{SW}: Generate CM Noise

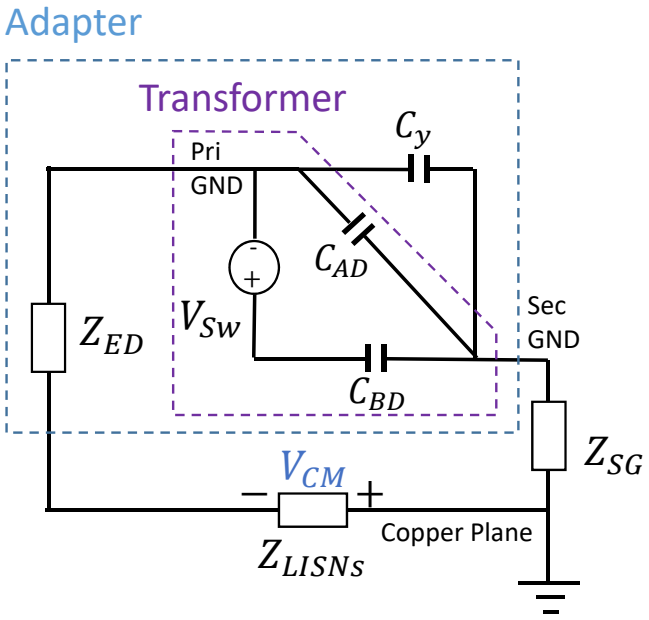
I_{Dout}: Does not generate CM Noise

I_{DCL}: Does not generate CM Noise

Final Adapter CM Noise Model

$$\frac{V_{CM}}{V_{Sw}} = \frac{Z_{LISNs}}{\frac{1}{j\omega C_T} + Z_{ED} + Z_{SG} + Z_{LISNs}} \cdot \frac{C_{BD}}{C_T}$$

$$C_T = C_y + C_{AD} + C_{BD}$$



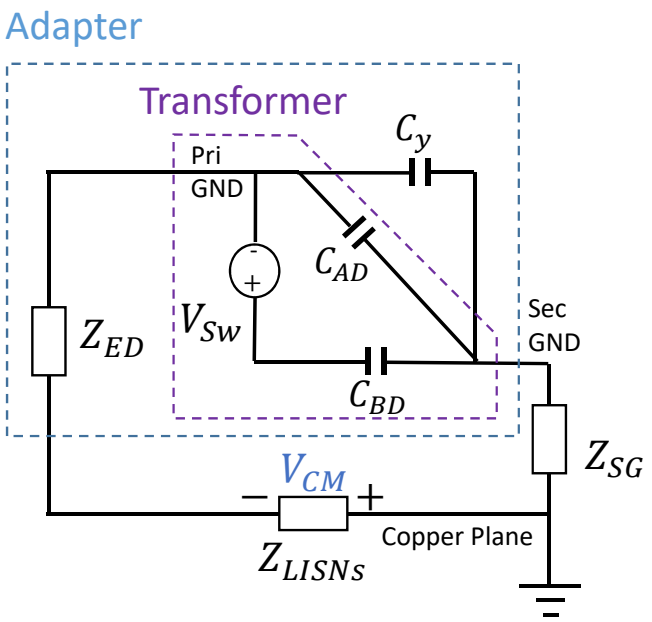
Note: If $C_{BD} = 0$, the CM noise flowing through the transformer is zero.

Z_{ED}: *Impedance of CM filter*

Discussion based on the CM transfer Gain

$$\frac{V_{CM}}{V_{Sw}} = \frac{Z_{LISNs}}{\frac{1}{j\omega C_T} + Z_{ED} + Z_{SG} + Z_{LISNs}} \cdot \frac{C_{BD}}{C_T}$$

$$C_T = C_y + C_{AD} + C_{BD}$$



- Z_{SG} and Z_{LISNs} are determined by the EUT => cannot be changed
- Increasing Z_{ED} means larger CM choke and higher cost => not desired
- Increasing C_T means larger Y-cap and higher leakage current => not desired
- Therefore, the best method is to balance the transformer to make $C_{BD} = 0$.

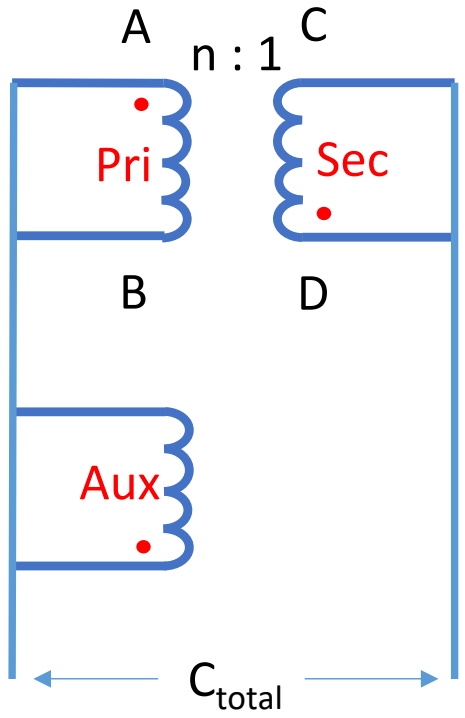
Question: How to extract the value of C_{AD} and C_{BD} in measurement?

Measurement of C_{total} of a Transformer

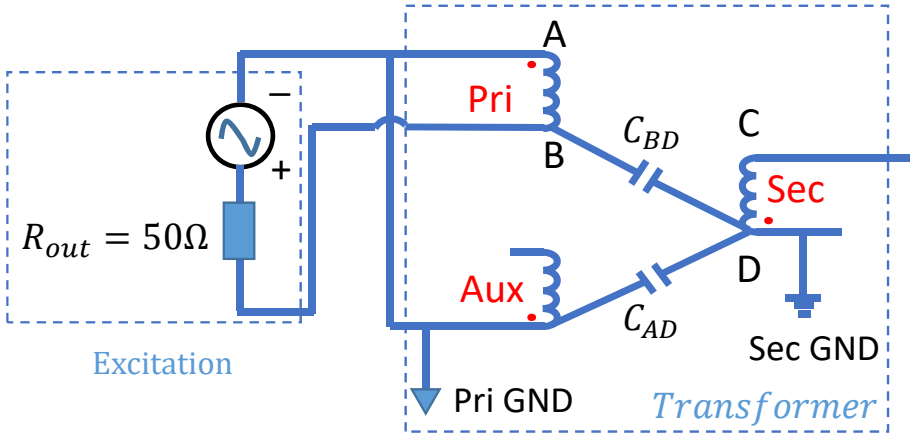
- C_{total} is the total capacitance between all the windings on the primary side and all the windings on the secondary side.

$$C_{total} = C_{BD} + C_{AD}$$

- C_{total} can be directly measured as shown in the figure.



Technique to Extract Parasitic Capacitances and Evaluate Transformer



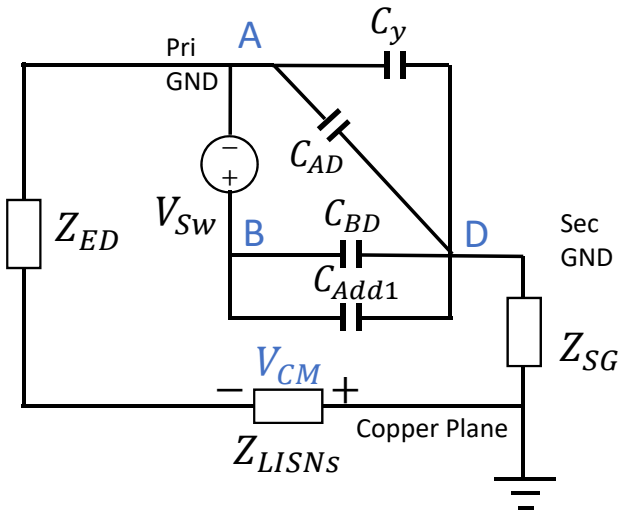
$$\frac{V_{AD}}{V_{AB}} = \frac{C_{BD}}{C_{total}}$$

Note: If V_{AD} is zero, C_{BD} is zero and there's no CM noise. Therefore, the method can be used to evaluate a transformer's CM performance.

Question: How to make $C_{BD} = 0$?

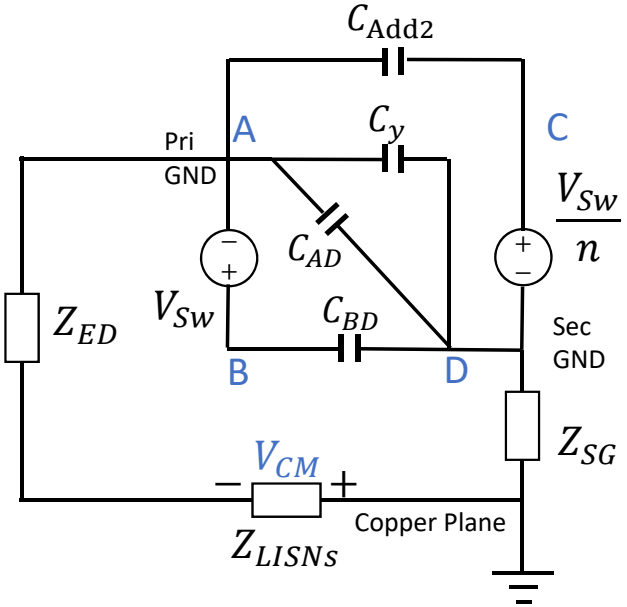
Add a Balance Capacitor

If C_{BD} is negative



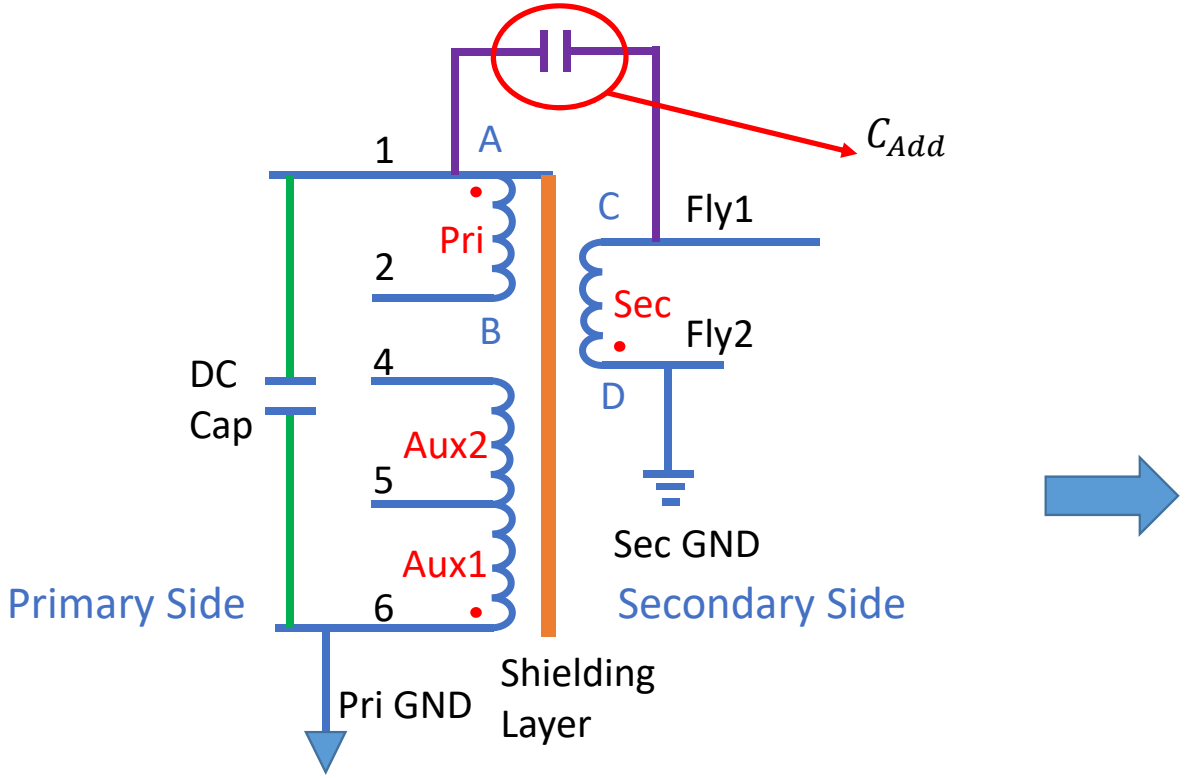
$$C_{Add1} = -C_{BD}$$

If C_{BD} is positive

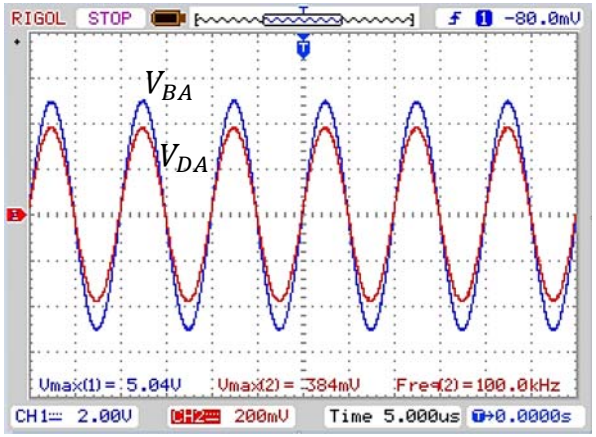


$$C_{Add2} = n \cdot C_{BD}$$

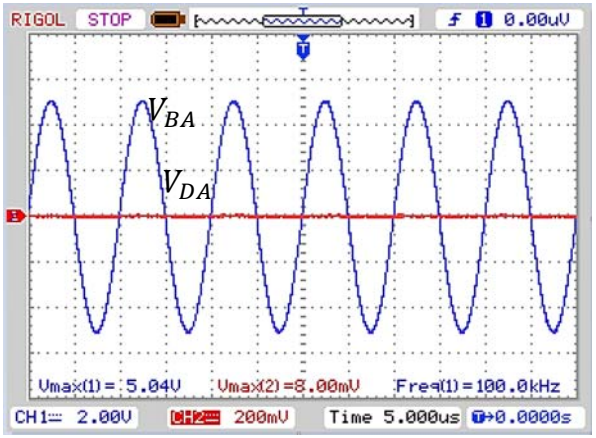
Add a Capacitor to Balance the Transformer



Original Transformer: V_{DA} and V_{BA}

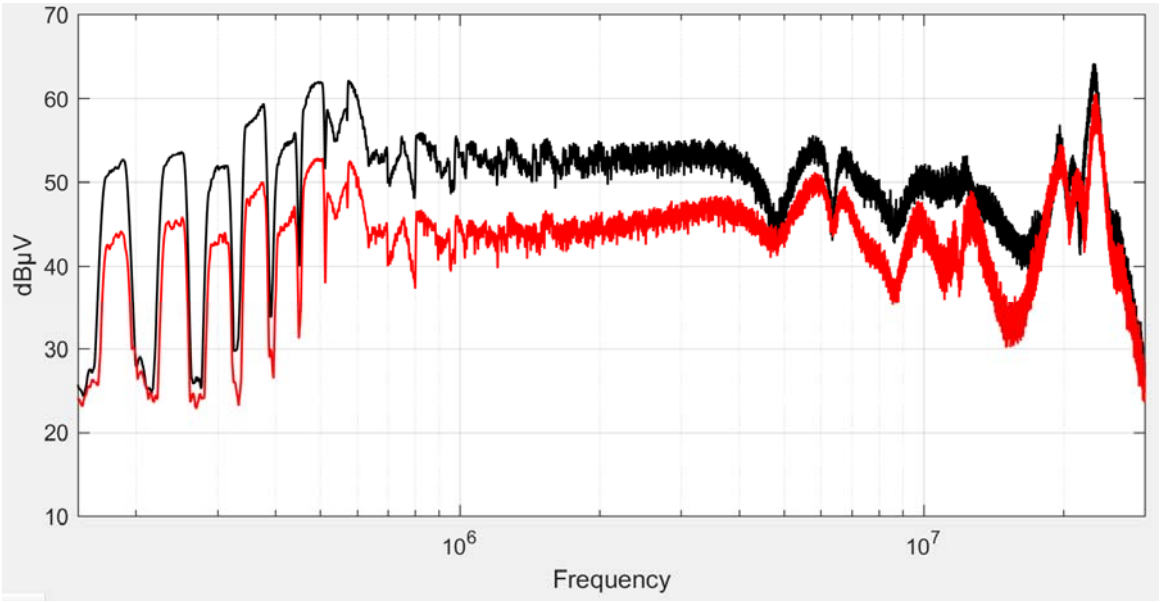


After Adding a Balance Cap: V_{DA} and V_{BA}



A balance capacitor can be applied between primary and secondary to make C_{BD} close to zero.

Measured CM Noise of the Adapter before and after Adding a Balance Capacitor



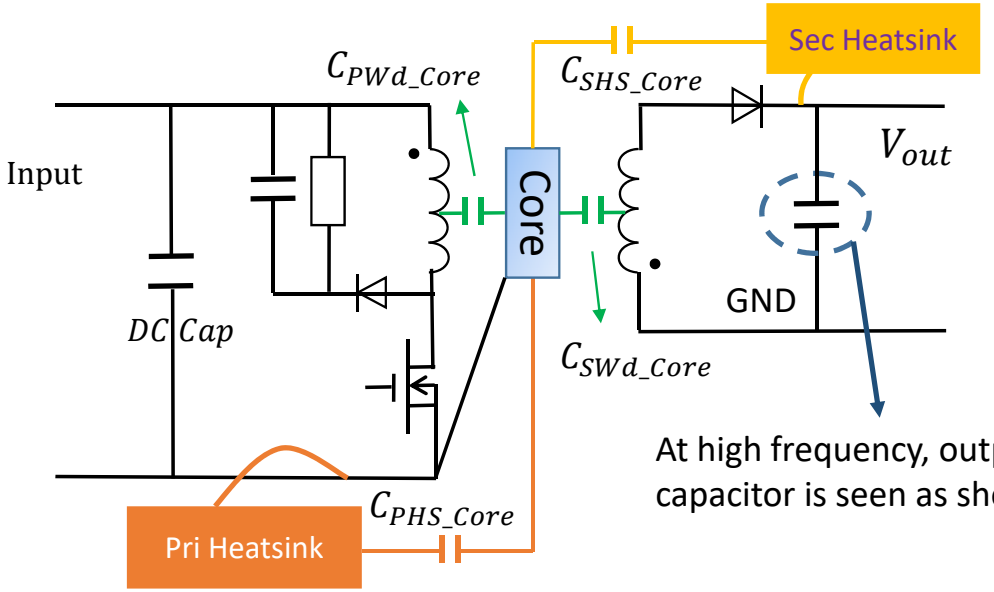
Original Transformer

After Adding a balance capacitor

The measured CM noise has a reduction of up to 10dB from 150kHz to 15MHz after adding a balance capacitor.

Question: The effort of balance capacitor is not very significant. Is there other reason for CM noise?

Shielding Transformer Core to Eliminate Capacitive Coupling due to the Core

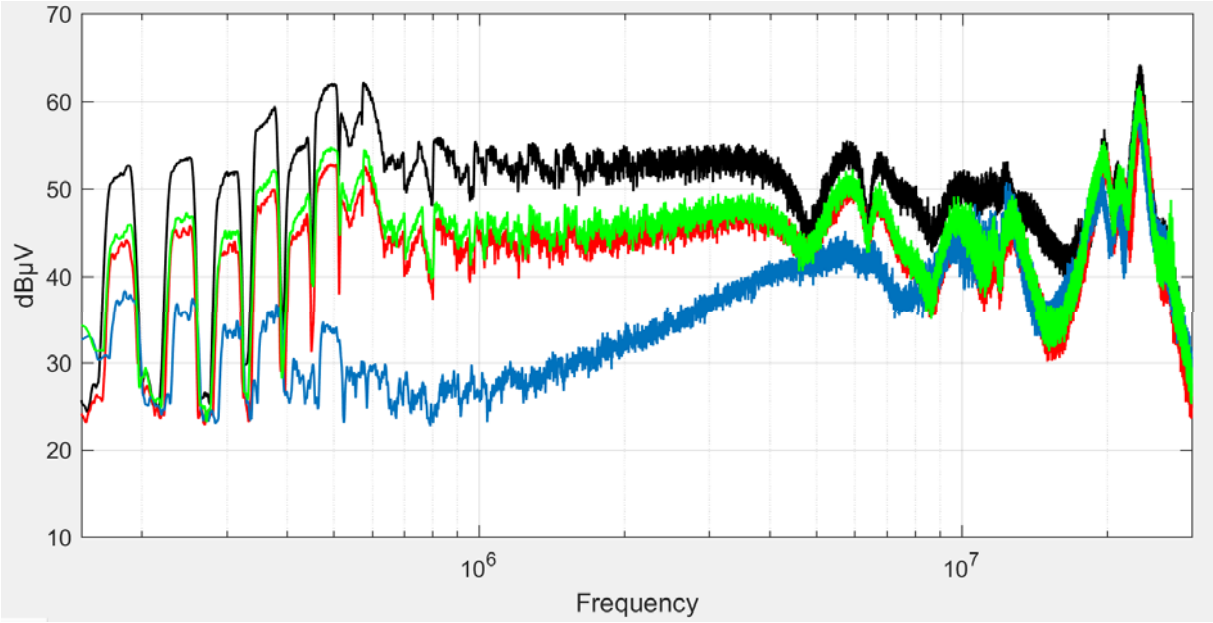


Step 1: Apply a copper shield on the core and connect it to Pri GND.

Step 2: Locate the secondary winding layers not adjacent to the core.

- Since the core is connected to Pri GND, C_{PHS_Core} is shorted and C_{SHS_Core} works as a Y-capacitor, which means the noise current flowing through C_{PWd_Core} to the core will not generate CM noise.
- The noise current flowing from C_{SWd_Core} to the core still generates CM noise. In order to reduce it, the secondary winding layers can be relocated not close to the core.

Experiment Results



Original Transformer

Balanced Transformer

Balanced and shielded Transformer with floating copper shell

Balanced and Shielded Transformer with copper shell connected to Primary GND

Conclusions:

1. A floating copper shield cannot shield capacitive coupling. Therefore the CM noise is not reduced.
2. By connecting the copper shield to Pri GND, the CM noise is reduced significantly by up to 30dB at low frequencies.

Question: Applying a balance capacitor increases the cost and may cause safety issue. How to achieve balance in transformer design?

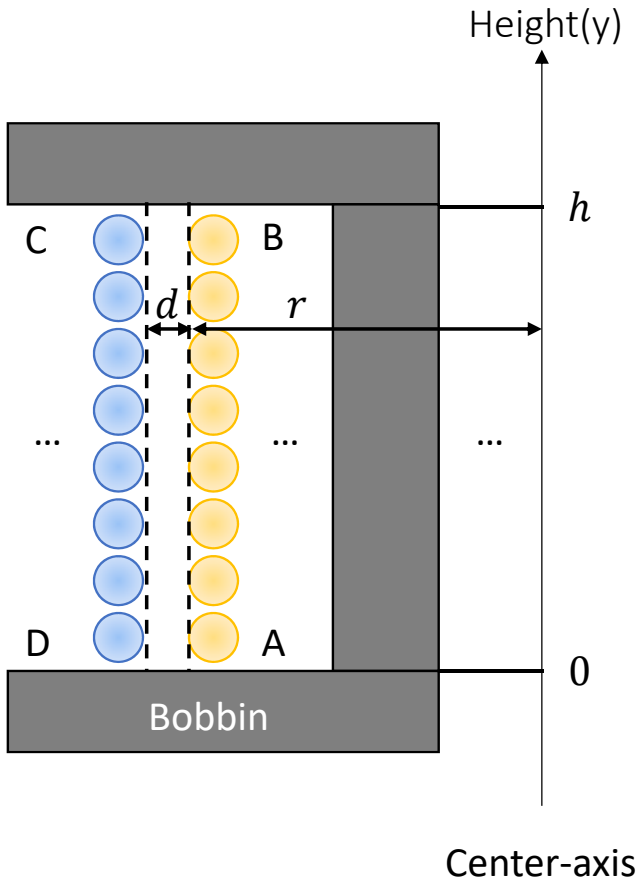
Parasitic Capacitance in Transformer

- Assume the wire is tightly wound. The capacitance can be modeled as parallel plate capacitor.

$$C_{ps} \approx \frac{2\pi\varepsilon h}{\ln(r+d)-\ln r} \approx \frac{2\pi\varepsilon h r}{d}$$

C_{ps}: Total capacitance between two adjacent layers

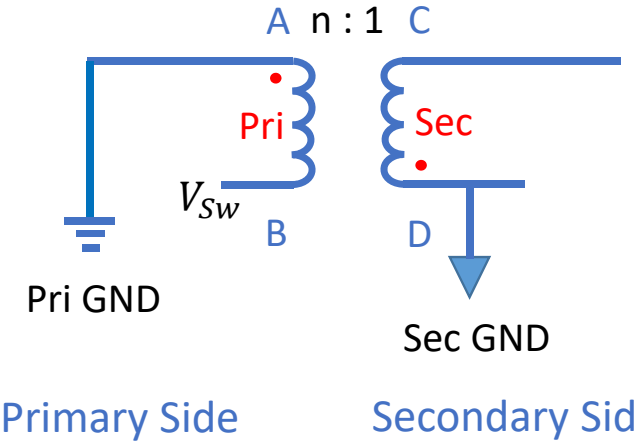
Note: C_{ps} is only related to the geometry of the layers.



CM Current between Adjacent Layers

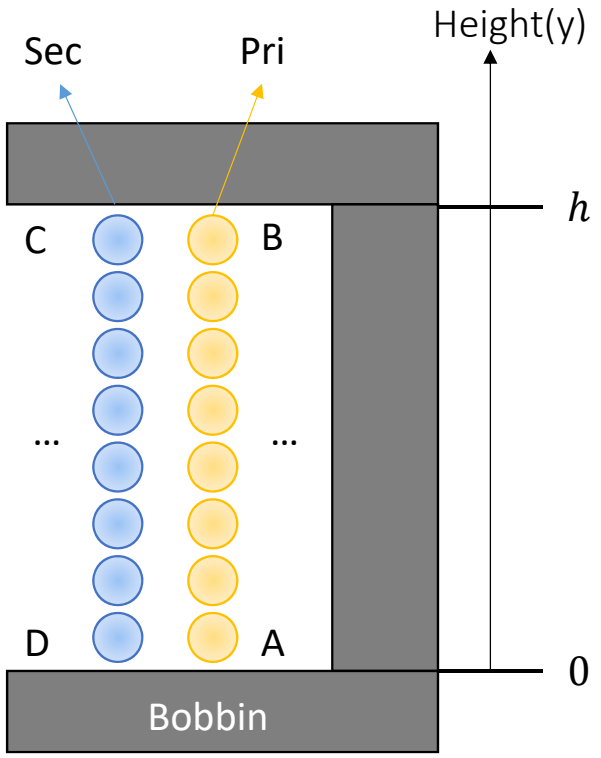
$$i_{CM_{pri-sec}} = \int_0^h \frac{C_{ps}}{h} \cdot \left(\frac{dV_{pri}(y)}{dt} - \frac{dV_{sec}(y)}{dt} \right) dy$$

Assume the parasitic capacitance is evenly distributed between adjacent layers.



Assume the voltage is evenly distributed along the winding.

$$\begin{cases} \frac{dV_{pri}(y)}{dt} = \frac{dV_{Sw}}{dt}\frac{y}{h} \\ \frac{dV_{sec}(y)}{dt} = \frac{dV_{Sw}}{dt}\frac{y}{nh} \end{cases}$$

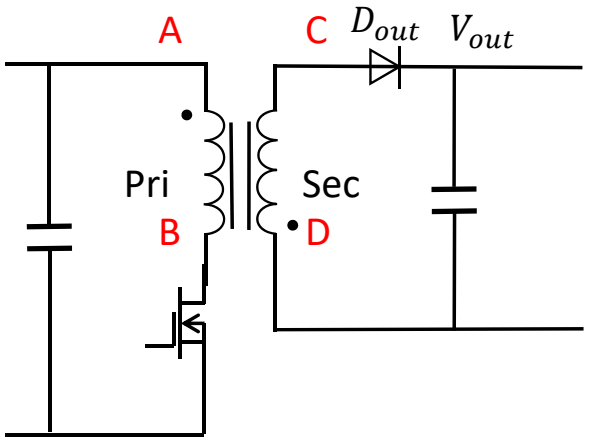


$$i_{CM_{pri-sec}} = C_{ps}\left(\frac{1}{2}\frac{dV_{Sw}}{dt} - \frac{1}{2n}\frac{dV_{Sw}}{dt}\right) = C_{ps}\left(\frac{n-1}{2n}\right)\frac{dV_{Sw}}{dt}$$

Note: The CM current between adjacent layers is proportional to the difference of the average of the dV/dt at two terminals.

Secondary Diode/FET Location

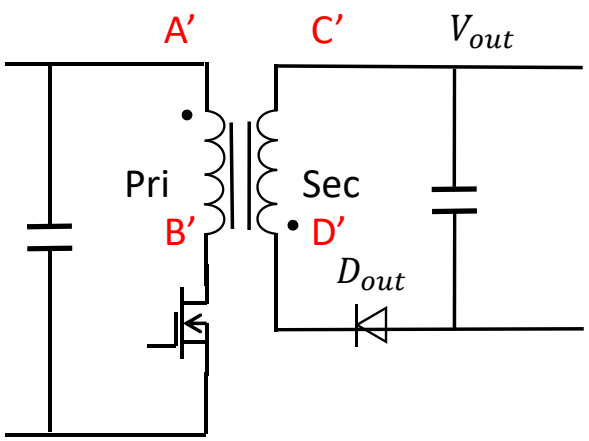
Secondary high side diode/FET

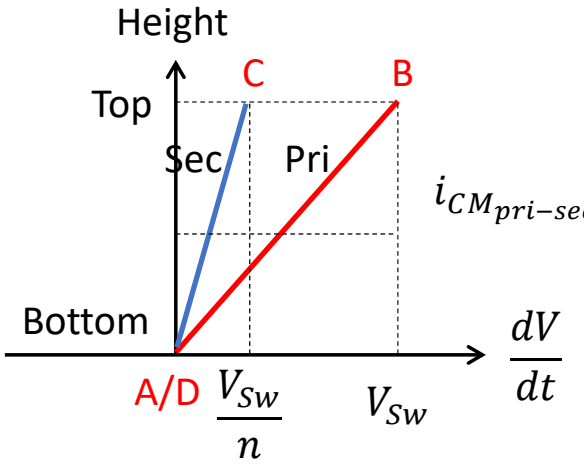


MP6908: low-drop diode emulator controller IC

Support both topology with an external MOSFET.

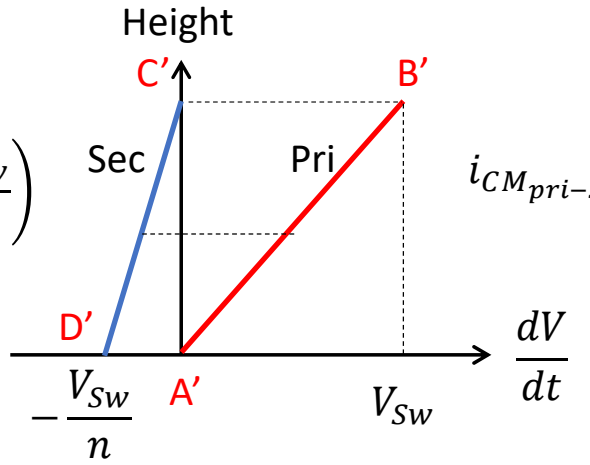
Secondary low side diode/FET





$$i_{CM_{pri-sec}} = C_{ps}\left(\frac{1}{2}\frac{dV_{Sw}}{dt} - \frac{1}{2n}\frac{dV_{Sw}}{dt}\right)$$

Lower CM noise



$$i_{CM_{pri-sec'}} = C_{ps}\left(\frac{1}{2}\frac{dV_{Sw}}{dt} + \frac{1}{2n}\frac{dV_{Sw}}{dt}\right)$$

Higher CM noise

A Transformer Design Consideration

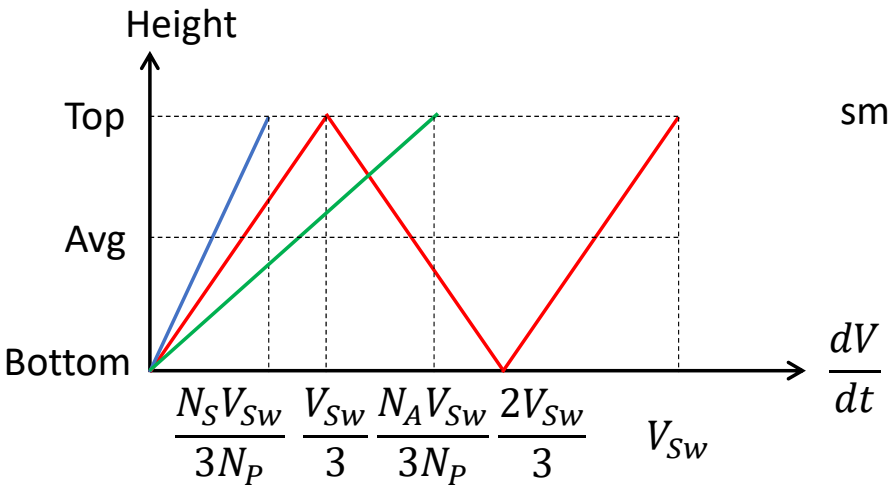
The winding terminal connections need to be designed to achieve the smallest CM noise.
The adjacent layers between the primary and secondary sides should have smallest dV/dt difference.

Example: Design an interleaved transformer with low leakage inductance and low CM noise

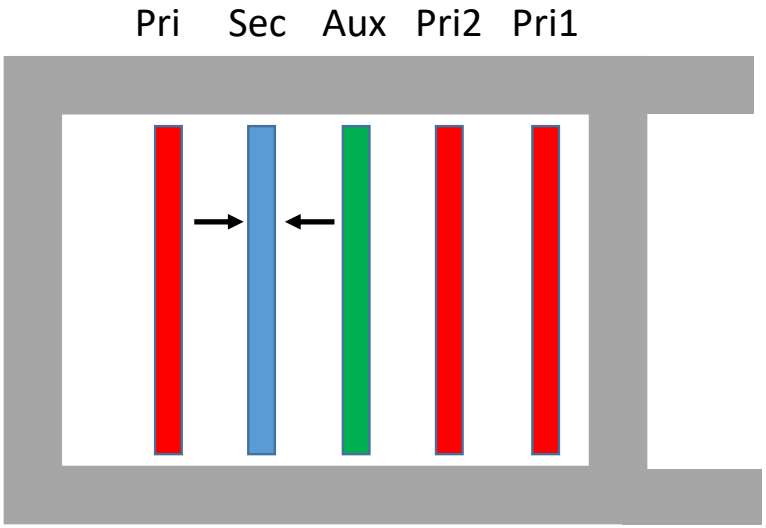
Primary winding: 3 layers, $3 \times N_P$ turns

Secondary winding: 1 layer, N_S turns

Auxiliary winding: 1 layer, N_A turns



smallest dV/dt difference



Shielding and Cancellation Winding

- Shielding layer is typically a copper tape that placed between the primary and secondary winding with one terminal grounded. It can be seen as a 1-turn cancellation winding.
- Cancellation winding is a winding with one terminal grounded and the other terminal floating, which generates a CM current to the adjacent layer to cancel the CM noise.

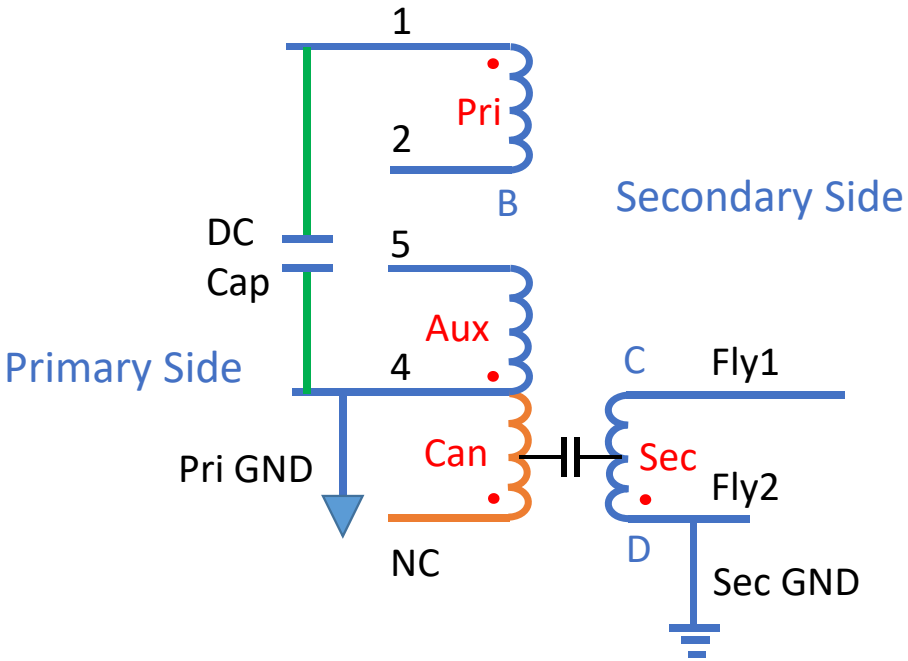
Advantage of cancellation winding:

- The balance capability of the cancellation winding is better than conventional shielding layers.
- The cancellation winding helps to reduce both the size and cost of the transformer. And it is suited for automatic manufacturing.

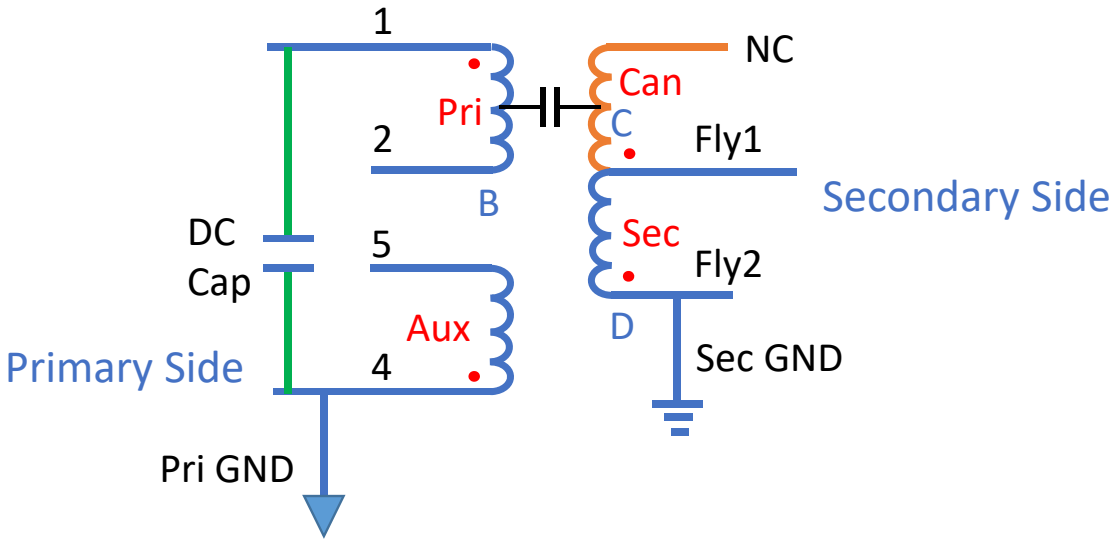
Cancellation Winding Connection and Location

Example: when C_{BD} is positive

Primary Can, adjacent to Sec

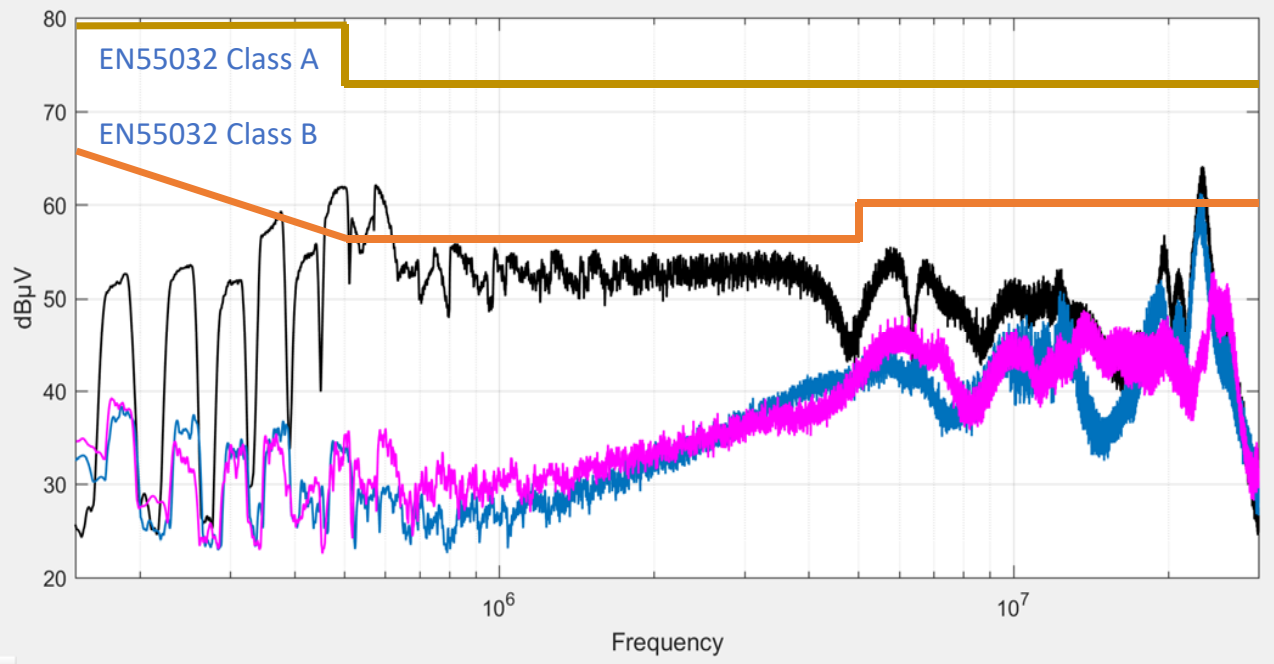


Secondary Can, adjacent to Pri



Note: It is always useful to check the CM performance to verify the effort of the cancellation winding. The cancellation turn number can also be estimated based on the two-capacitor model.

Final Experiment Results



Original Transformer

Original Transformer with balance cap and copper shell

Redesigned transformer without balance capacitor

Note: CM inductor was removed in experiments.

Original Adapter: CM noise exceeds EN55032 class B as its CM filter was removed.
Adding a balance cap and a core shielding: CM noise is reduced by up to 30dB at low frequencies. However, at 22MHz, the CM noise is still higher than the standard.
With the redesigned transformer: CM noise meets the EMI standard in whole frequency range with 8-30dB margin.

Summary

- 1. A two-capacitor CM noise model is introduced for a multi-winding transformer.
- 2. A technique to measure the value of two capacitors without in-circuit test is proposed. The technique is also applied to evaluate CM performance of a transformer.
- 3. Balance capacitor and transformer core shielding are applied to achieve significant CM noise reduction.
- 4. The transformer winding cancellation technique is introduced to reduce the CM noise with proper transformer design.

Thank you for listening !

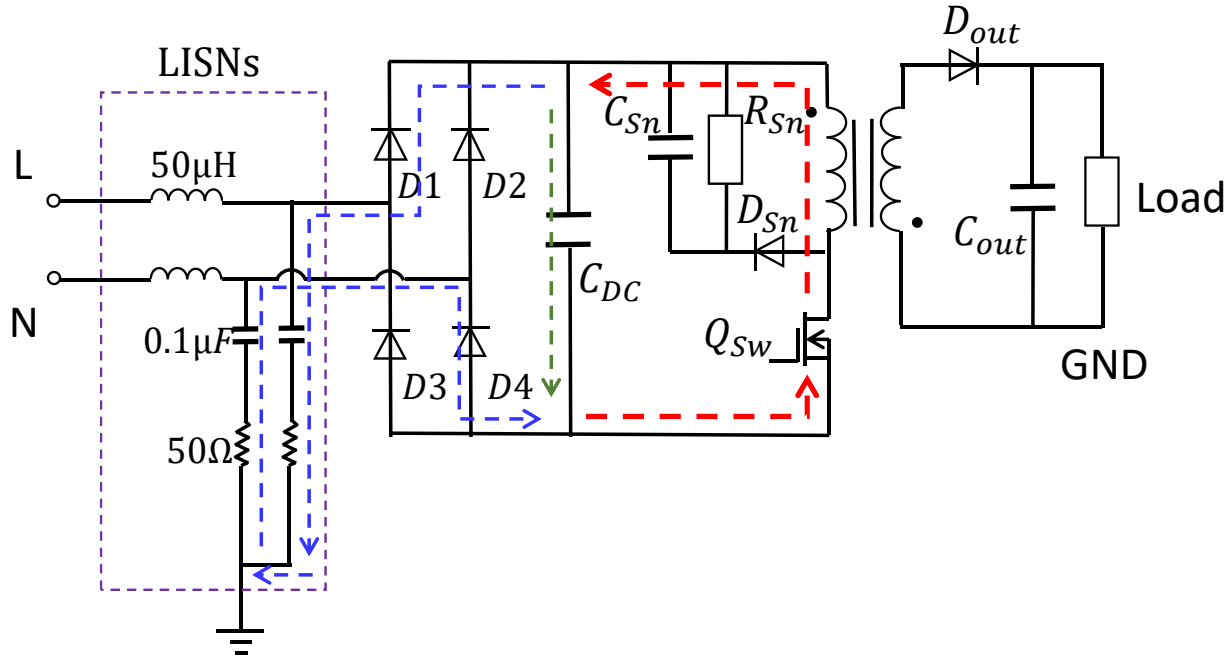
For more information:

[1] Y. Li, H. Zhang, S. Wang, H. Sheng, C. P. Chng and S. Lakshmikanthan, "Investigating Switching Transformers for Common Mode EMI Reduction to Remove Common Mode EMI Filters and Y Capacitors in Flyback Converters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 4, pp. 2287-2301, Dec. 2018.

[2] H. Zhang, S. Wang, Y. Li, Q. Wang and D. Fu, "Two-Capacitor Transformer Winding Capacitance Models for Common-Mode EMI Noise Analysis in Isolated DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8458-8469, Nov. 2017.

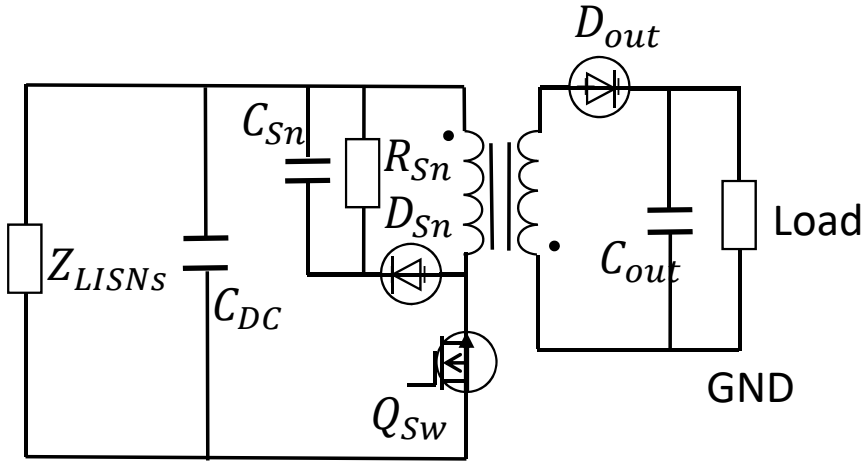
[3] Y. Li, S. Wang, H. Sheng and S. Lakshmikanthan, "Investigate and Reduce Capacitive Couplings in a Flyback Adapter With a DC-Bus Filter to Reduce EMI," in *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 6963-6973, Jul. 2020.

DM Noise Path for a Flyback Adapter



Note: For DM noise analysis, LISNs' impedance can be regarded as a 100-Ω resistor.

DM Noise Modeling with Substitution Theory

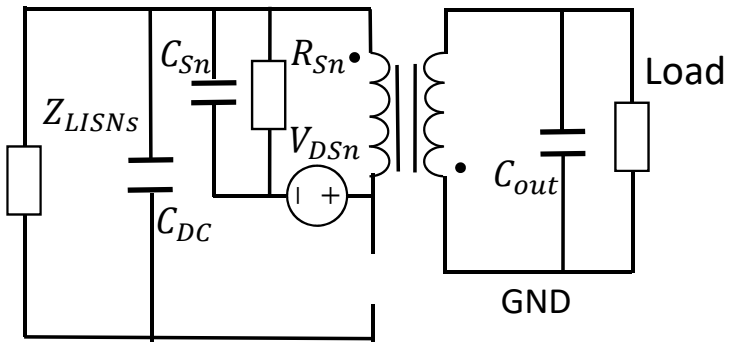


Z_{LISNs}: LISNs' Impedance: 100-Ω resistor

Note: Based on substitution theorem, all the voltages and currents of a network do not change if the nonlinear switching devices in the network are replaced with voltage or current sources which have the exact same voltage or current waveforms as the original components to be replaced.

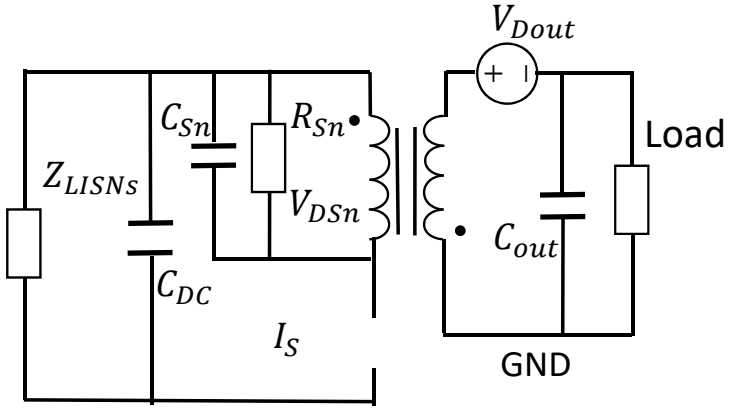
Apply Superposition Theory to Analyze the Effects of Noise Sources

Influence of V_{DSn}



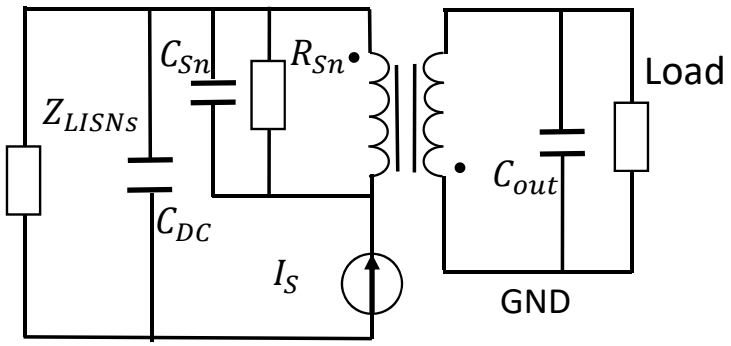
V_{DSn} will not generate DM noise

Influence of V_{Dout}



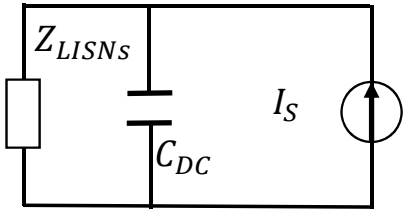
V_{Dout} will not generate DM noise

Influence of I_S



I_S will generate DM noise

Final DM Model



All the components series with the current source I_S can be shorted.

$$V_{Eq} = \frac{C_{BD}}{C_{BD} + C_{AD}} \cdot V_{SW} = \frac{C_{BD}}{C_{Total}} \cdot V_{SW}$$

$$Z_{Eq} = \frac{1}{j\omega\left(C_{BD} + C_{AD}\right)} = \frac{1}{j\omega C_{Total}}$$

$$C_{BD} = \left[\left(1 - \frac{1}{n}\right) \cdot C_2 + C_4 - \frac{1}{n} \cdot C_3\right] + \left[\left(\frac{1}{n_{a1}} - \frac{1}{n}\right) \cdot C_{a12} + \frac{1}{n_{a1}} \cdot C_{a14} - \frac{1}{n} \cdot C_{a13}\right]$$

$$+ \left[\frac{1}{n_{a1}} \cdot C_{a21} + \left(\frac{1}{n_{a1}} + \frac{1}{n_{a2}} - \frac{1}{n}\right) \cdot C_{a22} + \left(\frac{1}{n_{a1}} - \frac{1}{n}\right) \cdot C_{a23} + \left(\frac{1}{n_{a1}} + \frac{1}{n_{a2}}\right) \cdot C_{a24}\right]$$

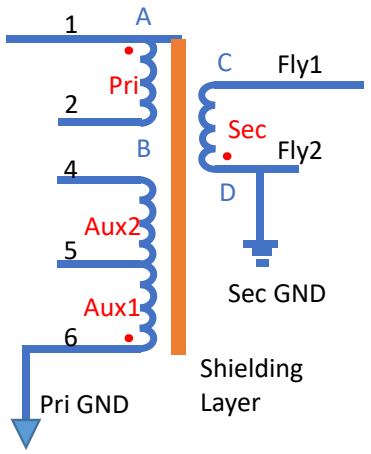
$$+ \left[\left(\frac{1}{n_{sh}} - \frac{1}{n}\right) \cdot C_{sh2} + \frac{1}{n_{sh}} \cdot C_{sh4} - \frac{1}{n} \cdot C_{sh3}\right]$$

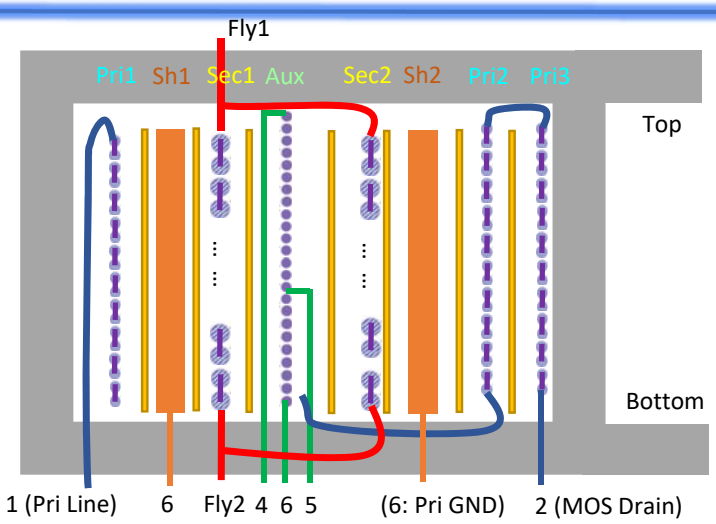
$$C_{AD} = C_{Total} - C_{BD}$$

Redesign Transformer to Achieve CM Balance and Small Leakage Inductance

- Step 1: Windings interleaving technique is applied to reduce leakage inductance.
- Step 2: The winding terminal connections are designed to achieve the smallest CM noise. The adjacent layers between the primary and secondary sides should have smallest voltage difference.
- Step 3: A cancellation winding is added to balance the CM noise.

Conventional Transformer





Redesigned Transformer