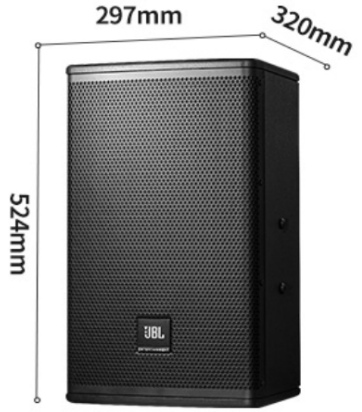
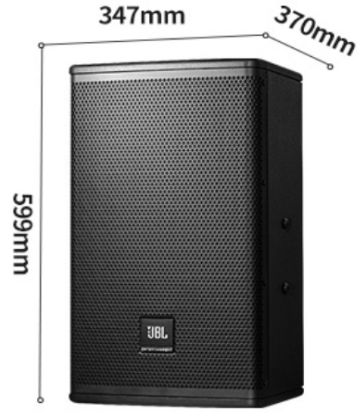
MPS Professional Audio power solution

HR1210 Digital PFC&LLC Controller+Flyback HF500-X

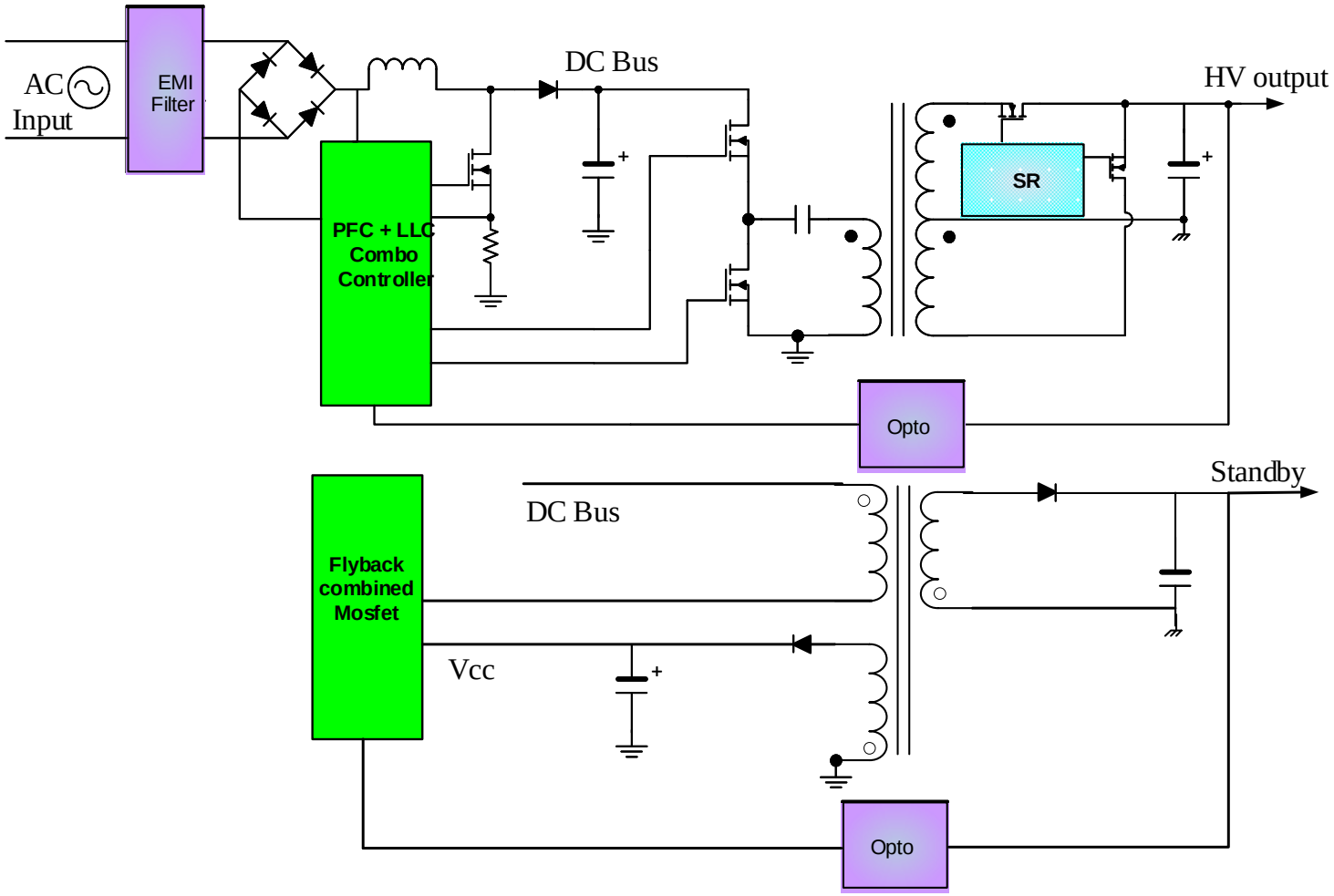
2020.12.28

Professional audio power

产品展示:		
系统类型	10英寸，两路，低音反射	12英寸，两路，低音反射
频响（-10dB）	50 Hz-20 kHz	47 Hz-20 kHz
频率响应（±3 dB）	85 Hz-18 kHz	80 Hz-18 kHz
灵敏度	94分贝	95分贝
标称阻抗	8欧姆	8欧姆
大声压级（1m）	119 dB（峰值125 dB）	121 dB（峰值127 dB）
额定功率	（连续/程序/峰值） 300瓦/ 600瓦/ 1200瓦	（连续/程序/峰值） 400瓦/ 800瓦/ 1600瓦

Professional audio power

Block diagram:



Powe spec:

- Peak power up to 1kW,standby within 20W
- Load transient speed is fast with ms level and frequently
- HV output have large cap,usually >1500uF

AC-DC solution need:

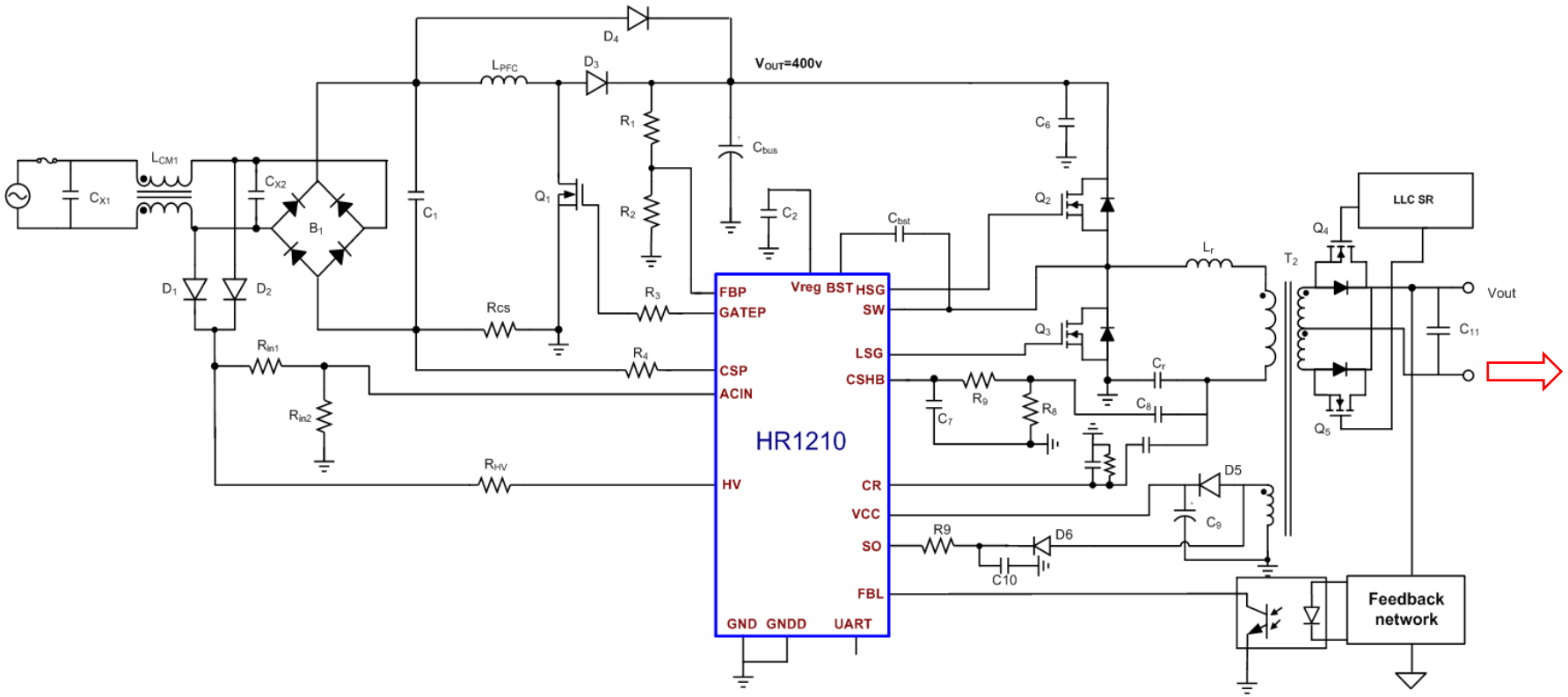
- High power density and efficiency
- High reliability but easy to design
- Full protection feature

MPS total solution:

- HR1210：PFC+LLC combin controller
- HF500-X：Flyback combined Mosfet

HR1210 Typical Application

CCM/DCM PFC + Current Mode LLC



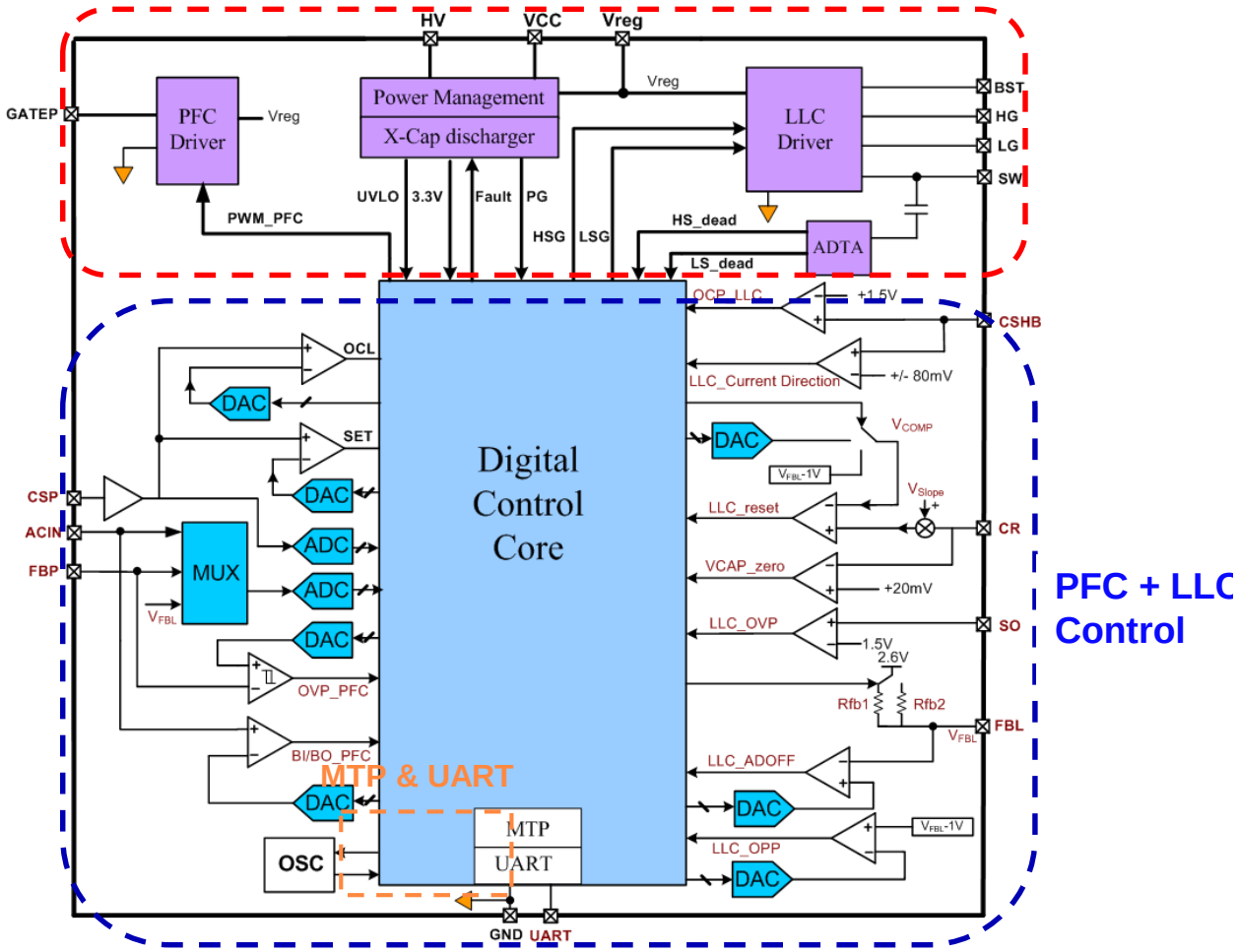
- •SOIC-20 & TSSOP-20
- •Full Digital Solution
- •CCM/DCM of PFC
- • Current/Voltage Mode LLC

HR1210

- • Ultra-low no load power loss (Pin<100mW @ No Load)
- • Improved and accurate burst mode control (η>80%@Pout=8W)
- • UART Interface
- • GUI for design (Both PFC & LLC)

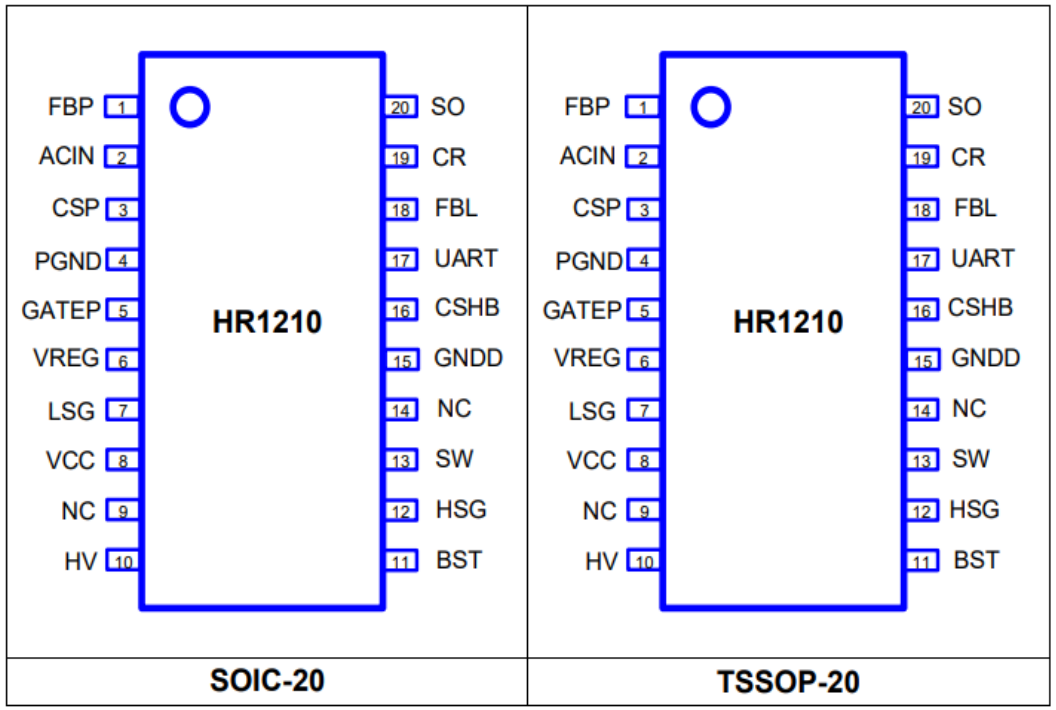
HR1210 Typical Application

Driver, Power Manager, X-cap discharge, ADTA



PFC + LLC Control

PACKAGE REFERENCE



HR1210 Key Features

System:

- **Pin<100mW@Pout=0mW**
- **High voltage current source for start up & Smart X-cap discharger**
- **UART Interface & GUI for parameters program**

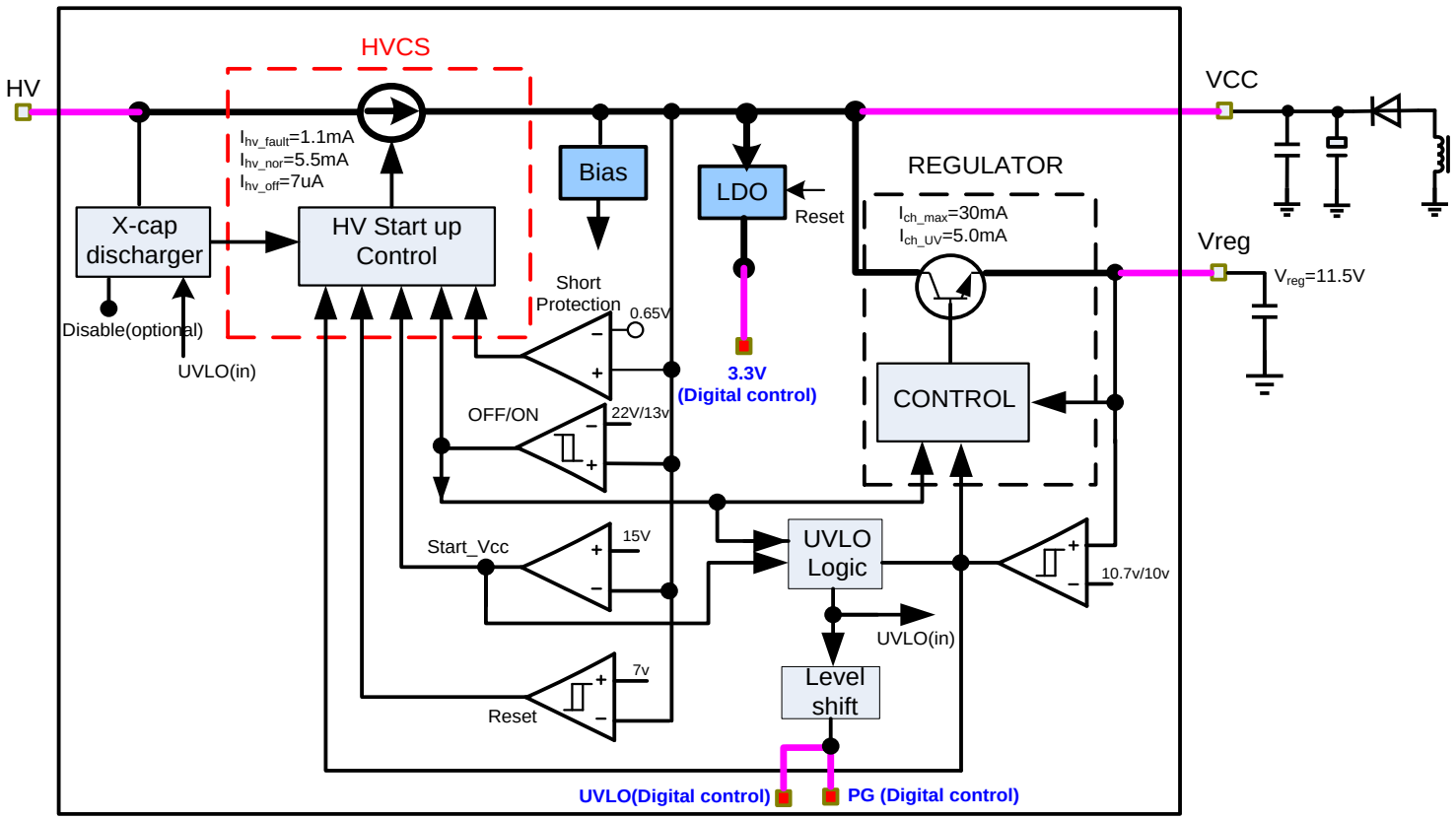
PFC:

- **CCM/DCM operation of digital PFC (Max. Switching up to 250KHz)**
- **High PF due to cap current compensation (>0.95@ 20% load)**
- **Programmable frequency Jitter to improve EMI.**
- **Digital PI for control loop**
- **Programmable AC BI/BO, OVP, OCL, OLP**

LLC:

- Current Mode / Voltage Mode Control
- Adaptive dead time adjustment (230ns~1us)
- Anti capacitive mode operation of LLC
- Programmable BI/BO, SCP, OPP
- Skip mode & frequency controlled Burst mode for better light load efficiency & low audible noise

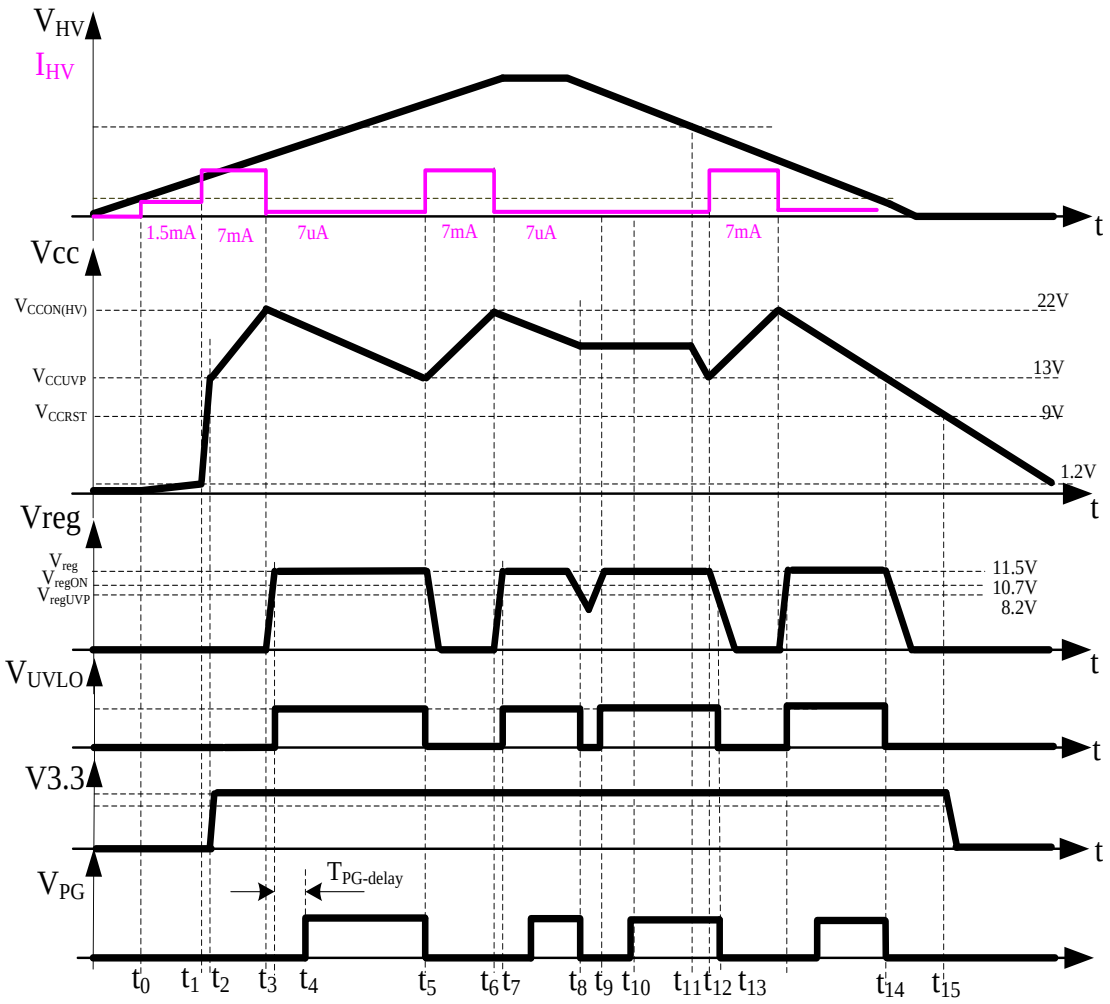
HR1210-HVCS and X-cap discharge



- A high voltage current source (HVCS) internal HV pin is used to power up VCC
- An internal 3.3V LDO is used to power digital control
- An internal 11V regulator is used to power the gate driver (Vreg)
- UVLO and PG logic signal is generated for the digital control set-up
- X-cap Discharge is detected on HV pin

HR1210-HVCS and X-cap discharge

Power Supply:



Normal Mode: V_{HV} is sinusoid

t0: V_{HV-PK} >35v, HVCS start charge Vcc.

t0~t1: 3.3v (digital control) power set-up

t3: V_{cc} >22v, HVCS turn off, Vreg LDO (driver supply) works

t3: UVLO is high, digital control stand-by to operate

t4: PG (power good) is high, digital control starts soft-start

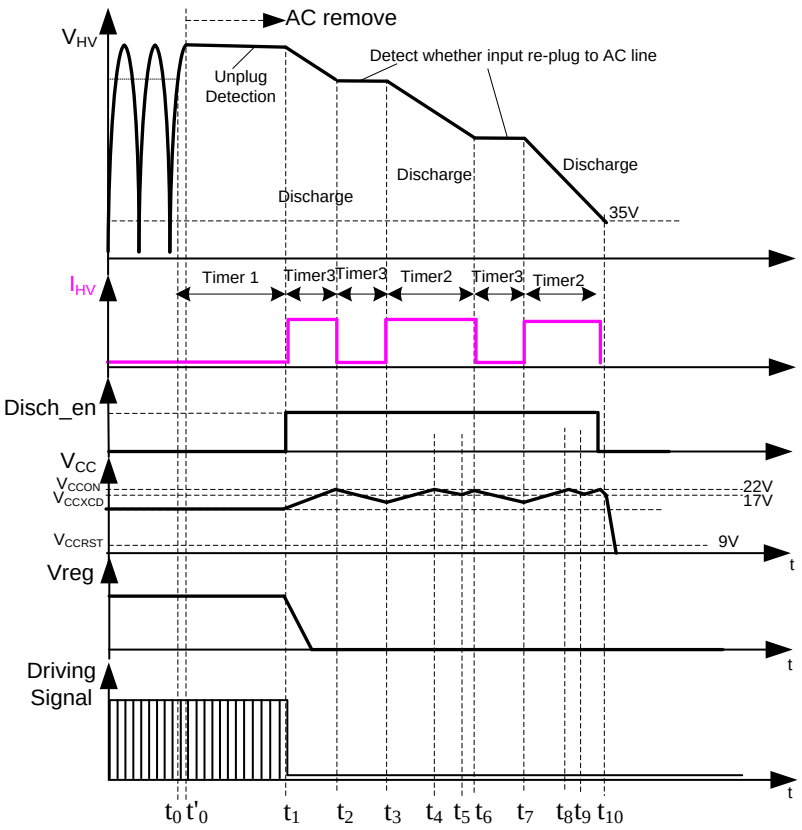
t4~t5: Capacitor value on Vcc determine this period.

t5-t8: Digital control stop work when Vcc<13v or Vreg<8.9v

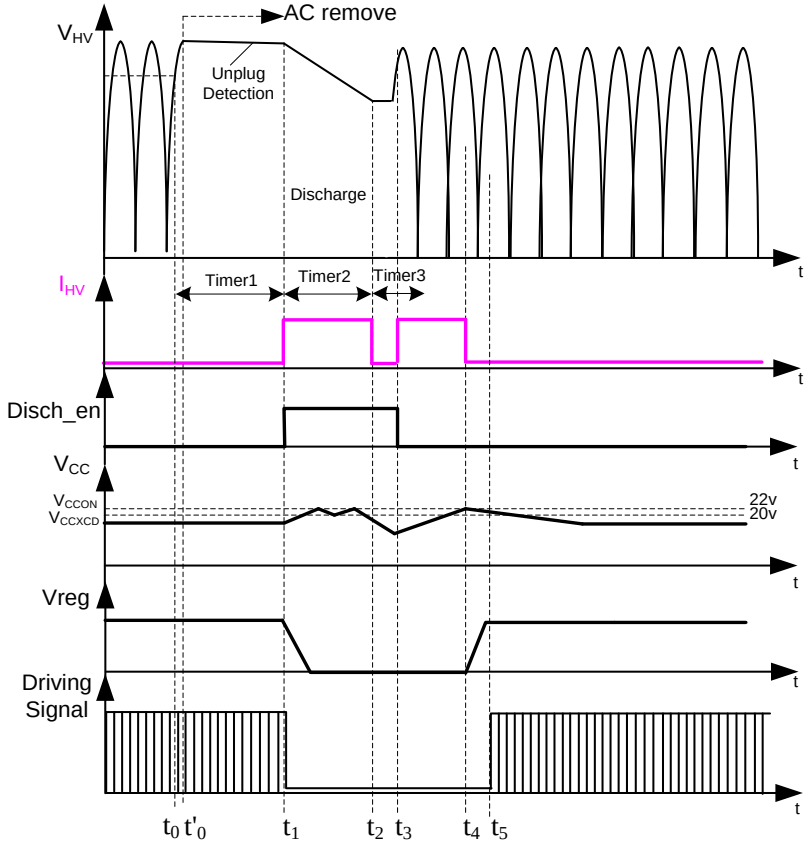
HR1210-HVCS and X-cap discharge

X-Cap Discharger:

When V_{HV} is DC or Open. Vcc will regulate in 17v~22v

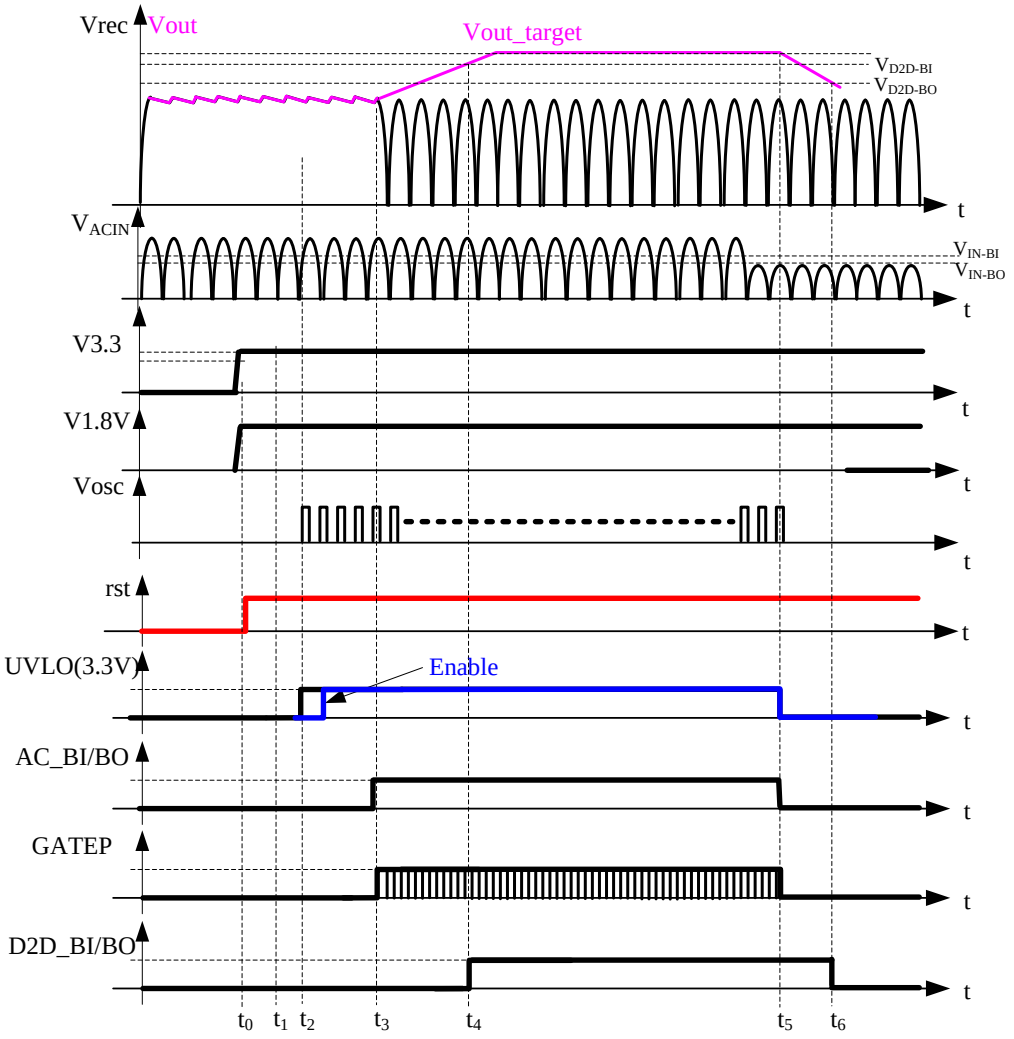


AC Removed and Don’t Recovery



AC Remove but Recovery

HR1210-PFC+LLC digital control timing



t0: Internal 1.8V supply set-up when 3.3V is ready, rst signal set-up to reset digital.

t2: UVLO high, digital control start works, sense FBP, FBL, ACIN, CSP voltage

t2~t3: $V_{in} > V_{in-BI}$, with a timer, PFC start works

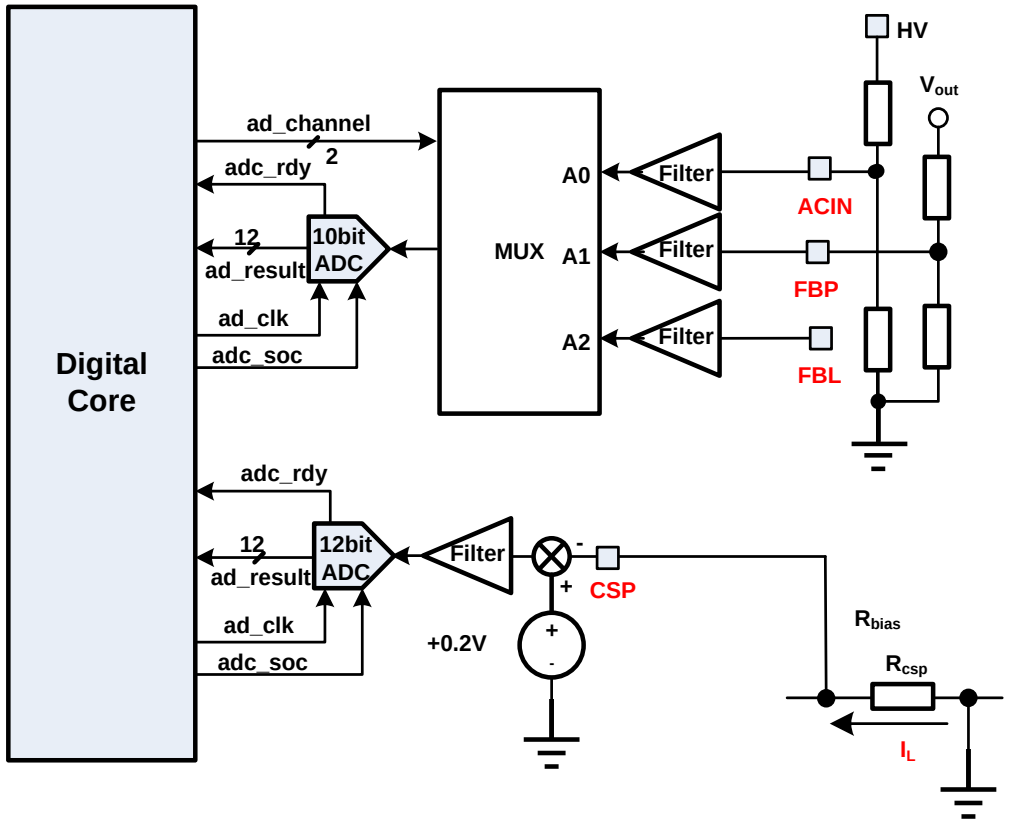
t3~t4: PFC Soft Start, LLC works when $V_{out} > V_{D2D\_BI}$

t4~t5: Normal operation

t5: $V_{in} < V_{in-BO}$ with a timer, PFC stops switching

t6: $V_{out} < V_{D2D-BO}$, LLC stops switching.

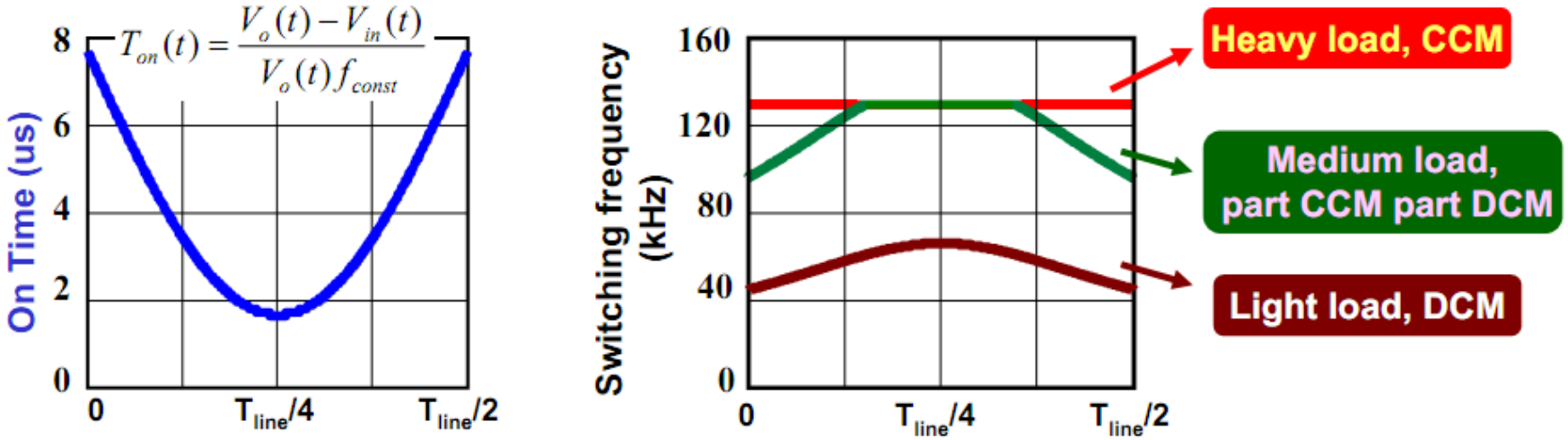
HR1210-PFC+LLC digital control sampling



- The digital core need to sample FBP (PFC output), ACIN (PFC input) & CSP (PFC inductor current) for PFC control
- The digital core need to sample FBL (LLC Feedback) for LLC control
- The FBP, FBL & ACIN is sampled by a 10bit ADC through a controlled MUX
- The CSP is sampled by a 12bit ADC
- The CSP is a negative voltage with internal biased by a 0.2V voltage source, so the sampled voltage of CSP is actually 0.2V-V_{CSP}.

HR1210-PFC digital control

Digital PFC: Quasi-fixed On Time Control



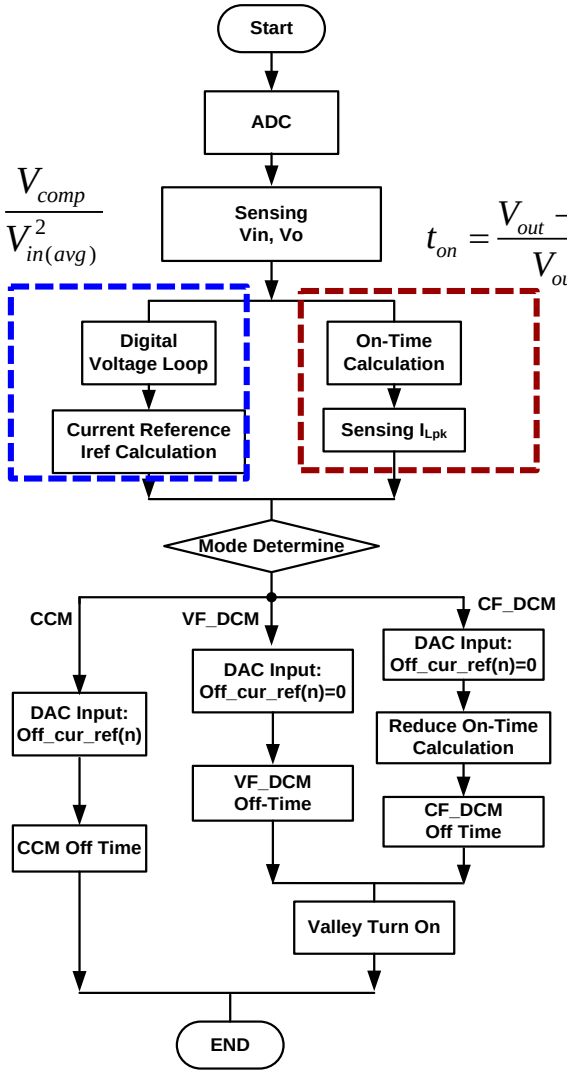
- By fix the Ton profile at different load conditions, switching frequency at light load can be reduced.
- On time is adaptively changed based on instantaneous input voltage.
- Light load efficiency can be improved.

HR1210-PFC digital control

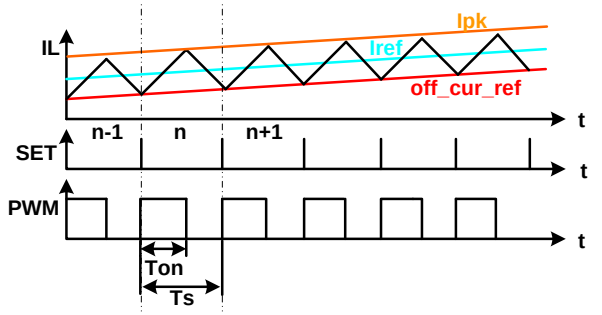
Flowchart in 1 switching cycle:

$$I_{in\_ref} = V_{in}\frac{V_{comp}}{V_{in(avg)}^2}$$

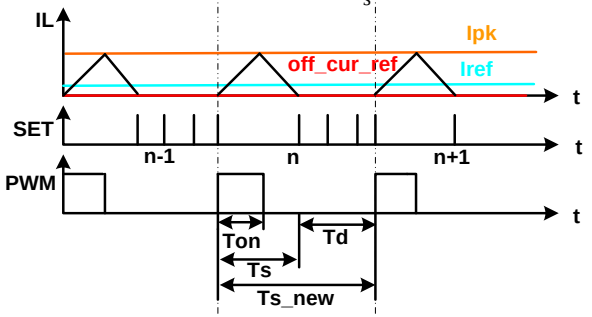
$$t_{on} = \frac{V_{out} - V_{in}}{V_{out}}T_s$$



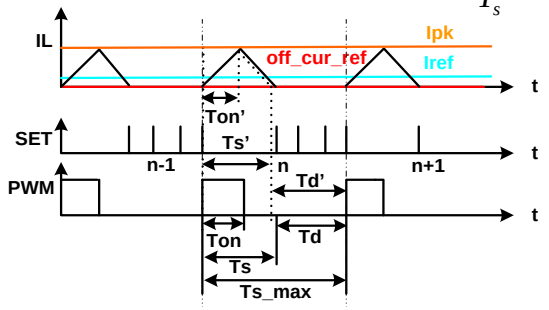
CCM: $I_{pk}(n) < 2I_{ref}(n)$



DCM: $I_{pk}(n) > 2I_{ref}(n)\cdot\frac{T_{s\_max}}{T_s}$



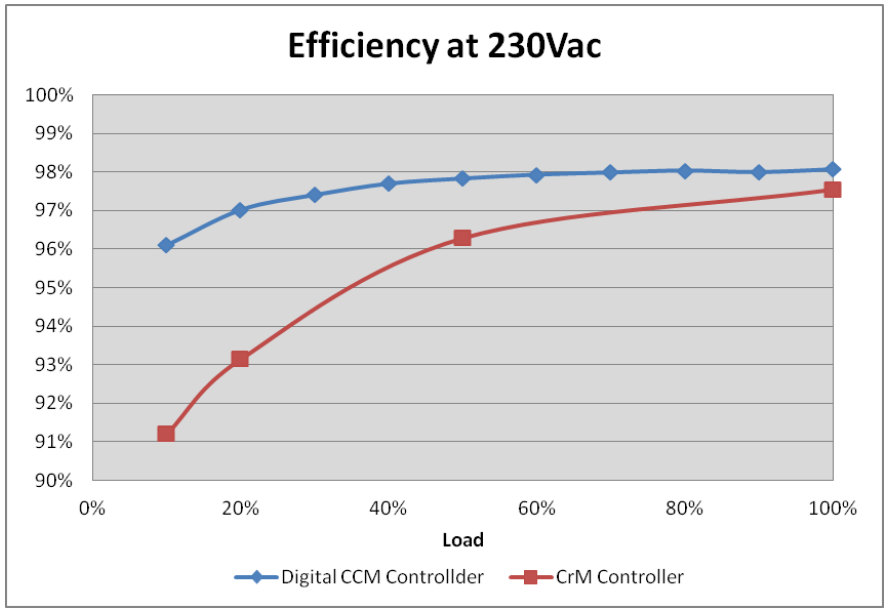
CF-DCM: $2I_{ref}(n) < I_{pk}(n) < 2I_{ref}(n)\cdot\frac{T_{s\_max}}{T_s}$

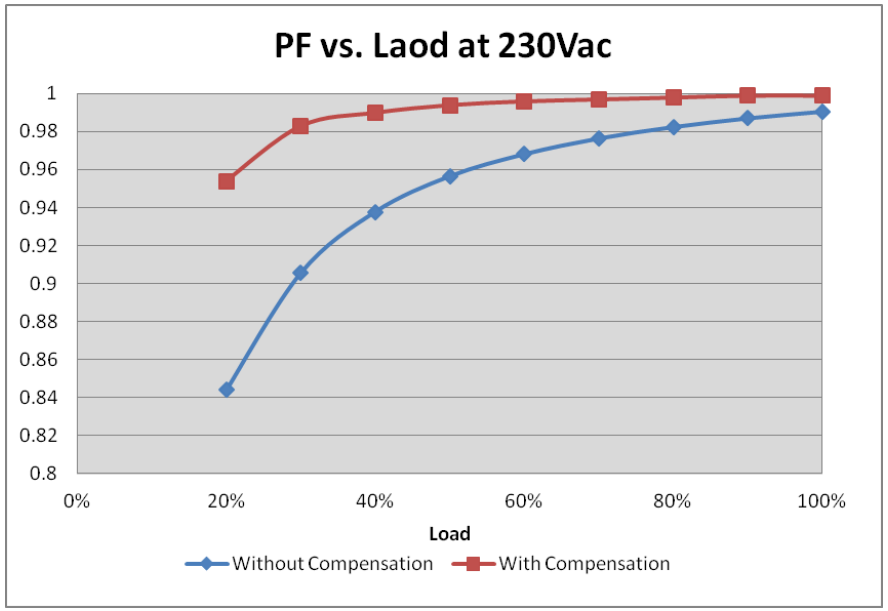


HR1210-PFC digital control

Key Performance:

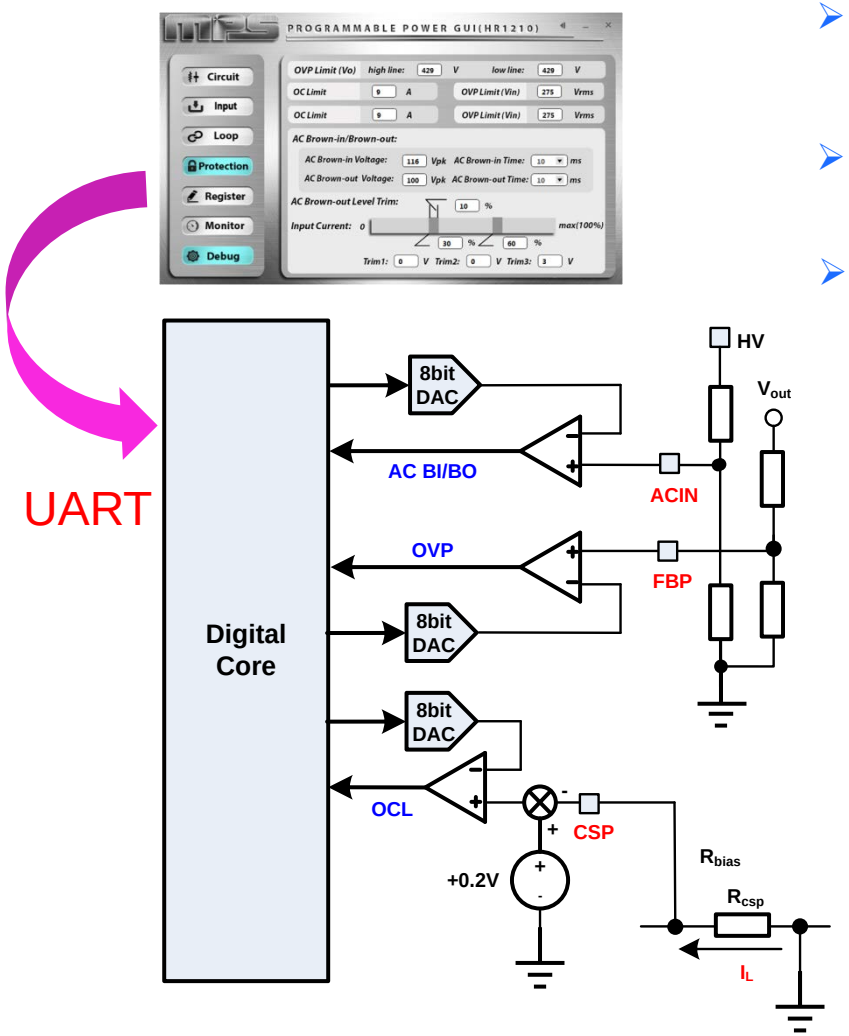
- High light load Efficiency, >96% @ 10% load of 400w output
- High light load PF, >0.95 @ 20% load for 400w output.





HR1210-PFC digital control

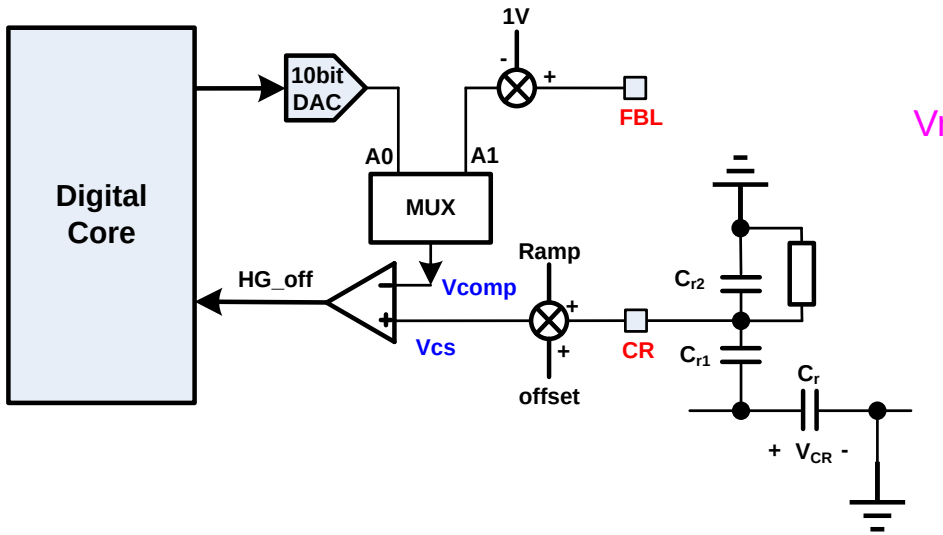
PFC Protection:

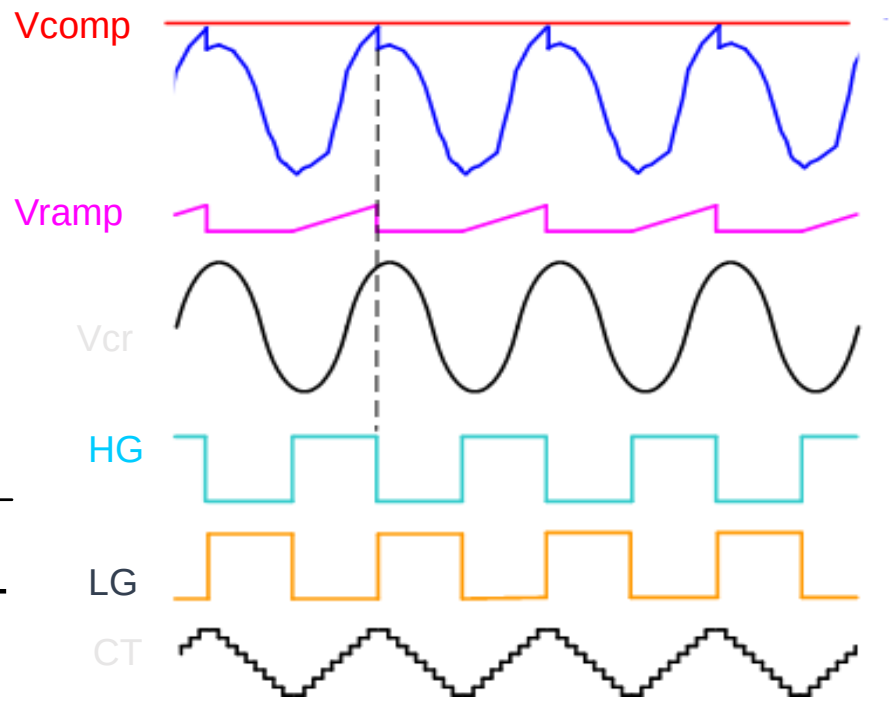


- The digital core control the threshold for AC BI/BO, OVP & OCL protection for PFC.
- A 8bit DAC is used for the output of the threshold of the protection
- By setting in GUI, the thresholds for these protection can be programmed through UART interface on IC.

HR1210-PFC digital control

LLC Current Mode Control:

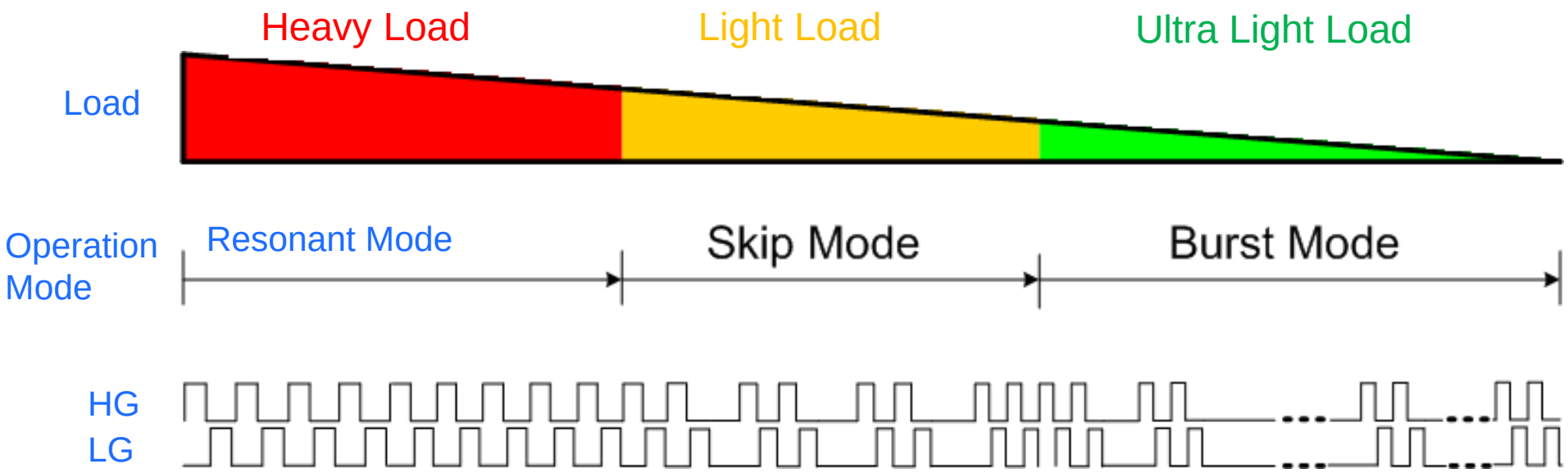




- The voltage on resonant cap (Cr) is compared with internal reference (Vcomp) to generate the HG-off signal
- The LG on time is equal with HG on time by an internal
- The Internal reference (Vcomp) is derived from FBL pin voltage or digital core (10 bit DAC), depend by LLC operating state:
  When in steady state, Vcomp=VFBL-1V
  When in Skip or burst mode, Vcomp=VDAC which determined by digital core

HR1210-LLC digital control

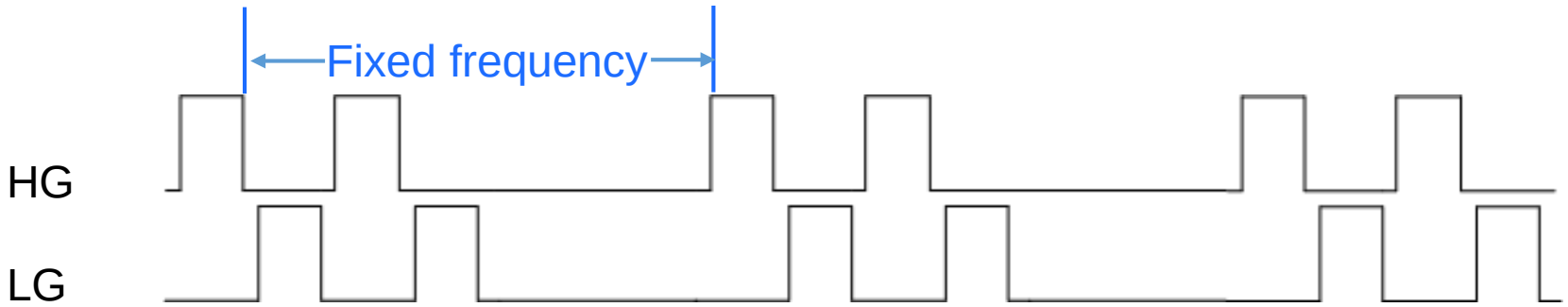
LLC Operating Mode:



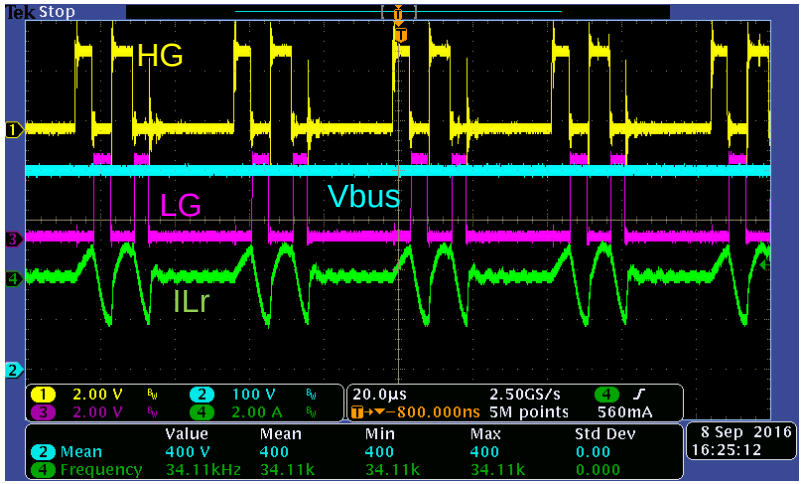
- LLC changes operation mode according to the load.
- It works in Resonant Mode (normal operation) at heavy load, switching to Skip Mode at lighter load and change to Burst Mode at ultra light load or no load.
- When run into Burst Mode, it works in PWM burst pattern to reduce audible noise.

HR1210-LLC digital control

LLC Skip Mode:

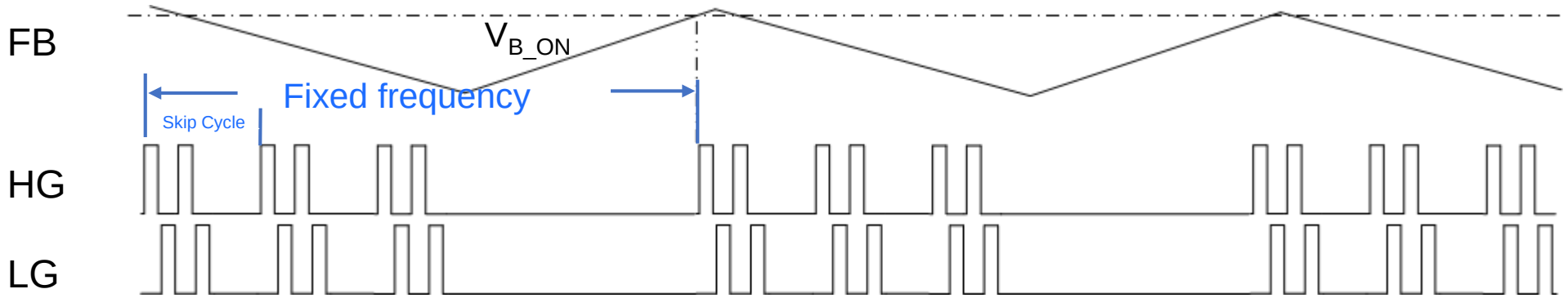


- At light load, HG & LG stops switching for a certain period every N cycles (programmable)
- The skip frequency is kept at fs (programmable)

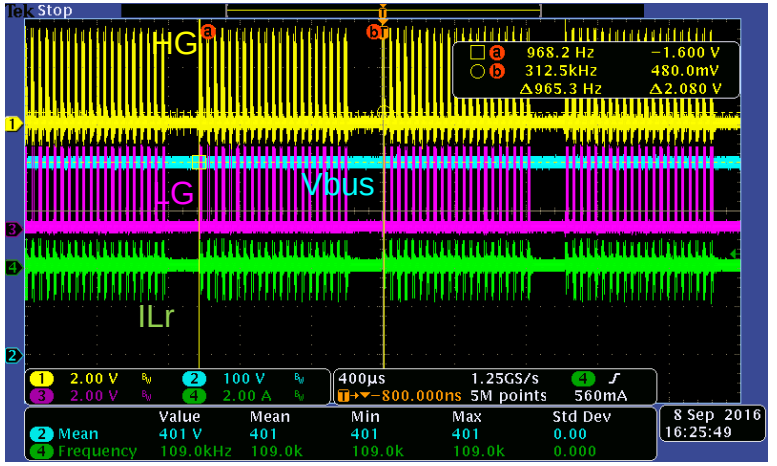


HR1210-LLC digital control

LLC Burst Mode:

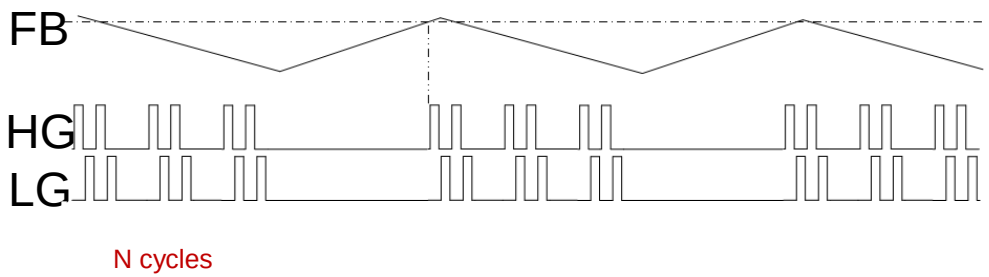


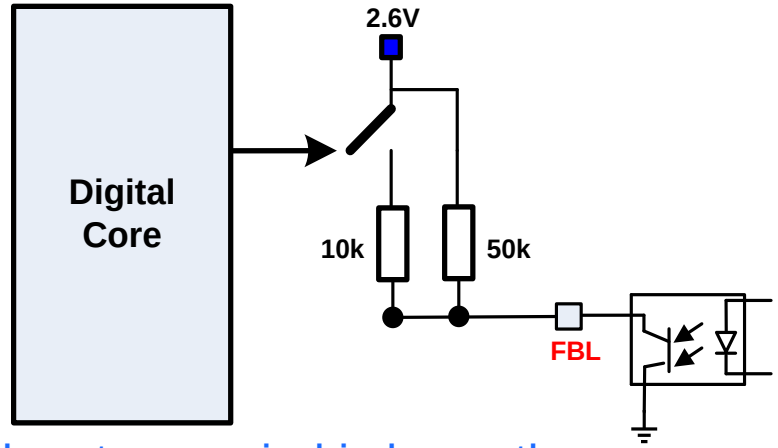
- At very light load condition, HG & LG switch in skip mode and stops switching for a long time which determined by VFBL touching the burst-on threshold (V_{B_ON})
- The burst frequency can be select to keep at fs (programmable) for low audible noise



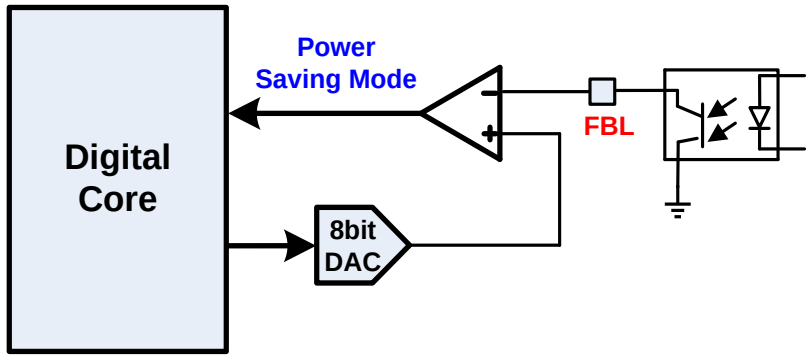
HR1210-LLC digital control

LLC Low Power Mode:





➢ When the LLC switching cycles N during each burst-on period is lower than a preset value (defined by GUI) , the digital core will switch the FBL pull up resistor from ~8kOhm to 50kOhm to pull down the opto current

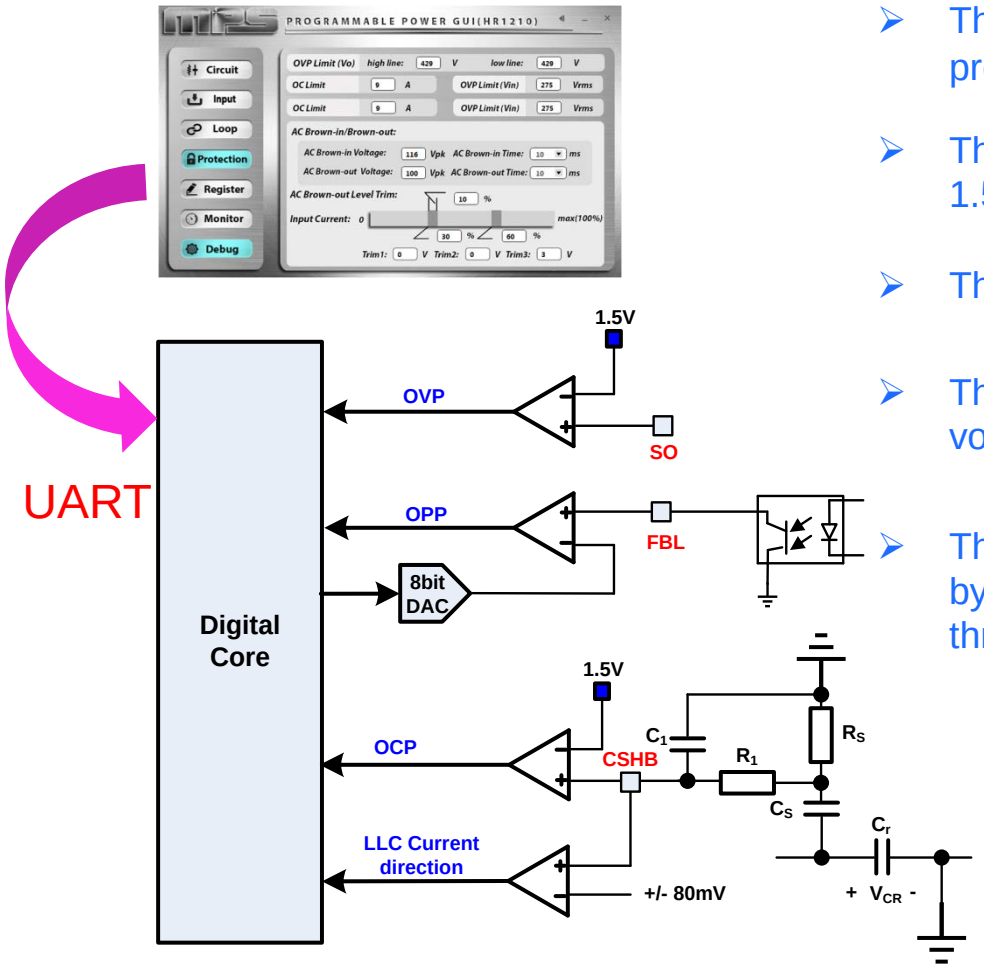


➢ When VFBL voltage (during burst-off) is lower than a preset value (defined by GUI) , the IC will enter

➢ In power saving mode, the IC will only active some necessary internal circuits, which help to decrease the

HR1210-LLC digital control

LLC Protection:

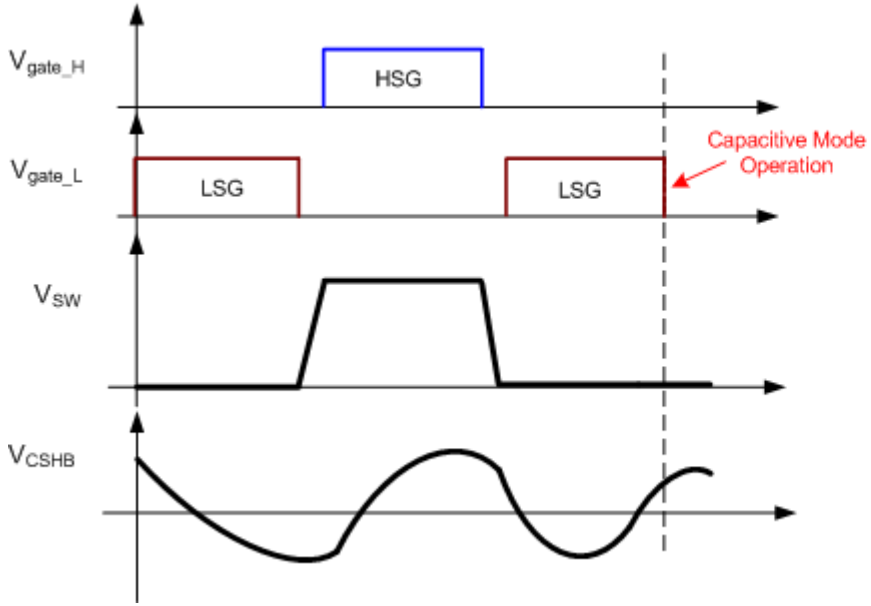


- The digital core control the threshold for OPP protection for LLC.
- The OVP protection is achieved by SO pin with fixed 1.5V threshold
- The CSHB pin is used to sense the LLC current
- The OCP protection is achieved by compare current sense voltage on CSHB with 1.5V fixed threshold.
- The digital core also sense the current direction of LLC by comparing the CSHB voltage with fixed +/- 80mV threshold (This used for CMP of LLC, see next page)

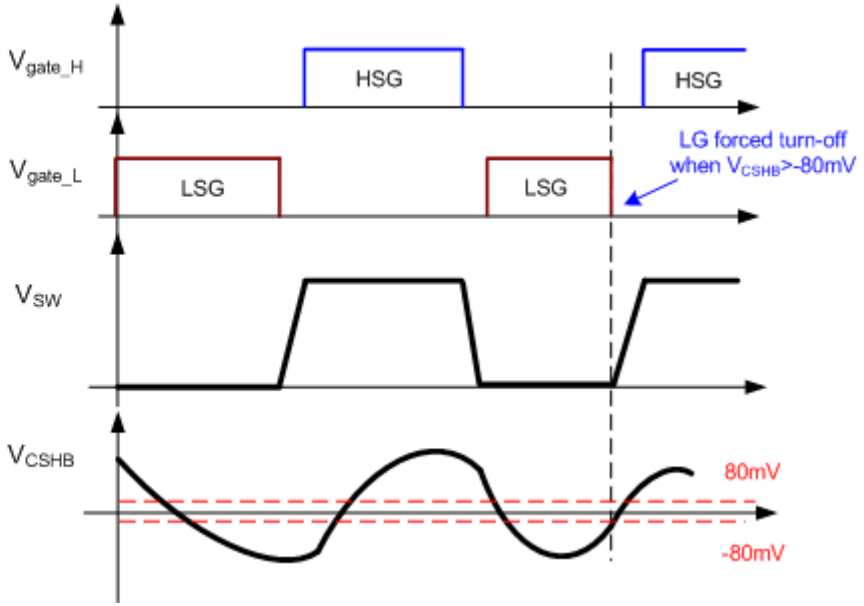
HR1210-LLC digital control

CMP (Capacitive Mode Protection):

Without CMP



HR1210 with CMP



Capacitive Mode operation:
HG turned off at I_r<0 (V_{CSHB}<0);
LG turned off at I_r>0 (V_{CSHB}>0);

In HR1210
HG will be forced off when V_{CSHB}>-80mV
LG will be forced off when V_{CSHB}<80mV

HR1210 key features

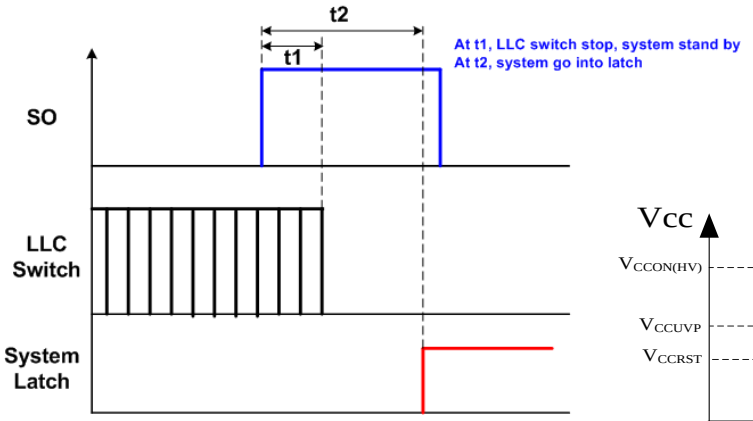
Enhanced Surge Immunity

Issue

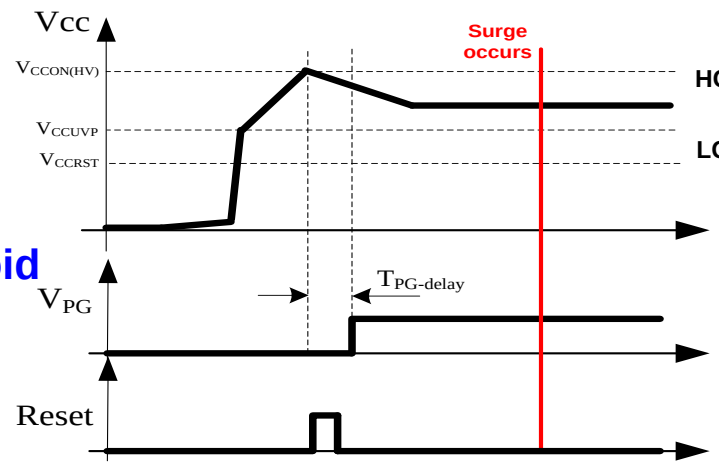
System shutdown & output drops when surge occur:

- Surge noise lead the digital IC restart.
- Surge noise trigger LLC OVP on SO pin
- Surge noise trigger LLC SCP on CSHB pin

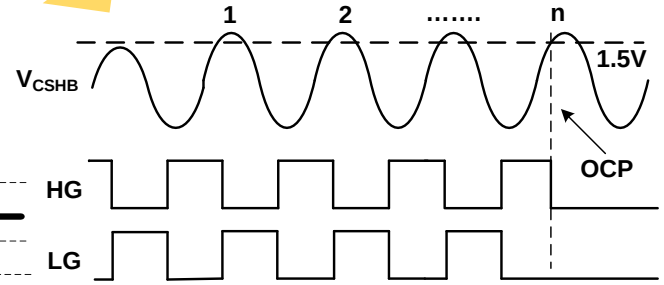
HR1210



A digital filter on SO to avoid error trigger



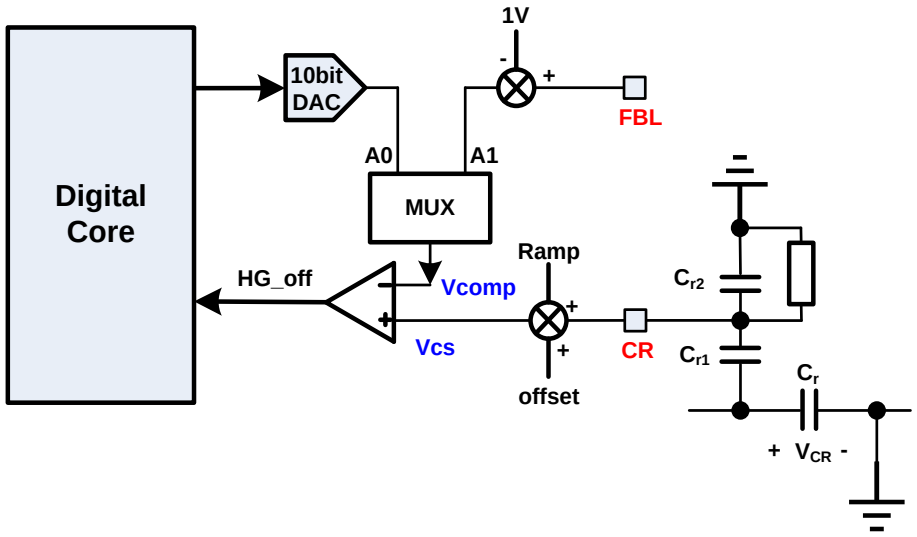
PG signal to indicate a real restart

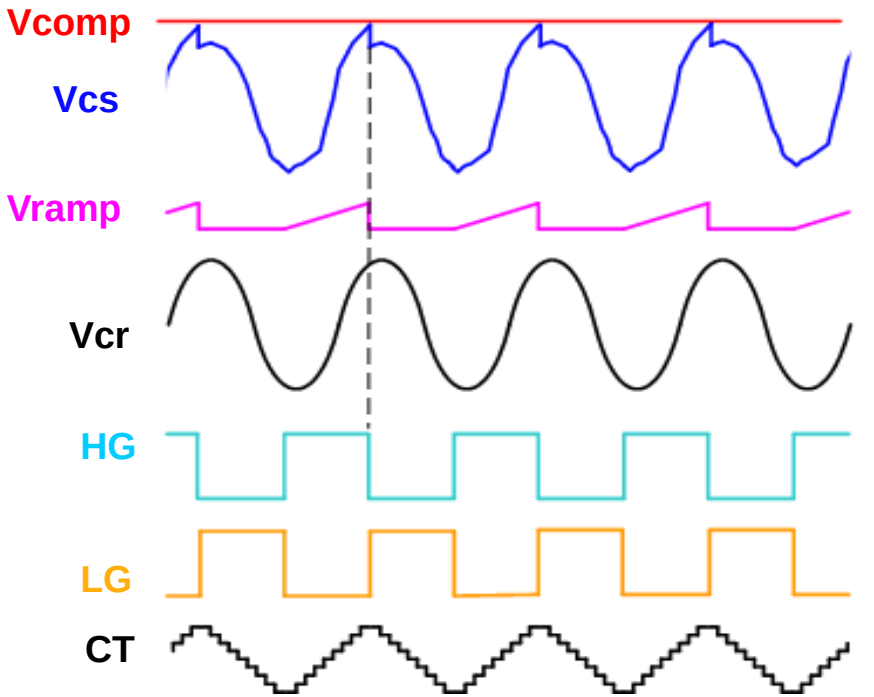


CSHB Counter to filter noise

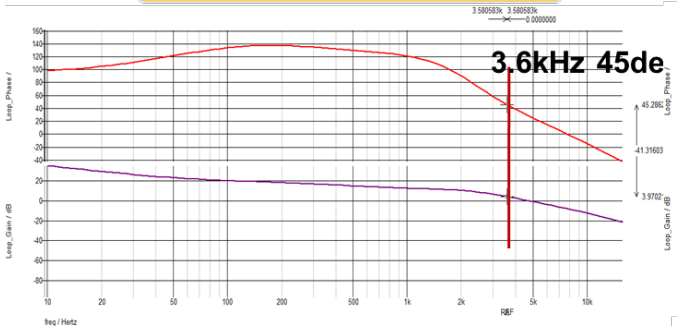
HR1210 key features

Current Mode Control LLC with better loop response

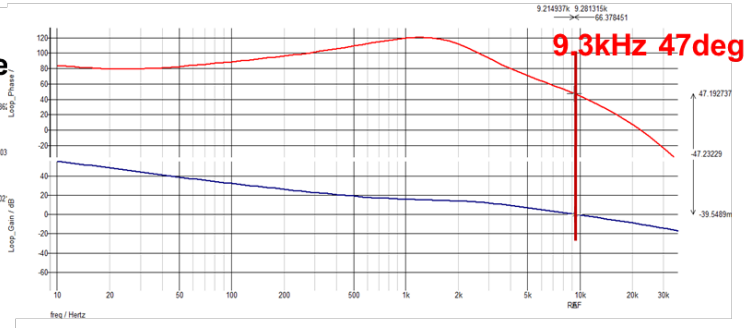




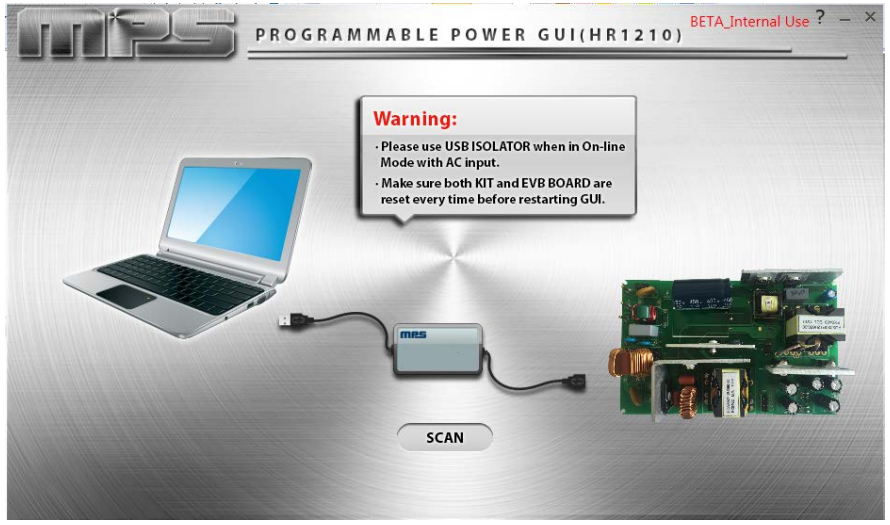
LLC_Voltage Mode Control



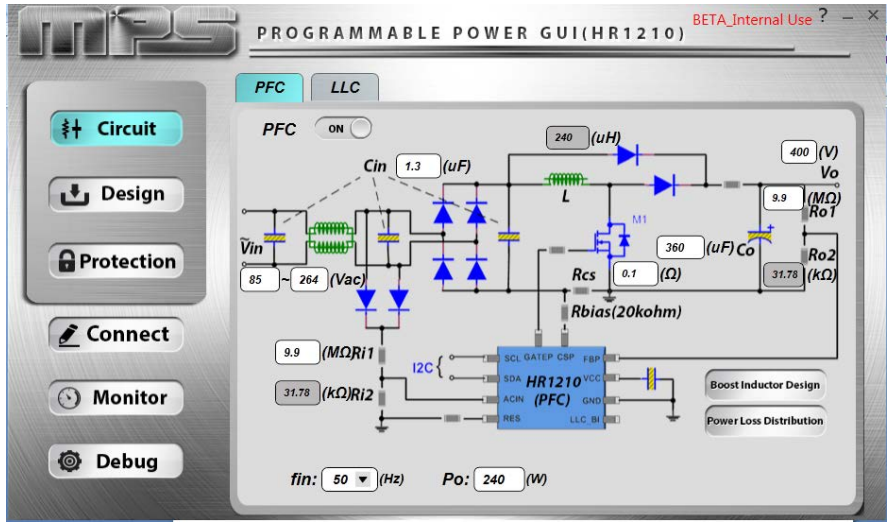
LLC_Current Mode Control



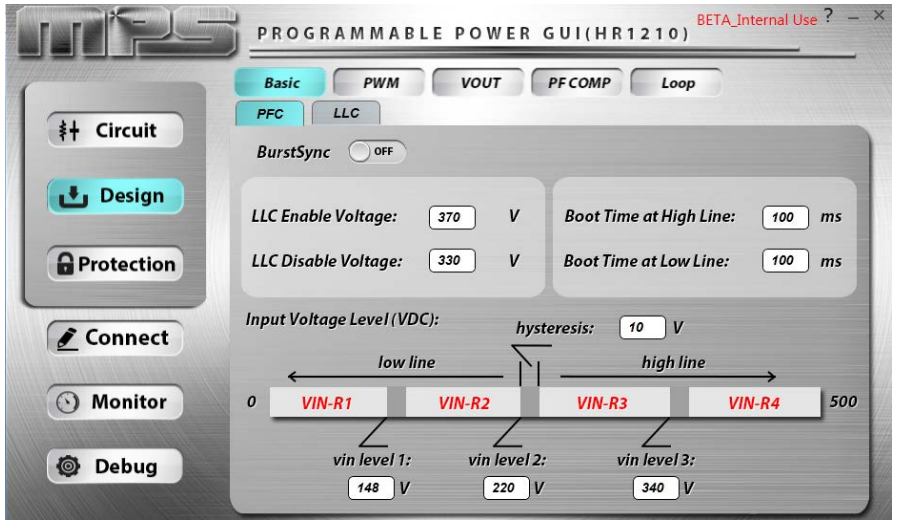
HR1210 User GUI for Parameters Configuration



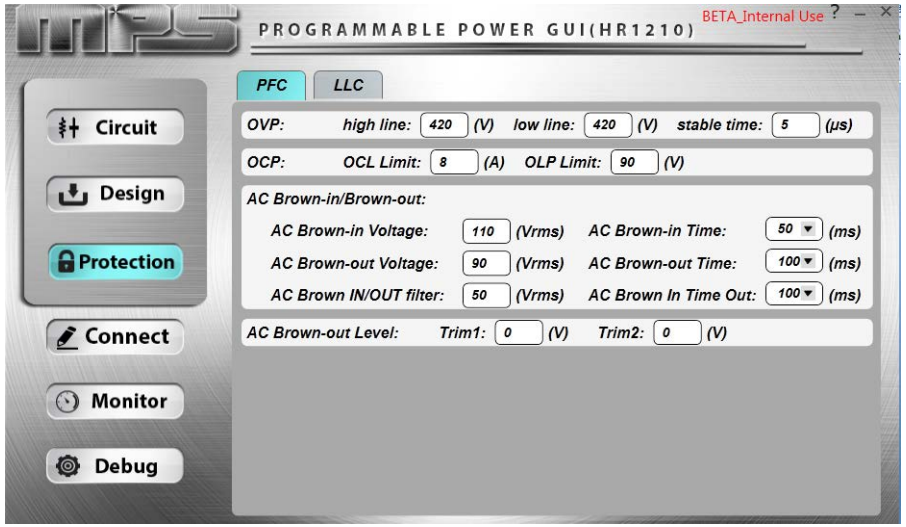
Step1: Connection Kits



Step2: Configuration Parameters



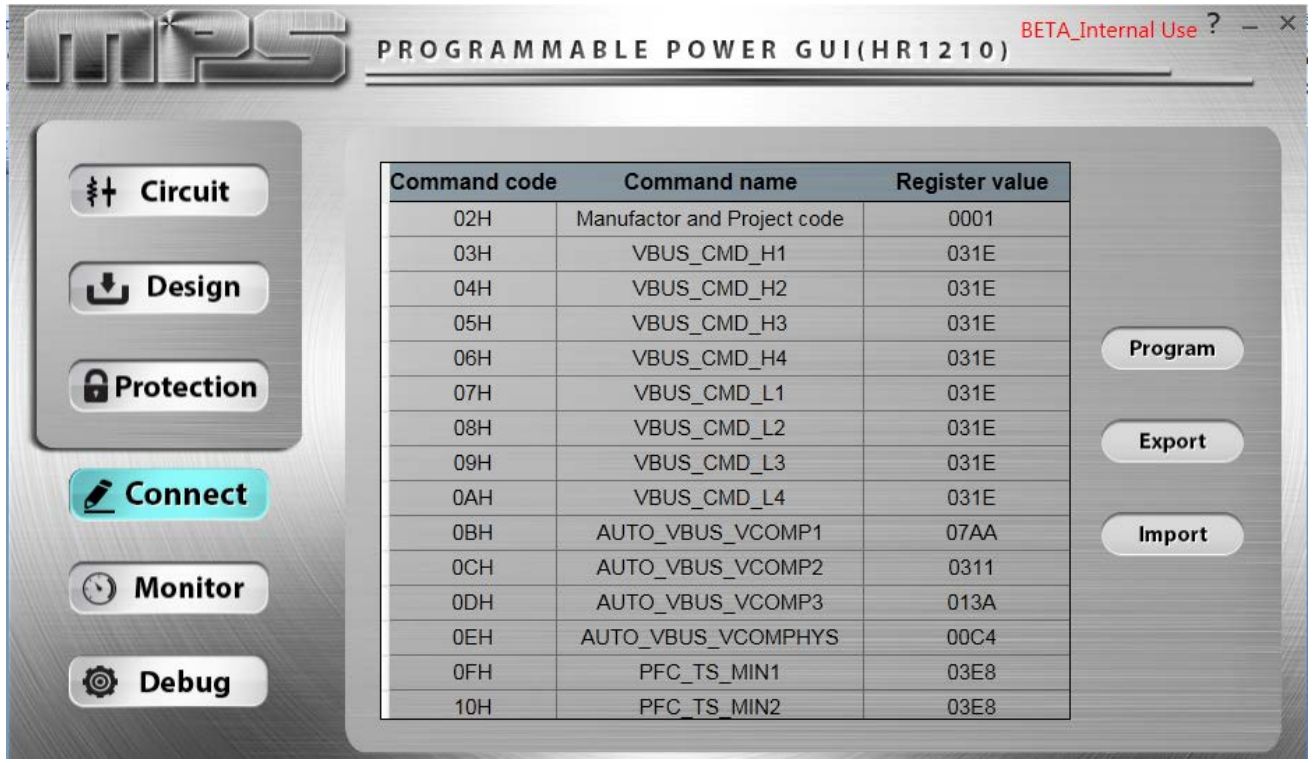
Input PFC & LLC Design Parameters



Input PFC & LLC Protection Parameters

HR1210 User GUI for Parameters Configuration

Use GUI for Parameters Configuration :

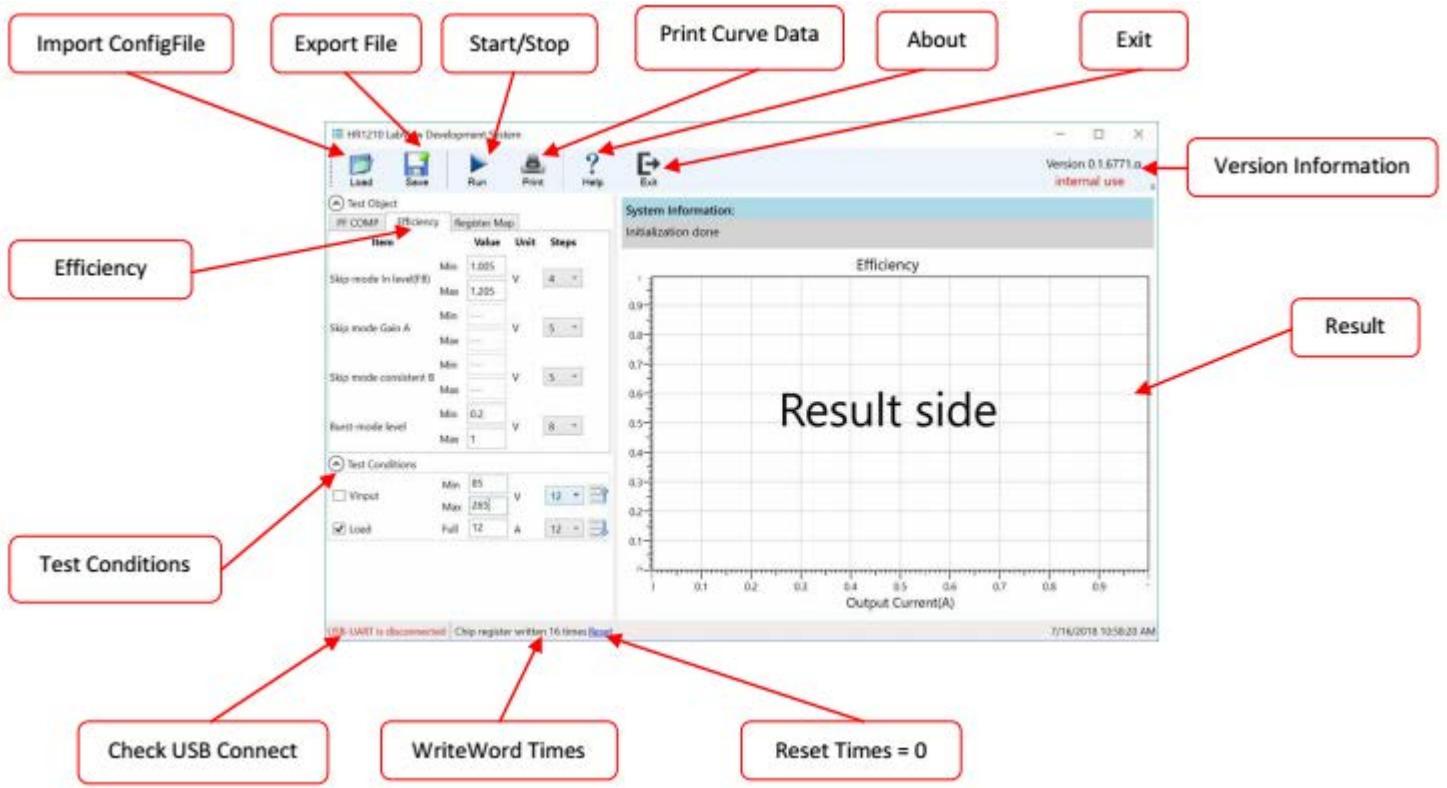


Command code	Command name	Register value
02H	Manufactor and Project code	0001
03H	VBUS_CMD_H1	031E
04H	VBUS_CMD_H2	031E
05H	VBUS_CMD_H3	031E
06H	VBUS_CMD_H4	031E
07H	VBUS_CMD_L1	031E
08H	VBUS_CMD_L2	031E
09H	VBUS_CMD_L3	031E
0AH	VBUS_CMD_L4	031E
0BH	AUTO_VBUS_VCOMP1	07AA
0CH	AUTO_VBUS_VCOMP2	0311
0DH	AUTO_VBUS_VCOMP3	013A
0EH	AUTO_VBUS_VCOMPHYS	00C4
0FH	PFC_TS_MIN1	03E8
10H	PFC_TS_MIN2	03E8

Import & Export Register List

HR1210 User GUI for Parameters Configuration

Design Optimization with Labview:



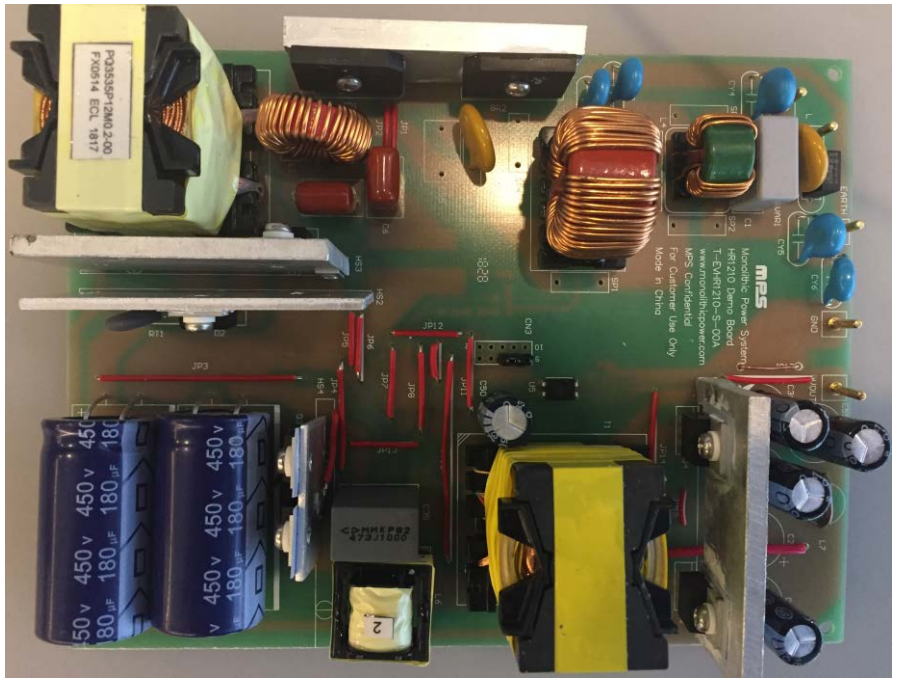
Use labview to get optimized parameters to improve the design

Appendix

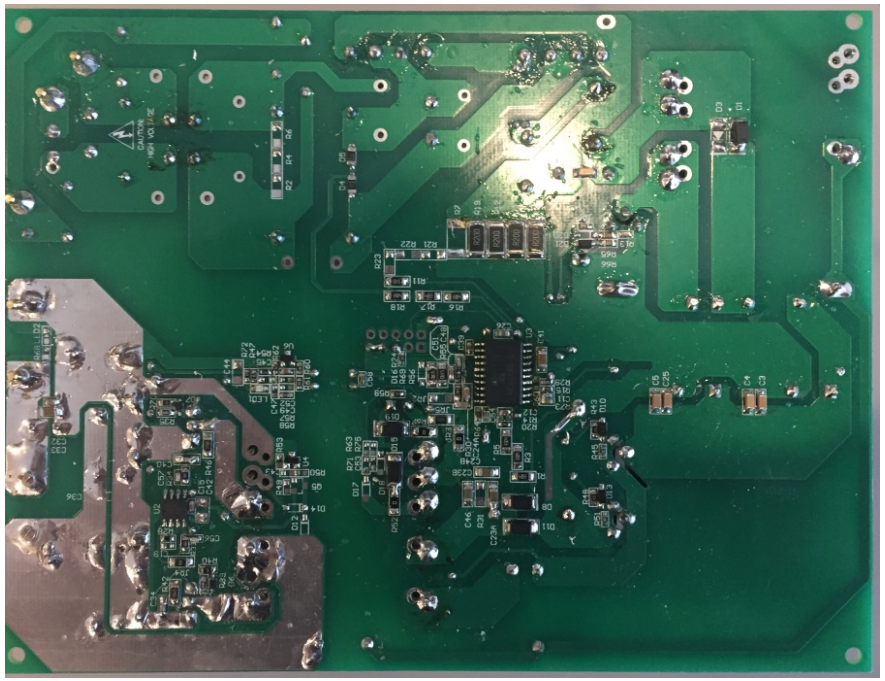
HR1210-Demo board and test results

HR1210 Demo Board (12V/33.3A):

TOP VIEW



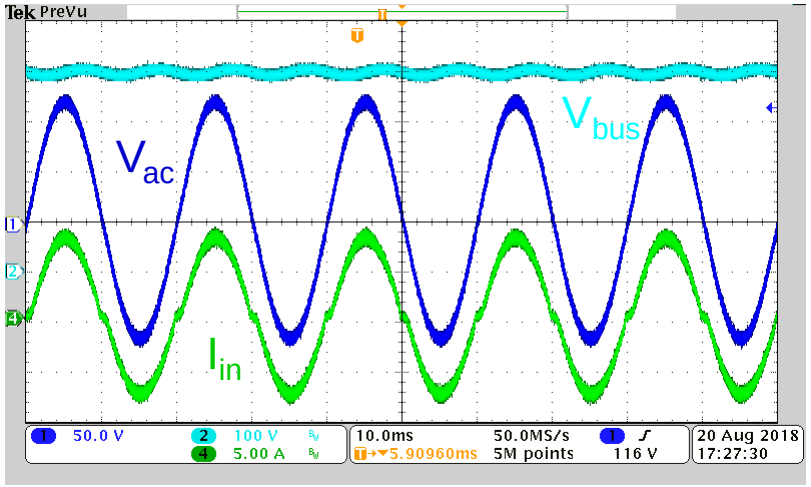
BOTTOM VIEW

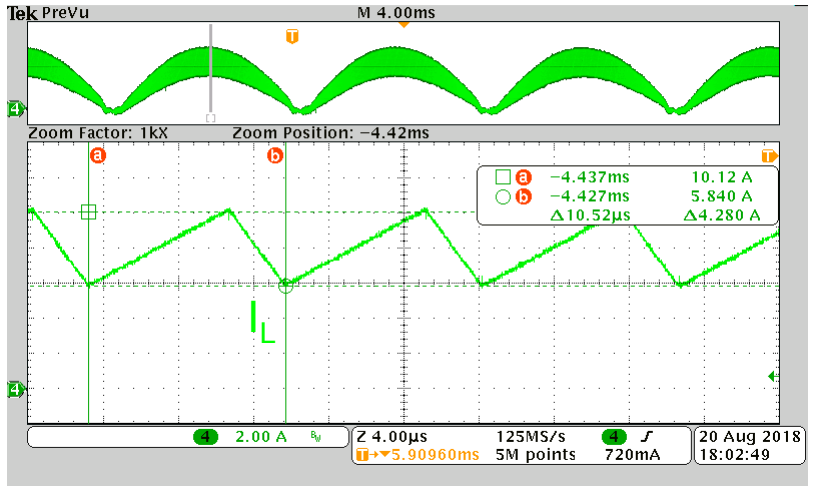


HR1210-Demo board and test results

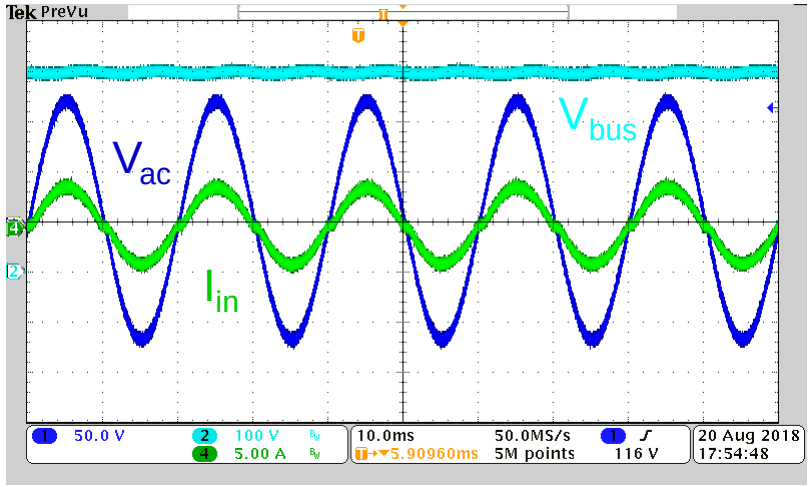
Steady State Waveform (PFC):

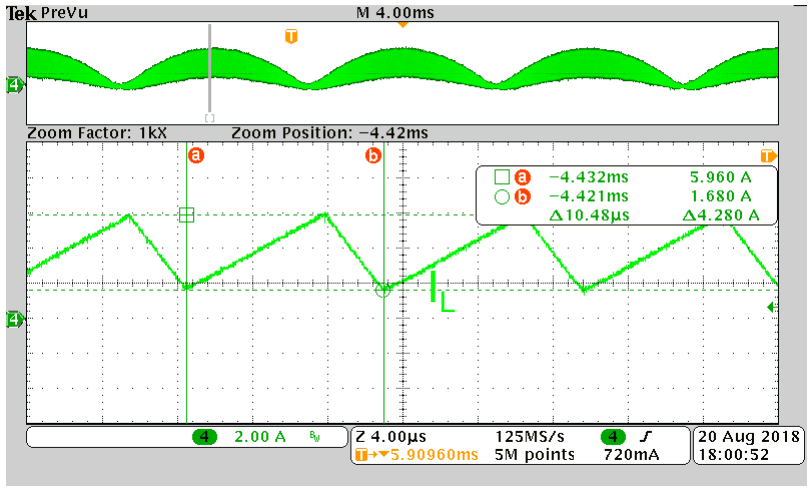
Test Condition: Vin=85Vac, Full Load





Test Condition: Vin=85Vac, 50% Load

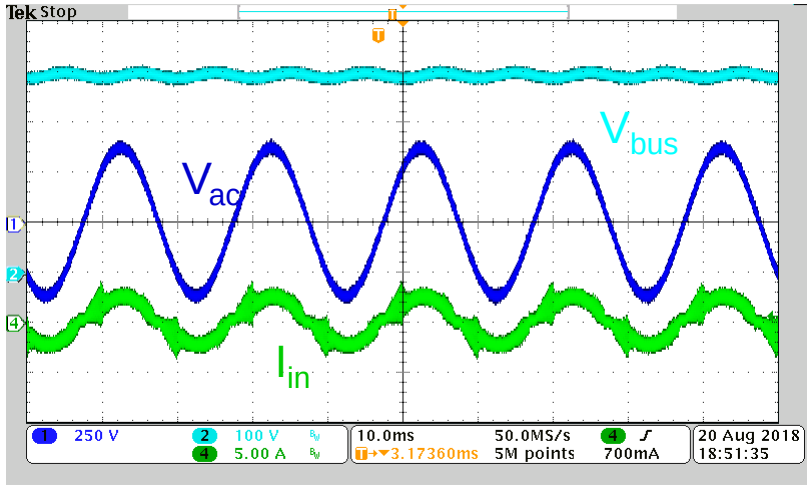


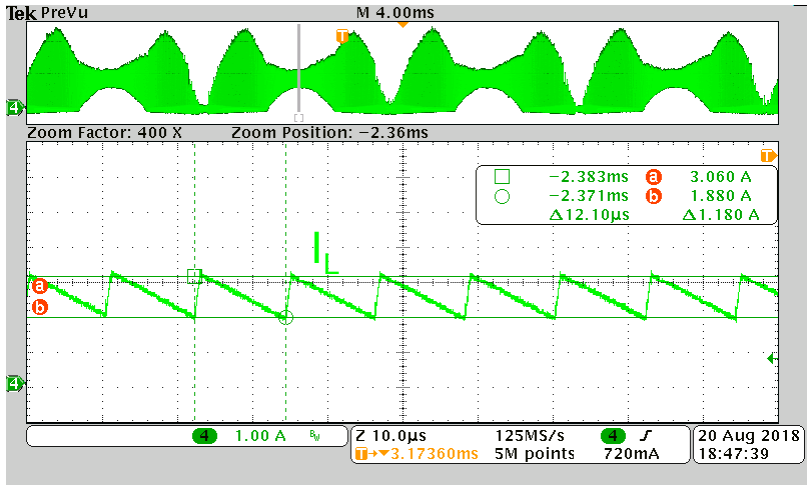


HR1210-Demo board and test results

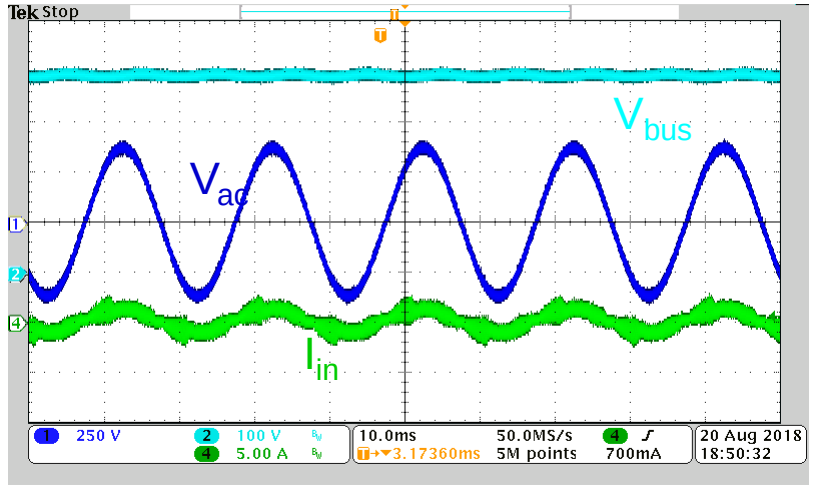
Steady State Waveform (PFC):

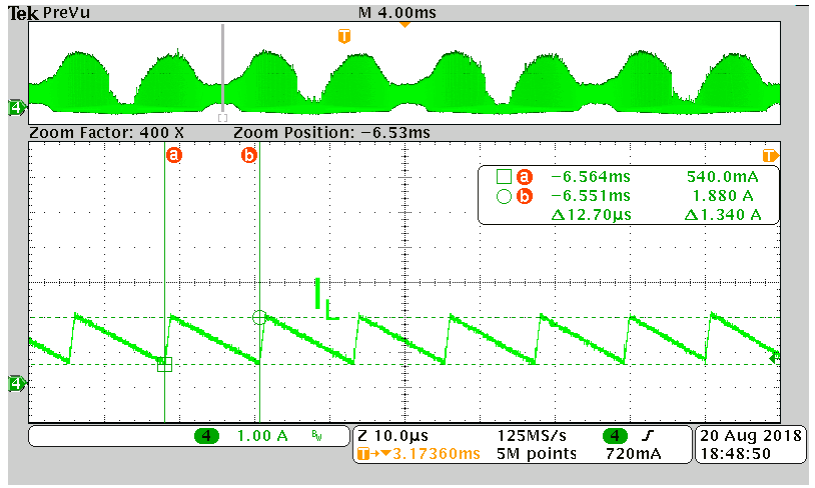
Test Condition: Vin=265Vac, Full Load





Test Condition: Vin=265Vac, 50% Load

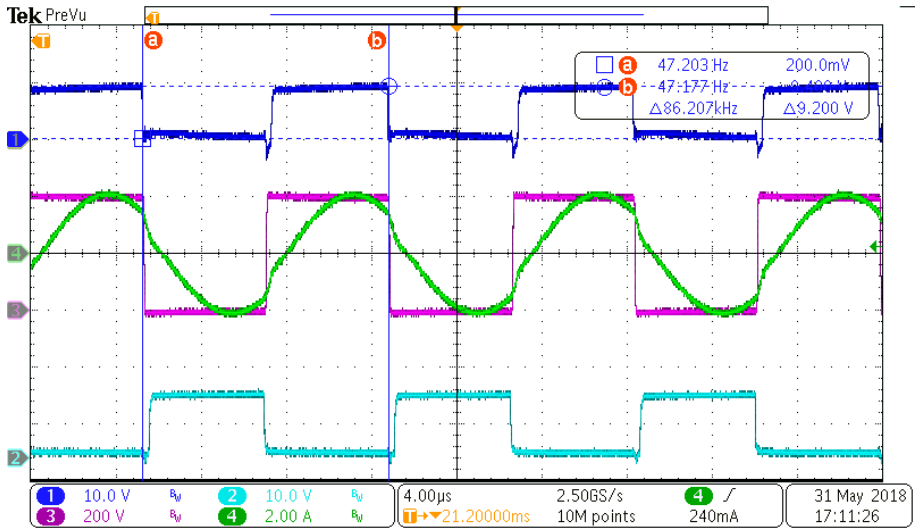




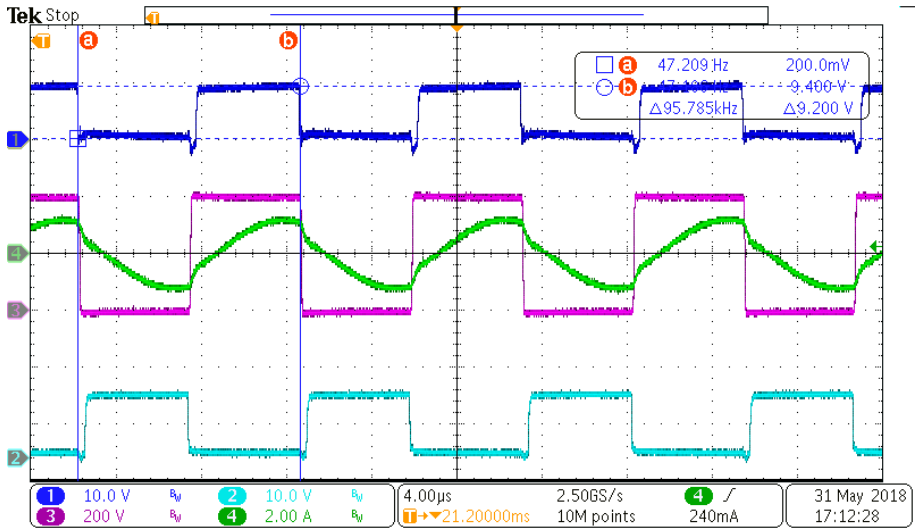
HR1210-Demo board and test results

Steady State Waveform (LLC):

Test Condition: Vin=220Vrms, Io=20A



Test Condition: Vin=220Vrms, Io=10A

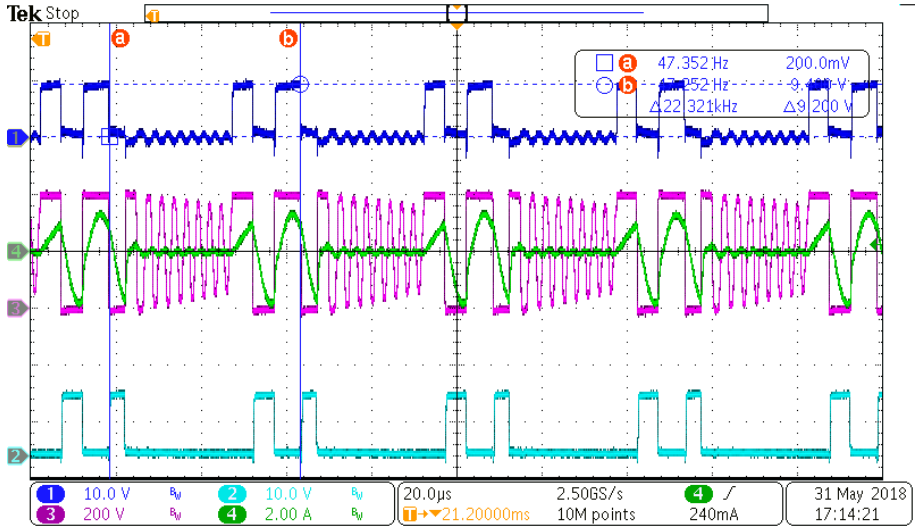


CH1:HSG CH:LSG CH3:SW CH4:Ir

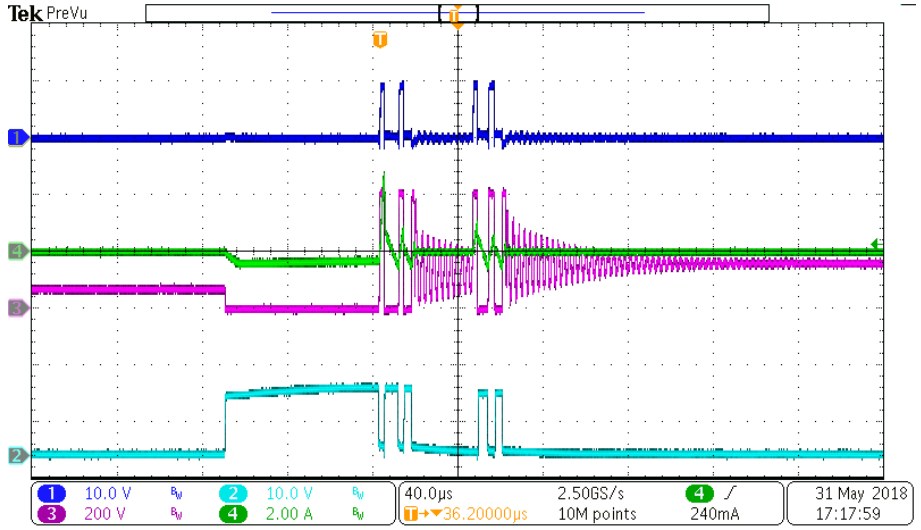
HR1210-Demo board and test results

Steady State Waveform (LLC):

Test Condition: Vin=220Vrms, Io=5A



Test Condition: Vin=220Vrms, Io=0A

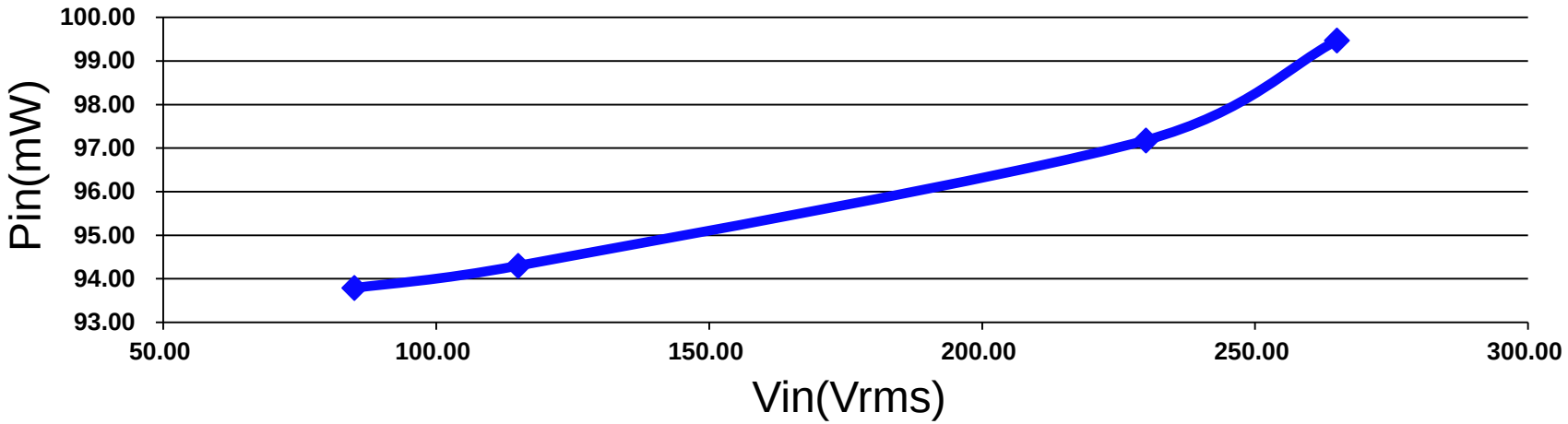


CH1:HSG CH2:LSG CH3:SW CH4:Ir

HR1210-Demo board and test results

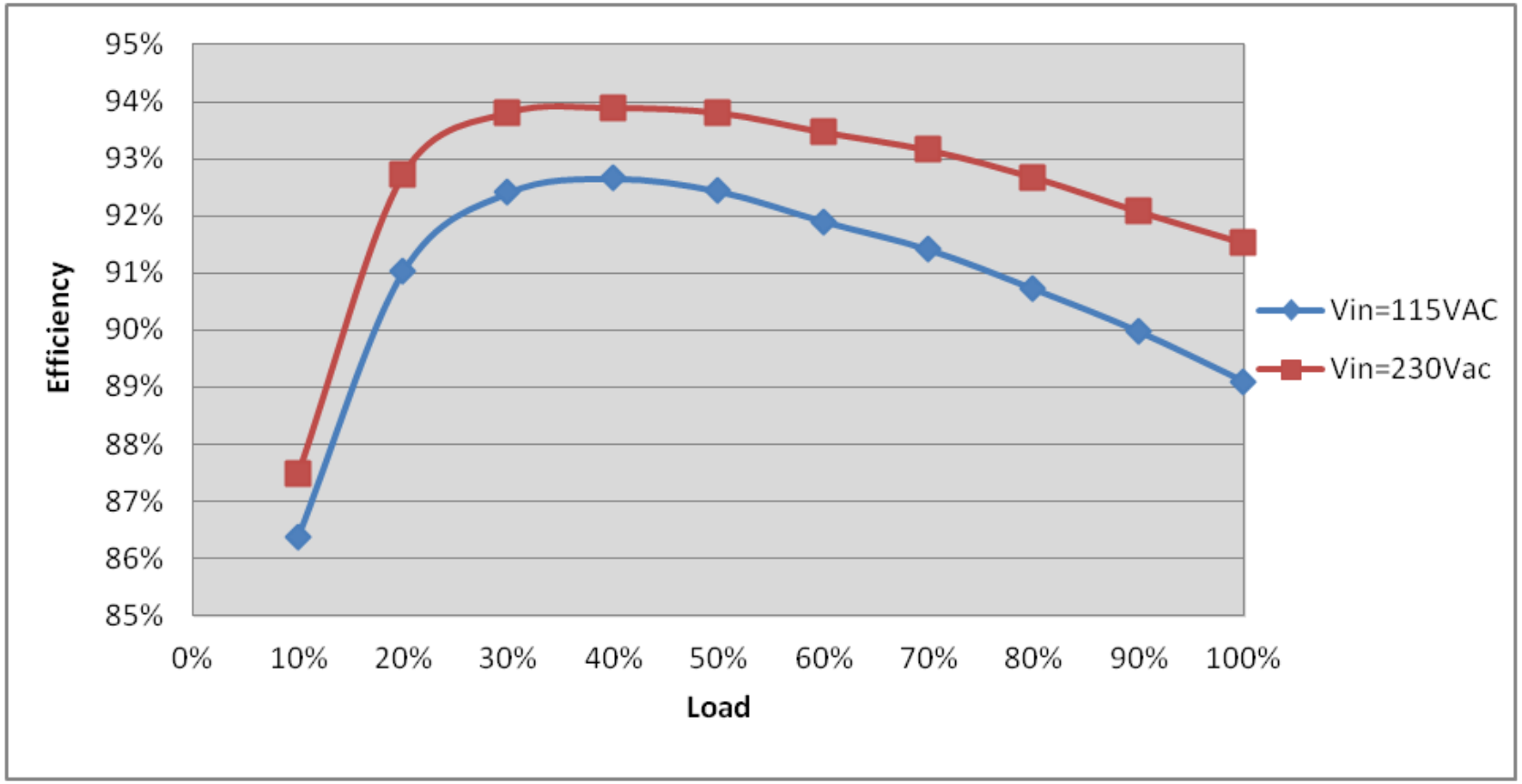
No Load Power Consumption:

Vin	85Vac	115Vac	230Vac	265Vac
No load consumption	93.79mW	94.30mW	97.18mW	99.47mW



HR1210-Demo board and test results

Total Efficiency:

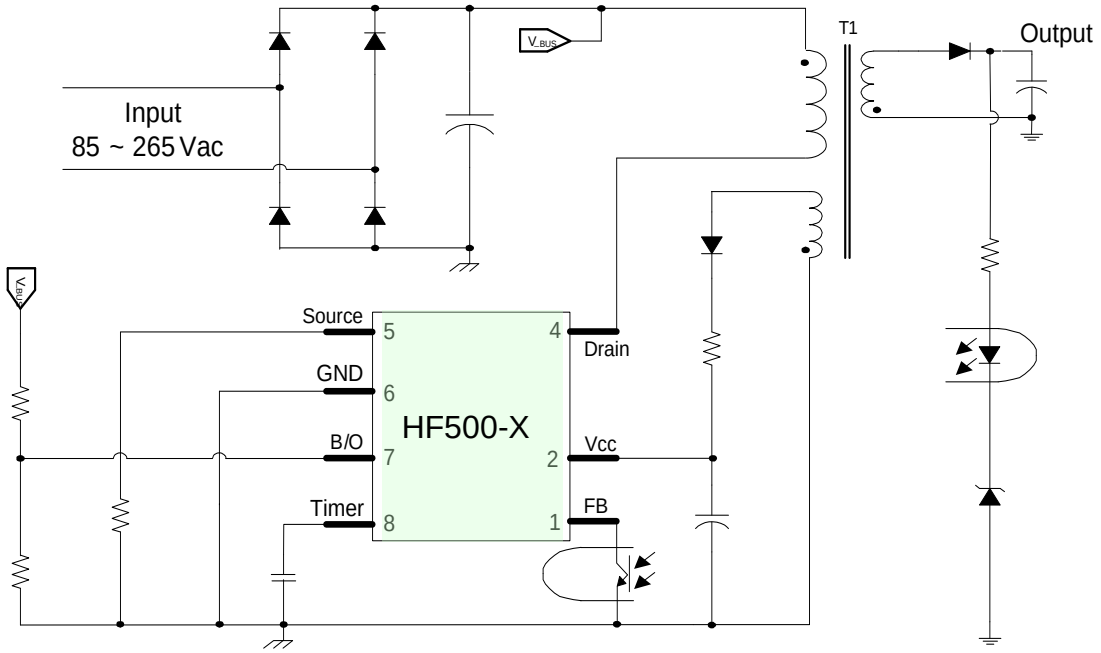


Full Features Flyback Solution-HF500-X

Features

- 700V FET integrated
- Fixed-frequency current mode control operation with built-in slope compensation
- Frequency Foldback down to 25kHz at light load condition
- Burst Mode for low standby power consumption
- Frequency jittering for a reduced EMI signature
- Over power compensation
- Internal high voltage current source
- VCC UVLO
- Programmable input B/O and OVP
- Over Load Protection with programmable delay
- Latch-off protection on TIMER pin
- OVP, OTP, SCP
- Programmable soft start

Typical application



Full Features Flyback Solution-HF500-X

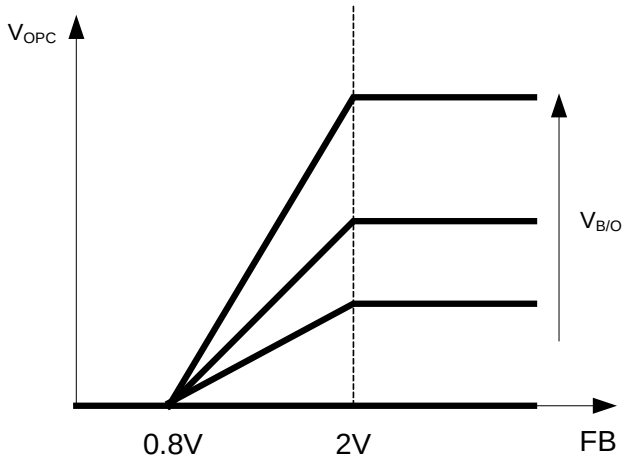
HF500-X Family

Part No	HF500-7	HF500-15	HF500-30	HF500-40
Package	SOIC8-7	SOIC8-7	DIP8-7	DIP8-7
Integrated Mosfet Ron	12Ω/700V	4.5Ω/700V	1.4Ω/700V	1.0Ω/700V
Power Rating Target	5-7W	7-15W	25-30W	35-40W

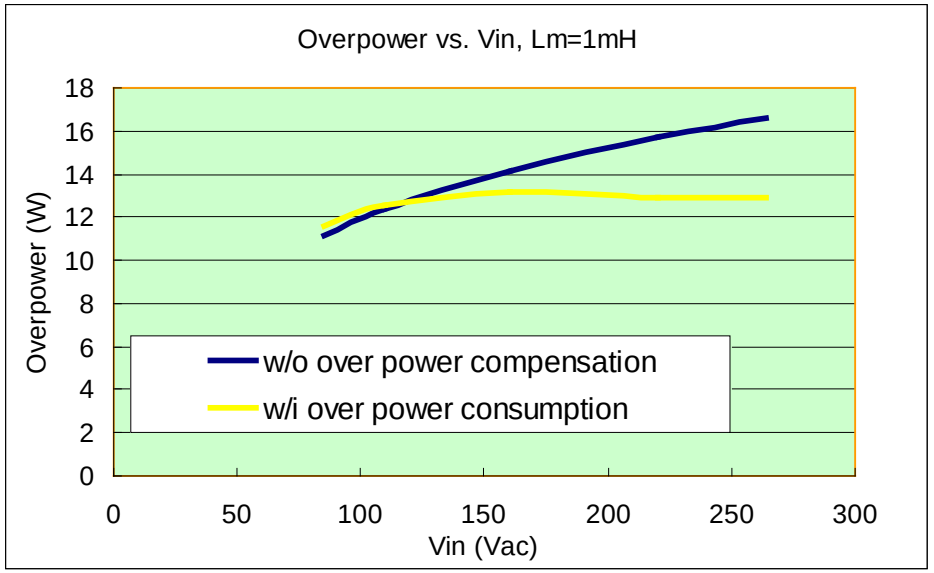
All parts released

Full Features Flyback Solution-HF500-X

➢ Over Power Compensation



$$V_{OPC} = 94mV \cdot (V_{B/O} - 1.1)$$

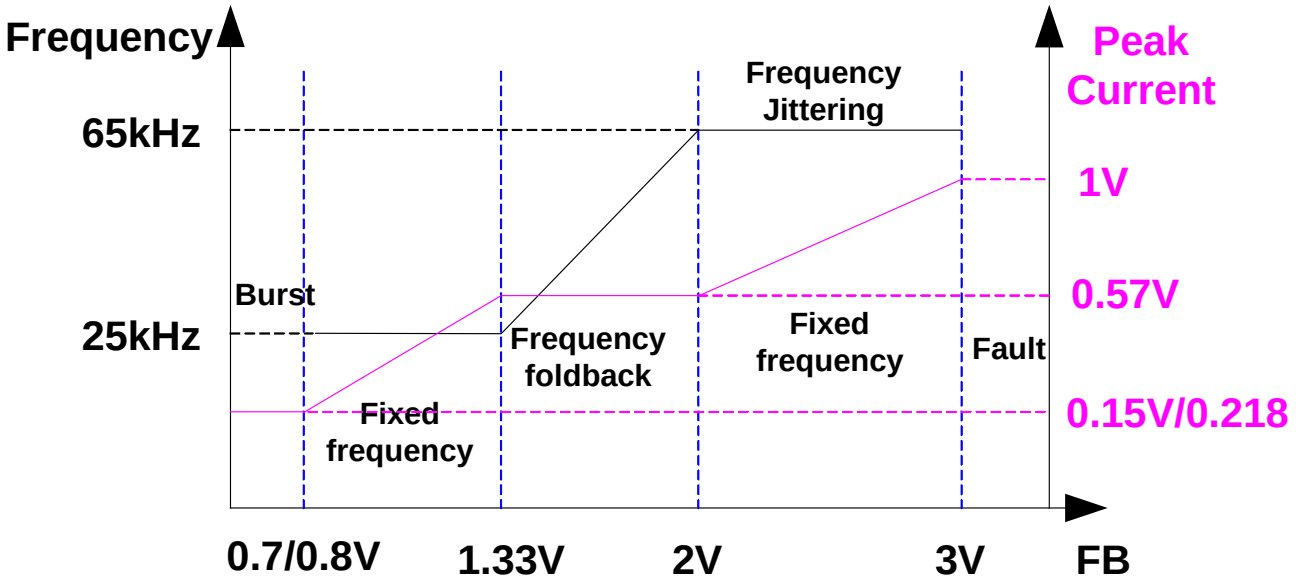


Based on 10W output design

The over power point can be kept similar both in low line and high line.

Full Features Flyback Solution-HF500-X

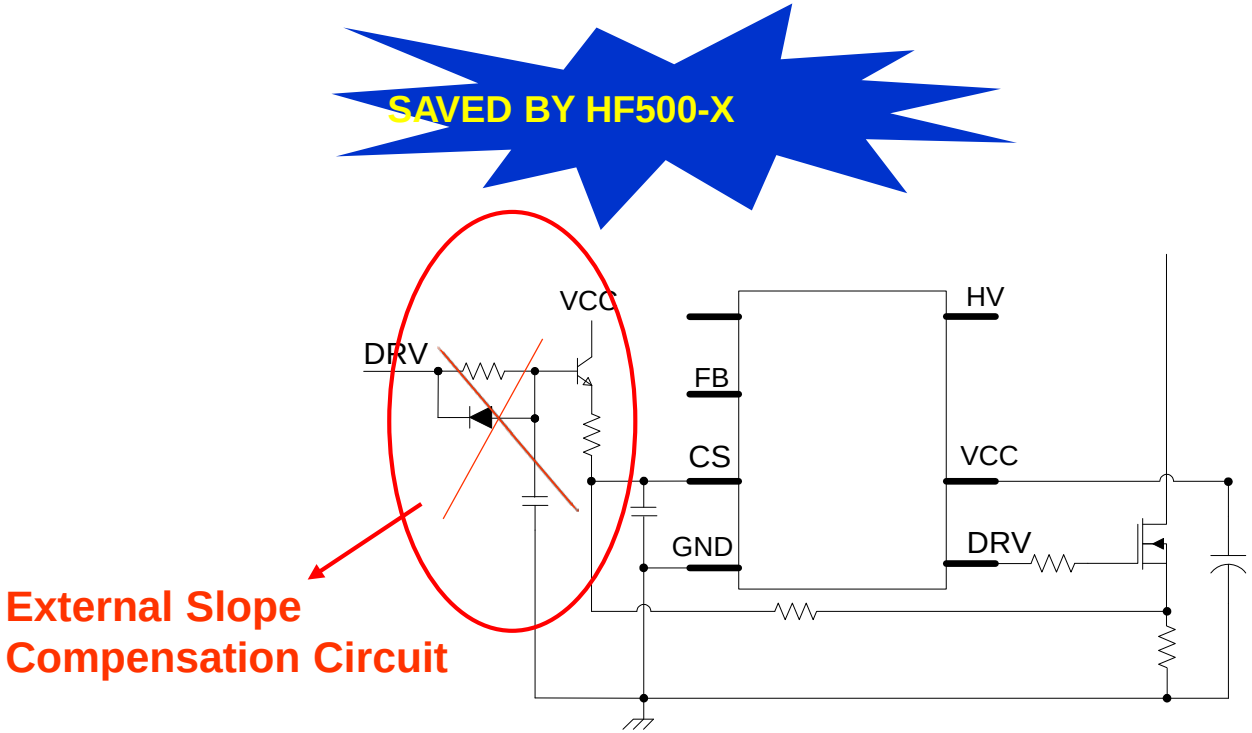
➢ Frequency Foldback



Frequency foldback at light load condition for higher efficiency and low no load power consumption.

Full Features Flyback Solution-HF500-X

➢ Internal Slope Compensation

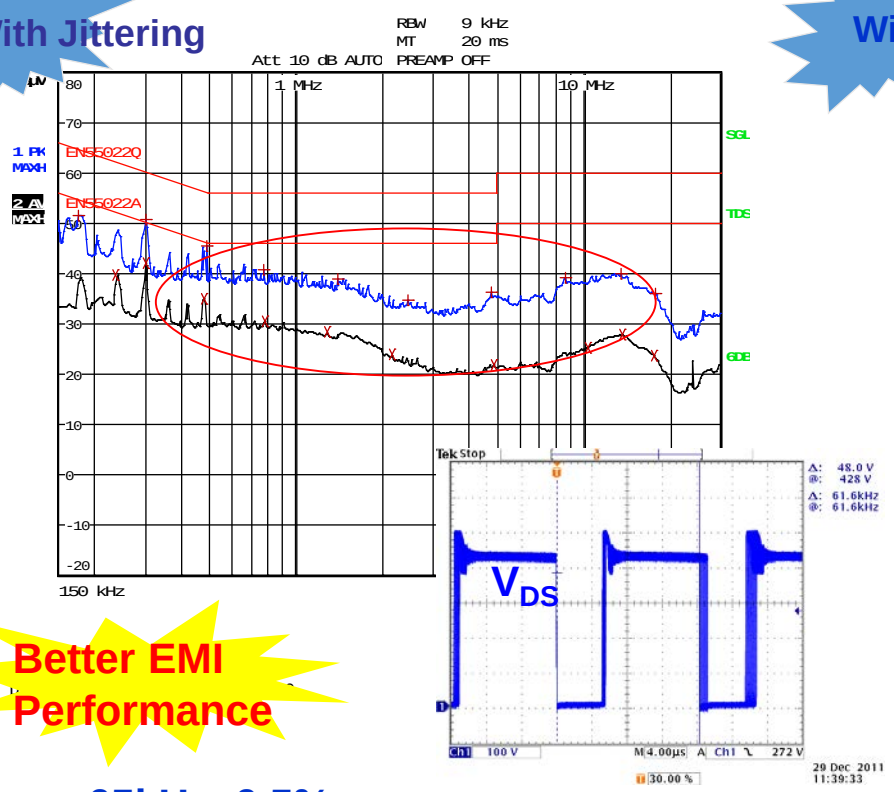


Converter keeps stable when duty cycle is larger than 0.5 in CCM.

Full Features Flyback Solution-HF500-X

➢ Frequency Jittering

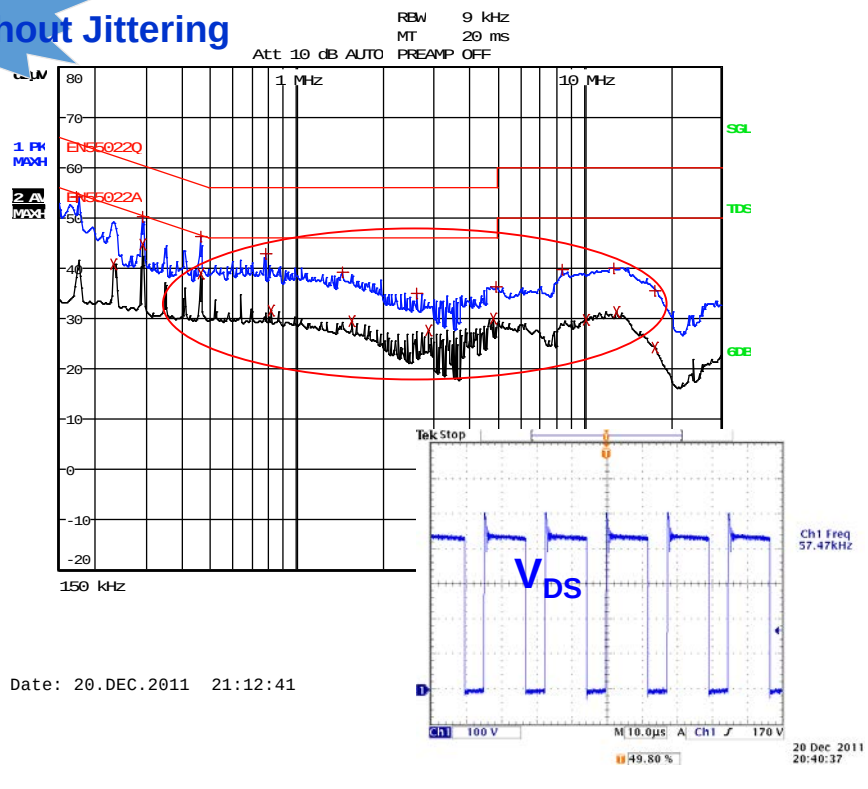
With Jittering



Better EMI Performance

65kHz±6.5%

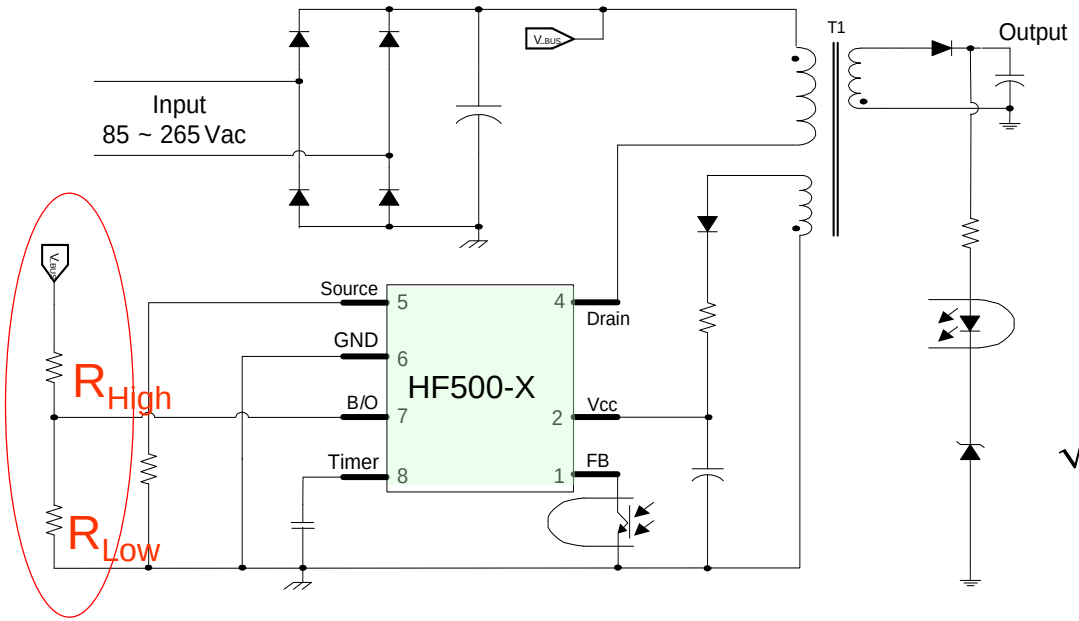
Without Jittering



Frequency jittering which leads to better EMI performance.

Full Features Flyback Solution-HF500-X

➢ Input Brown Out and OVP Function



$$\sqrt{2}\cdot V_{AC\_Min}\cdot\frac{R_{Low}}{R_{Low}+R_{High}} > V_{B/O\_In}$$

$$\sqrt{2}\cdot V_{AC\_Max}\cdot\frac{R_{Low}}{R_{Low}+R_{High}} < V\_OVP_{B/O}$$

By selecting the proper resistor divider, the input B/O and OVP can be realized by B/O pin.