Optimizing Capacitance in the Power Delivery Network for 5G Applications

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Introduction

When designing the power systems for 5G applications, designers must consider the wide range of frequencies intrinsic to such applications, from mid-range frequencies in the voltage regulators to high clock frequencies in the FPGA core. This end-to-end, full-duplex design is crucial in optimizing the performance of the power supply, power conversion, and power distribution processes.

This article focuses on how to achieve efficient power delivery network (PDN) design. The PDN is comprised of all the components connected to the voltage and ground rails, including the power and ground plane layout, passive components, ICs, and any other copper components that are connected or coupled to the main power rails. The parasitic behaviors of the components in the PDN must be considered during the design process as this impacts the overall system behavior.

The bypass and decoupling capacitors are essential components in the PDN. Capacitor selection and placement in the PDN design requires special consideration, as insufficient capacitance can lead to system instability and performance issues.

Importance of Decoupling and Bypass Capacitors

Bypass capacitors are used in voltage regulator modules (VRMs) to provide a low-impedance voltage source for the converter by filtering the input ripple current. They also compensate for potential ground bounce voltages generated by the switching noise from coupling the power supply to the IC ground connection.

At the buck voltage regulator's output, the main purpose of decoupling capacitors is to guarantee that the output voltage (V_{OUT}) remains constant by reducing the output voltage ripple (ΔV_{OUT}). The capacitance is therefore selected to limit ΔV_{OUT} to an amplitude set by the load input specification, while also considering limitations to voltage variations caused by sudden changes in the converter's load.

Placement Strategy for the Bypass Capacitor

The bypass capacitor is the most important element to ensure reliable buck converter operation. After the IC is placed, the bypass capacitor is the first component placed in the layout and must be routed immediately following IC placement. Additional parasitic inductance due to incorrect routing combined with the converter's switching can create excessive voltage spikes that may lead to IC failure.

Figure 1 shows the optimal placement of the bypass capacitors (CI21 and CI26) for the MPQ8655, a point-of-load (PoL) converter.

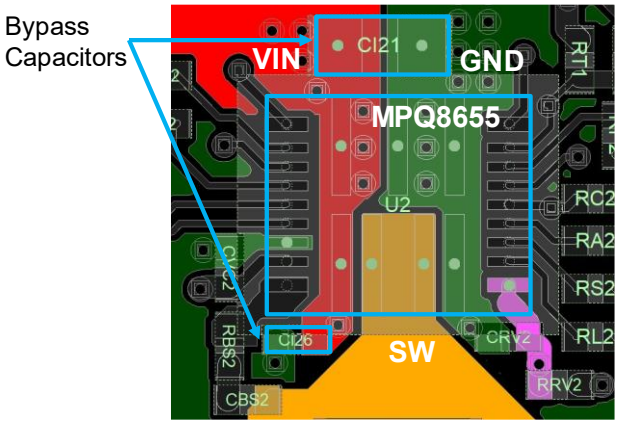

Figure 1: Bypass Capacitor Placement for the MPQ8655

The parasitic inductance created in the bypass capacitor loop can be divided into two parts: the parasitic inductance of the capacitor, and the inductance generated by the current path layout between the inductor and the IC. Since the inductance created by the PCB layout geometry is more significant relative to the total inductance than the inherent capacitor inductance, this is where design efforts should be focused. To minimize loop inductance, the bypass capacitors should be placed as close to the IC as possible. Vias should also be used to connect the capacitor's pad directly to the power (PWR) and ground (GND) nets as close to the IC pins as possible, which minimizes the current path.

Selecting the Decoupling Capacitors

The required type and number of decoupling capacitors depends on the behavior of the capacitors in the frequency domain. Decoupling capacitors are designed to minimize the VRM's ΔV_{OUT} that is generated by the converter's switching operation, as well as to supply instantaneous current to the FPGA/ASIC at high frequencies until the power supply can respond. As a result, the entire operating frequency spectrum must be considered.

The basic capacitor model includes three key elements: capacitance (C), equivalent series resistance (ESR), and equivalent series inductance (ESL) (see Figure 2).

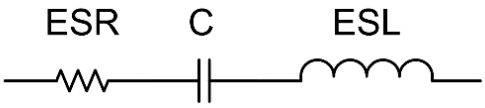

Figure 2: Capacitor Equivalent Circuit Model

ESR is caused by the impedance of the conductive elements in the component, and determines the minimum impedance at the resonance frequency. ESL is created by the effect of current flowing through the capacitor, and determines the resonance frequency. The resonance frequency is the point in the capacitor's impedance profile where the component starts behaving like an inductor, increasing in impedance proportional to the frequency.

At low frequencies (up to 50kHz), the buck converter has a low impedance. However, the buck converter's impedance at high frequencies is primarily inductive. Each capacitor added to the PCB reduces the PDN impedance at a given frequency, meaning accurate placement and selection enables realizing a set target impedance profile. Therefore, target impedances can be met at given frequencies by measuring from a sensing point.

The target impedance (Z_{TARGET}) can be calculated with Equation (1):

$$Z_{TARGET} = \frac{\Delta V_{NOISE}}{I_{TRANSIENT\_MAX}} \quad (1)$$

Where ΔV_{NOISE} is the maximum allowable ripple voltage, and $I_{TRANSIENT\_MAX}$ is the maximum load step that the converter must deliver. The required input and output capacitances can also be calculated.

To maintain the impedance below the target level, it is necessary to constrain the design and reduce the parasitic inductance. Bulk capacitors lower the impedance within a frequency range of up to 10MHz, whereas MLCC capacitors lower the impedance within the mid- to high-frequency range.

Figure 3 shows the impedance frequency characteristics of bulk and MLCC capacitors.

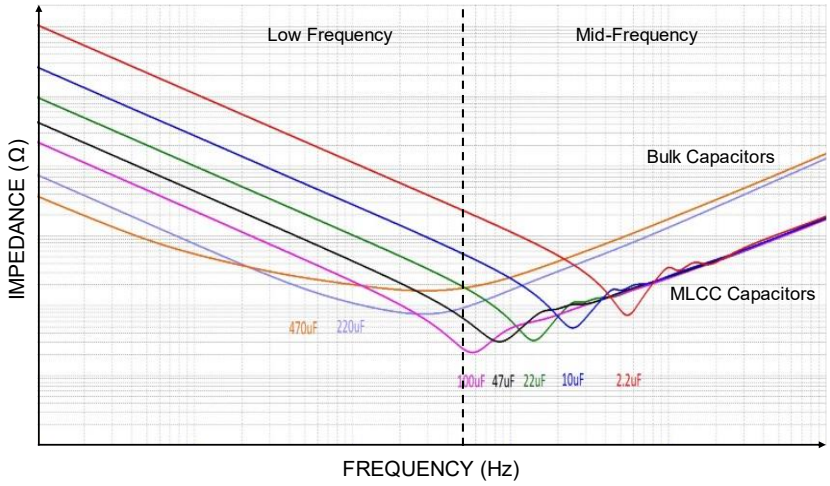

Figure 3: Impedance Frequency Characteristics of Typical Bulk and MLCC Capacitors

Placement Strategy for the Decoupling Capacitor

Once the capacitance is calculated and analyzed, the optimal placement of the decoupling capacitors in the PCB is important. The layout geometry, via placement, and distance mainly contribute to power plane loop inductance, which affects the PDN response. Figure 4 shows the current loops created by the converter, the decoupling capacitors, and the load. Since these loops are intrinsic to the structure and unavoidable, it is crucial to minimize these loops as much as possible.

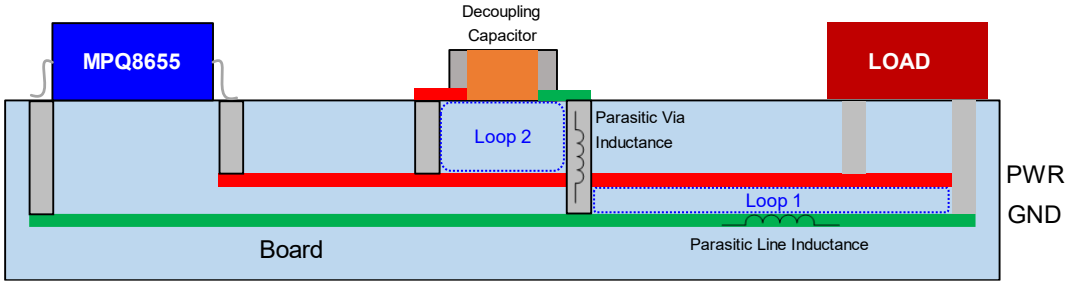

Figure 4: Loop Inductance of the Decoupling Capacitor Due to Layout Geometry, Distance, and Vias

Loop 1 is the horizontal loop component, and is determined by the distance between the converter (the MPQ8655) and the decoupling capacitor. Loop 2 is the vertical loop component, and is determined by the via height that connects the capacitor to the power plane. The power plane is typically placed on the innermost layer(s) of the PCB.

The test board uses two MPQ8655 devices in dual-phase operation, with a V_{OUT} of 0.9V and a maximum output current (I_{OUT_MAX}) of 50A, which are generic values for ASIC/FPGA power rails. Simulations of different scenarios can be conducted using the test board to determine the optimal placement of the capacitors.

To assess the optimal capacitor placement, the impedance is measured at the board-level sensing point in the ASIC/FPGA center. Using the analysis from Equation (1), the VRM impedance profile can be realized using 8 x 22µF MLCC capacitors and 2 x 220µF bulk capacitors. To maintain the voltage regulator's stability, the bulk capacitors are placed immediately after the output inductor. The test board considers different placements of the 22µF MLCC capacitor with Case 1a and Case 1b (see Figure 5).

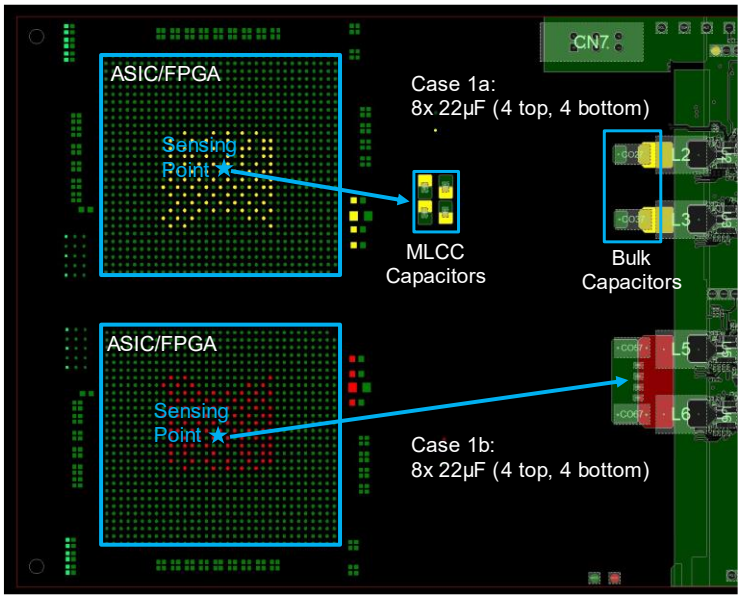

Figure 5: Decoupling Capacitor Placement

In Case 1a, the MLCC capacitors are placed immediately before the ASIC/FPGA, reducing the size of Loop 1. In Case 1b, the MLCC capacitors are placed next to the bulk capacitors, resulting in twice as much a distance between the MLCC capacitor and the sensing point compared to Case 1a.

Figure 6 shows the simulation results of placing the bulk capacitor close to the buck converter, which results in reduced impedance in the low-frequency range (green trace). Placing the MLCC capacitors close to the load (red trace) reduces the impedance in the high-frequency range, allowing the capacitors to deliver the instantaneous current steps required by the FPGA/ASIC load more effectively.

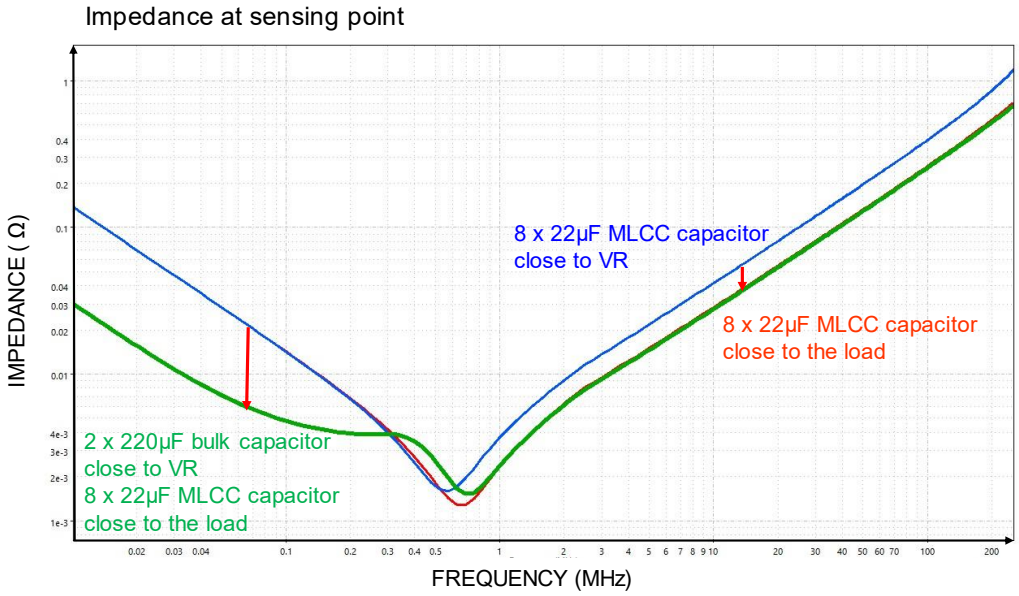

Figure 6: Test Results for Variations in Loop 1 Size (Decoupling Capacitor Placement)

Traditional design guidelines recommend placing the decoupling capacitors on the bottom side of the PCB under the IC in an attempt to reduce the board space, which increases the power density. However, placing the capacitors on the bottom of the board requires longer vias to reach the opposite side where the ASIC/FPGA is located. This increases the size of the vertical path, shown in Figure 4 as Loop 2.

An additional test was conducted by doubling the height of the vias to analyze the effect of increasing the size of Loop 2. Figure 7 shows the test results for variations in the size of Loop 2, where similar trends are observed, with increased via height resulting in increased impedance in the mid- to high-frequency range.

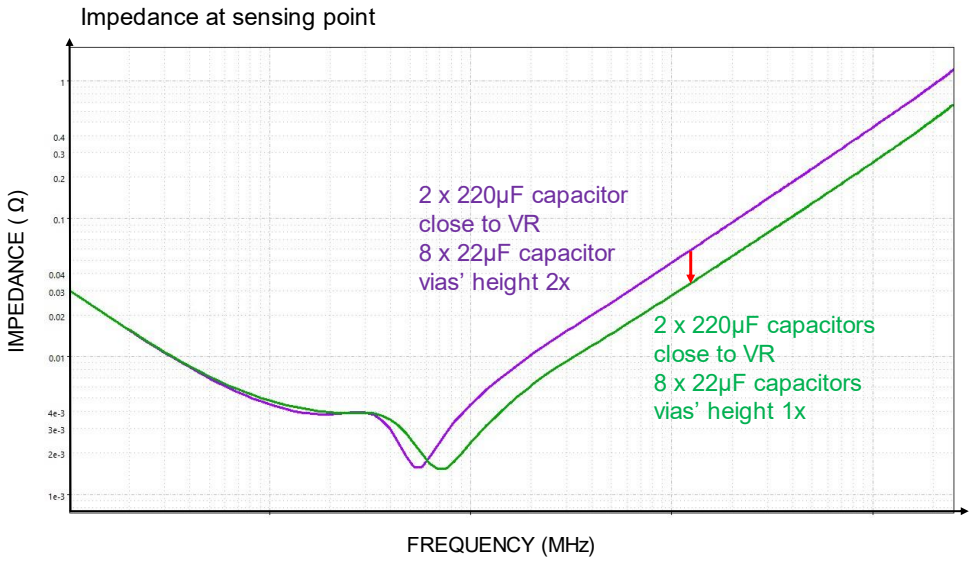

Figure 7: Test Results for Variations in Loop 2 Size (Increased Via Height)

Minimizing loop inductance in the decoupling capacitors is equally important as the capacitor quantity. There are two methods to achieve reduced loop inductance. The first method is to decrease the horizontal distance between the IC and the capacitor. The second method is to reduce the via height by placing the power and ground planes in the upper layers.

Placing multiple components in small areas to reduce board space often leads to capacitors sharing vias. When capacitors share vias, the overall improvement from proper capacitor selection and positioning may be significantly reduced or even negligible if via positioning and quantity is not considered. As such, via layout design is also key to reducing loop impedance.

To analyze the impact of via positioning and quantity, a second test was conducted using the board via placement of two general design recommendations. In the first set-up, each capacitor has its own set of vias to the power and ground planes (see Figure 8).

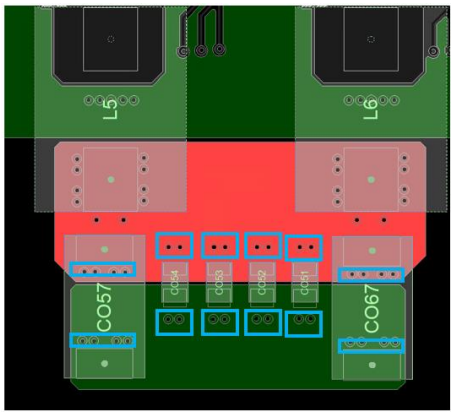

Figure 8: Optimal Capacitor Via Placement

In the second set-up, all the capacitors share a set of vias placed on one side of the plane (see Figure 9).

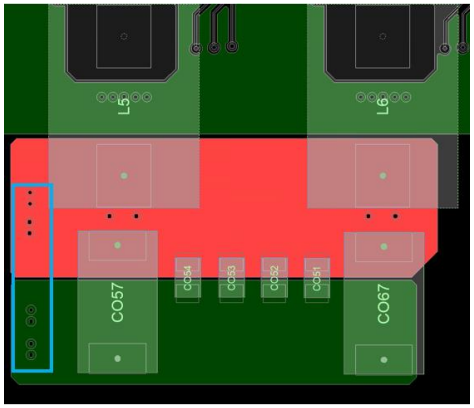

Figure 9: Sharing Vias between Several Capacitors

Figure 10 shows the test results for variations in via placement. Placing the vias away from the capacitors increases the size of Loop 1, increasing loop inductance. Thus, via sharing increases high-frequency impedance.

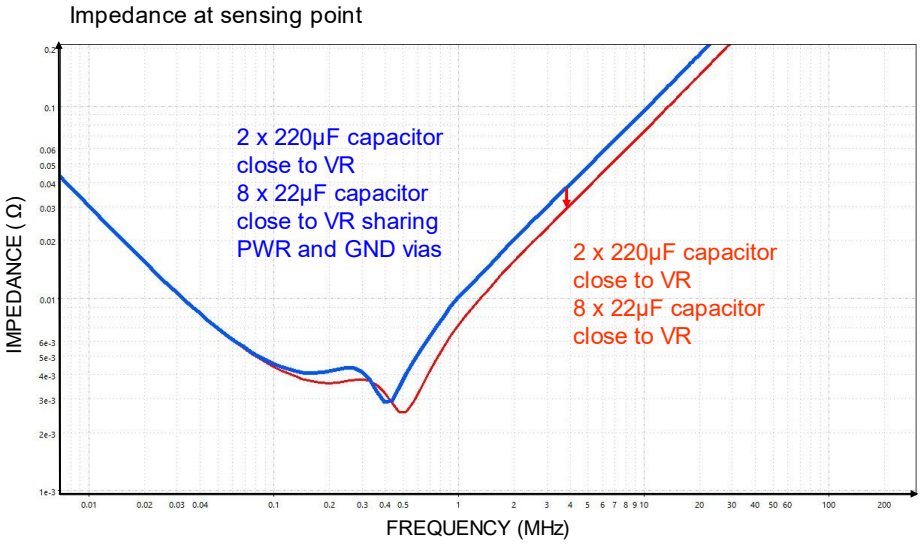

Figure 10: Test Results for Variations in Via Placement

From subsequent tests, it is recommended to use at least four power and four ground vias for the bulk capacitors, and at least two power and two ground vias for the MLCC capacitors, in both 0805 and 0603 packages. The vias should be placed as close to the capacitor as possible.

Conclusion

When designing an FPGA/ASIC system or any circuit requiring high currents and fast load transients, it is crucial to consider the PDN in its entirety to optimize system performance. Fast load steps, such as those observed in FPGAs, incur powerful high-frequency currents throughout the circuit. At such high frequencies, parasitic elements in the PDN that can typically be disregarded may suddenly cause the device to malfunction. Designers must take care to ensure that the PDN's parasitic components are minimized.

This article focused on reducing the parasitic impedance caused by the current path in the VRM's decoupling capacitors using the MPQ8655. For optimal performance, the current loops should be kept as short as possible in both the vertical and horizontal axes. Placing the current loops as close to the load as possible and keeping the power traces on the outer layers effectively reduces via length. Proper via placement is also key to reducing parasitic inductance. It is recommended to place several vias as close as possible to each of the capacitor's pads to reduce the total parasitic inductance of the vias, as well as the current flowing through each via.

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