5G基站电源关键技术与解决方案

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  - 5G网络架构与基站规划
  - 5G基站电源架构
- 5G基站电源设计的关键技术
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  - “动”与“静”
  - “短”与“长”
- MPS电源模块产品介绍
- 5G电源基站中的实际案例

5G 基站架构和电源需求综述

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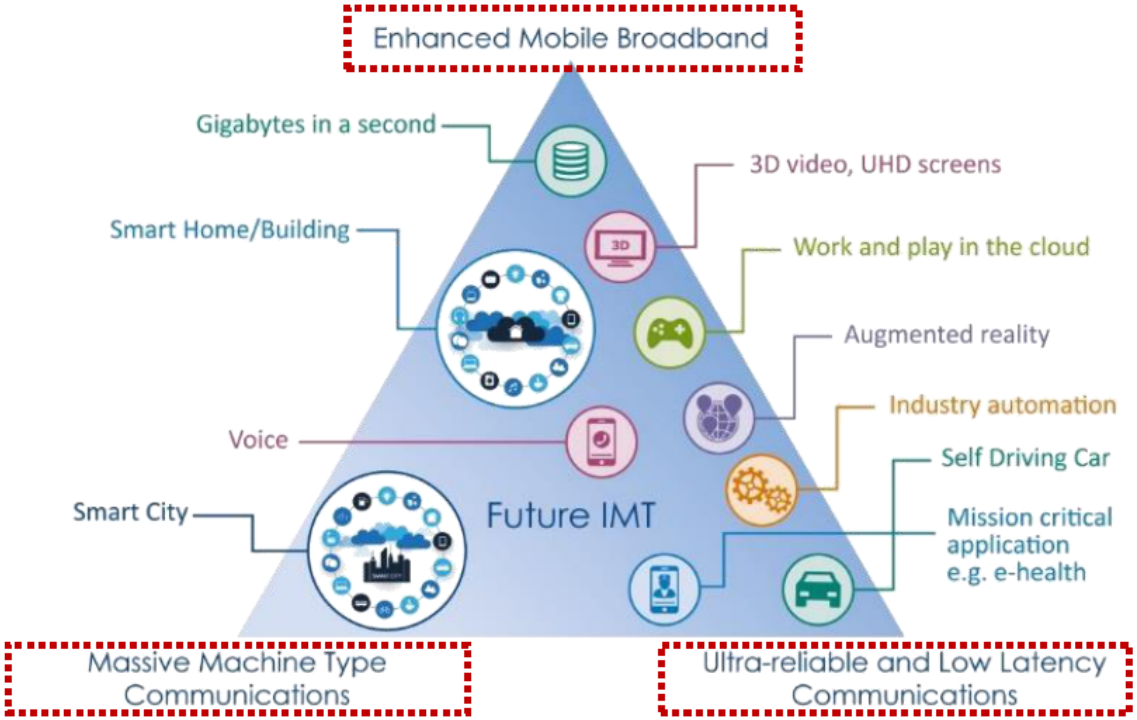
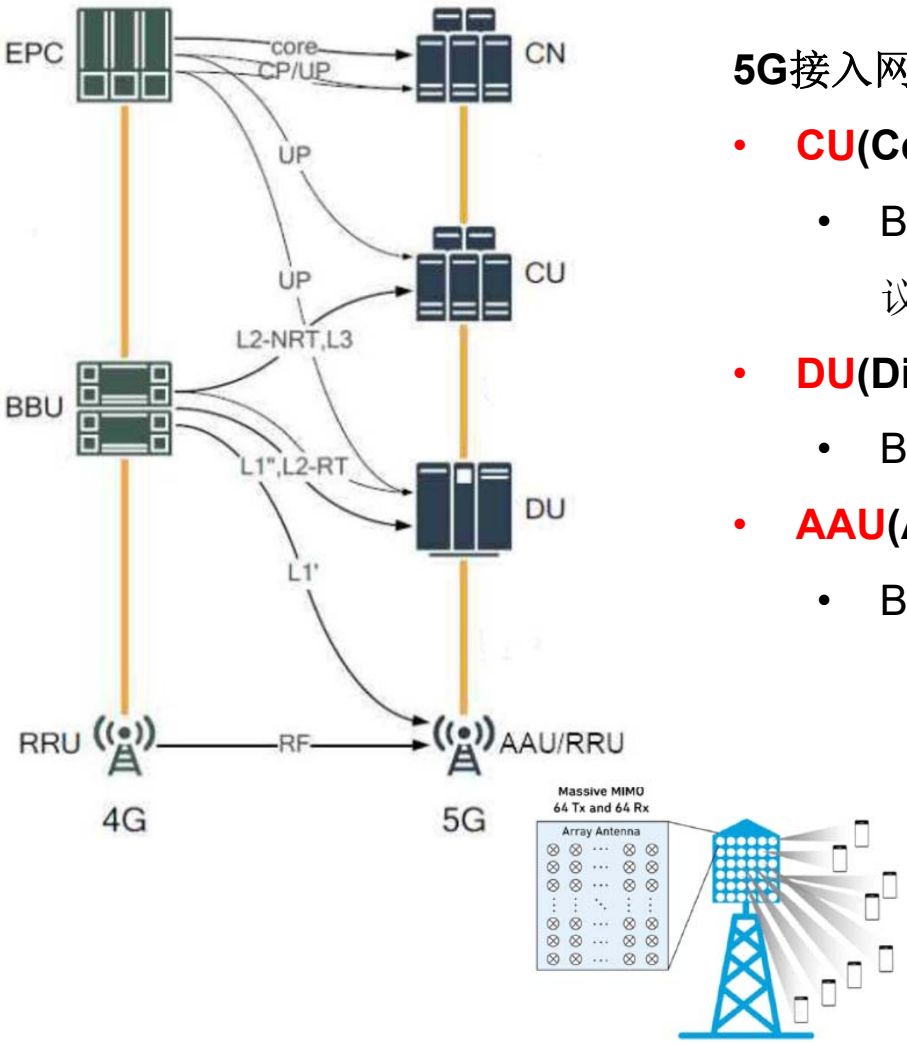
5G三类典型业务场景

5G三大特点	应用场景
eMMB--增强型移动宽带	超高清视频、虚拟现实（VR）/增强现实（AR)
mMTC--大规模机器类通信	智慧城市，智能家居等物联网应用
uRLLC--超可靠低时延通信	工业控制，无人机控制，智能驾驶控制



Network	Traffic Density	Connection Density	Latency	Mobility	Experienced Rate	Peak Rate
4G	0.1Mbps/m2	100K/km2	10ms	350km/h	10Mbps	1Gbps
5G	10Mbps/m2	1M/km2	1ms	500km/h	100M1Gbps	20Gbps

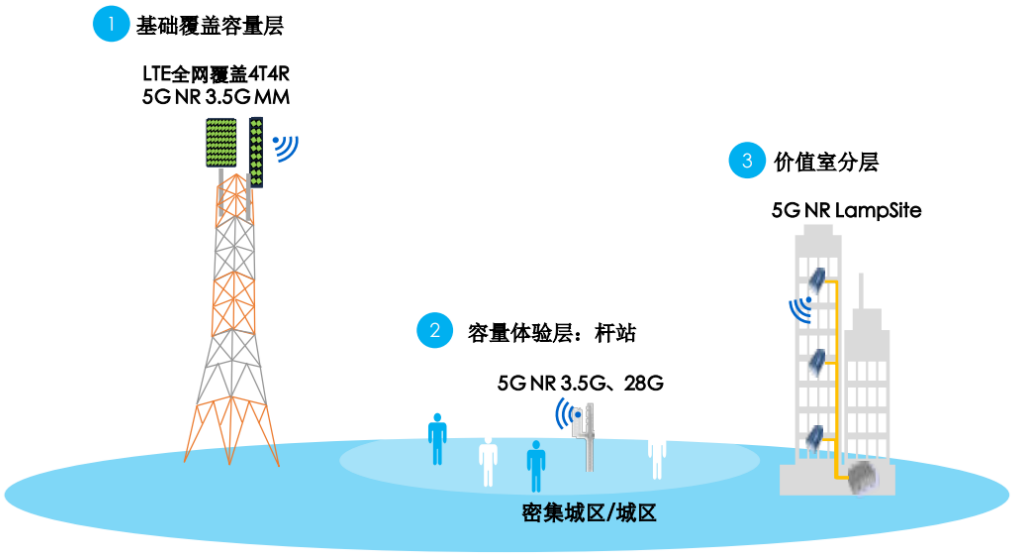
5G 接入网 (RAN, Radio Access Network)



5G接入网的三个功能实体：

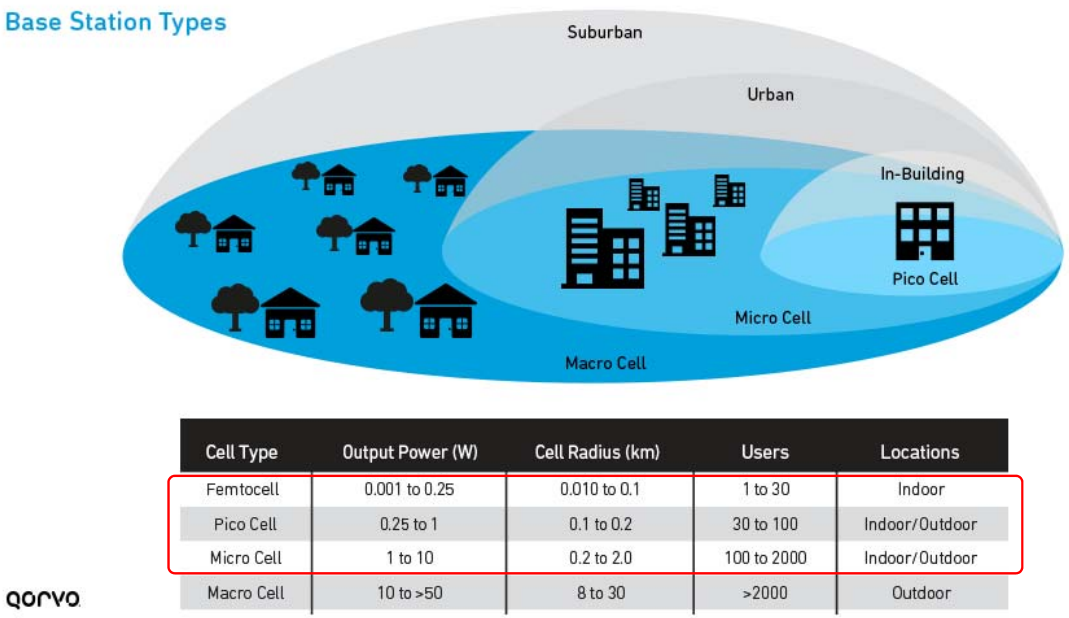
- **CU(Centralized Unit,集中单元)**
  - BBU的非实时部分将分割出来，重新定义为CU，负责处理非实时协议和服务
- **DU(Distribute Unit,分布单元)**
  - BBU的剩余功能重新定义为DU，负责处理物理层协议和实时服务。
- **AAU(Active Antenna Unit,有源天线单元)**
  - BBU的部分物理层处理功能与原RRU及无源天线合并为AAU。

5G 三层立体组网



- **基础覆盖容量层（底层网）：**
  - 以宏站为主的连续覆盖和容量网络
  - 应用于室外普遍的业务承载
- **容量体验层（中层网）：**
  - 以杆站等简易站为主的非连续覆盖和容量网络
  - 应用于道路，高层建筑，居民区， 大型集会，风景区等
- **价值室分层（室内覆盖）：**
  - 以室内数字化为主的室内价值建网
  - 应用于CBD，交通枢纽、商场等大型建筑室内场景

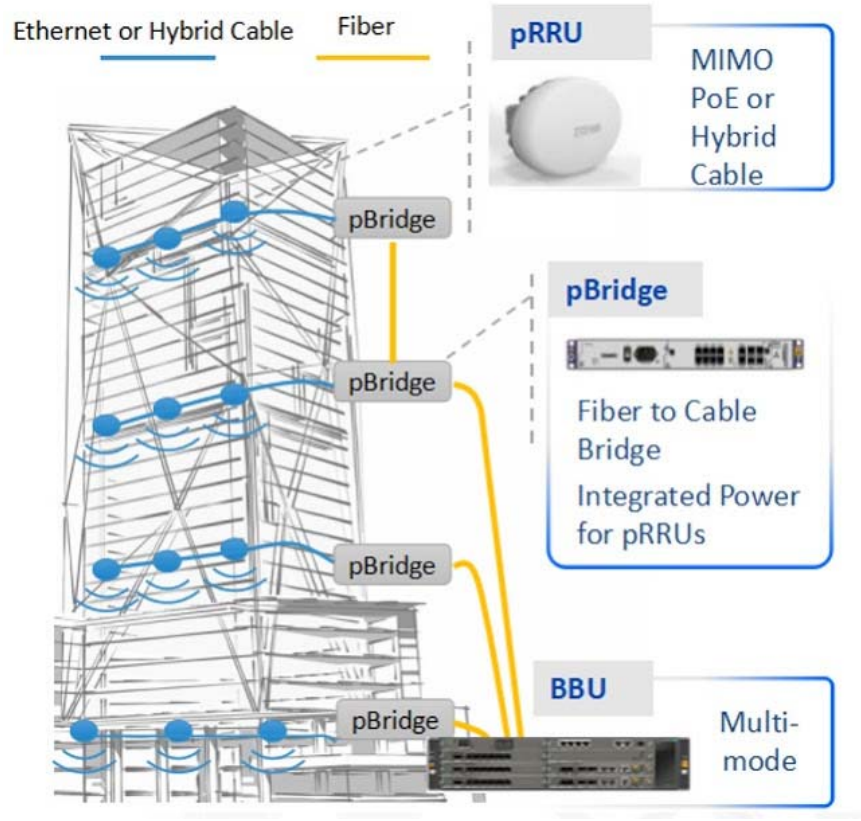
5G 小基站



Cell Type	Output Power (W)	Cell Radius (km)	Users	Locations
Femtocell	0.001 to 0.25	0.010 to 0.1	1 to 30	Indoor
Pico Cell	0.25 to 1	0.1 to 0.2	30 to 100	Indoor/Outdoor
Micro Cell	1 to 10	0.2 to 2.0	100 to 2000	Indoor/Outdoor
Macro Cell	10 to >50	8 to 30	>2000	Outdoor

qorvo

Small Cell根据覆盖范围的大小依次分为Microcell、Picocell和家庭Femtocell，通常覆盖10米到几百米的范围。 Small Cells的使命是不断补充宏站的覆盖盲点和容量，以更低成本的方式提高网络服务质量。



QCell - ZTE's 5G Solution for Gigabit Indoor User Experience
https://www.telecomsinfrastructure.com/2020/06/qcell-ztes-5g-solution-for-gigabit.html

未来几年的5G规划

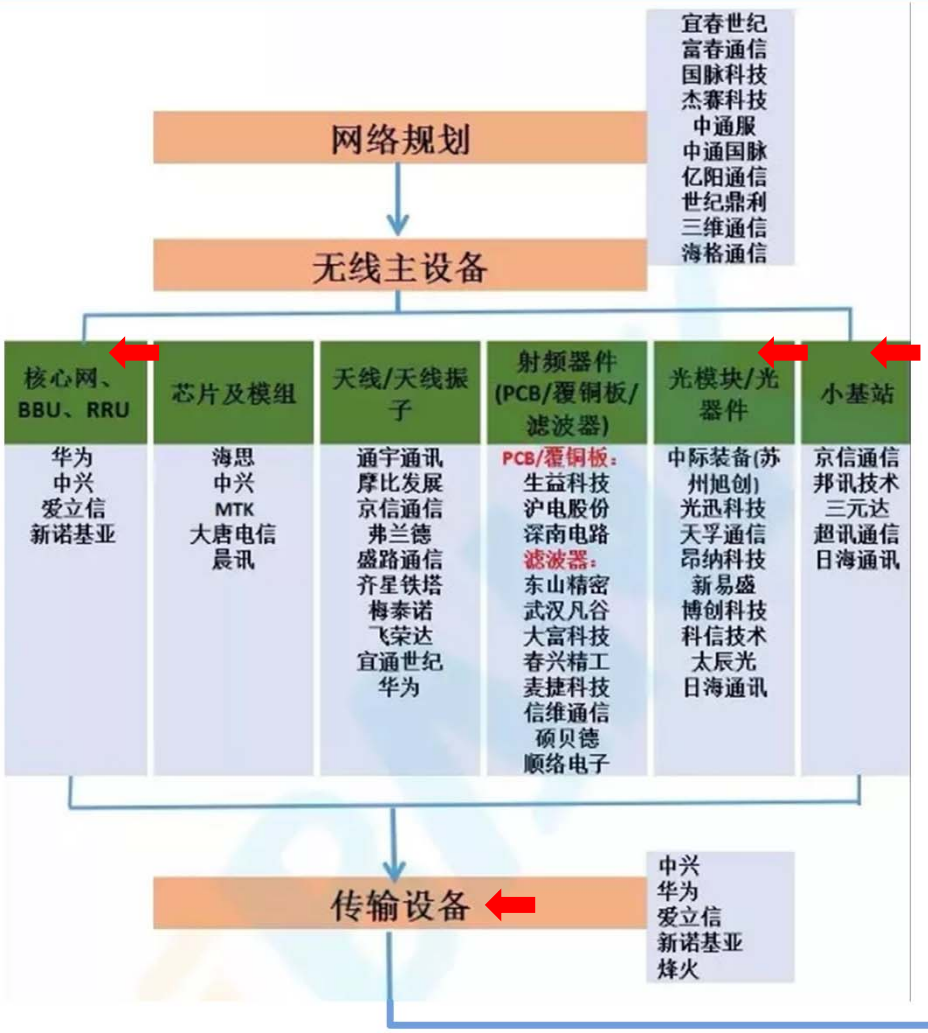
5G宏站与小站预估数量（万站）

5G的无线接入将实现中低高频段的全频谱接入.

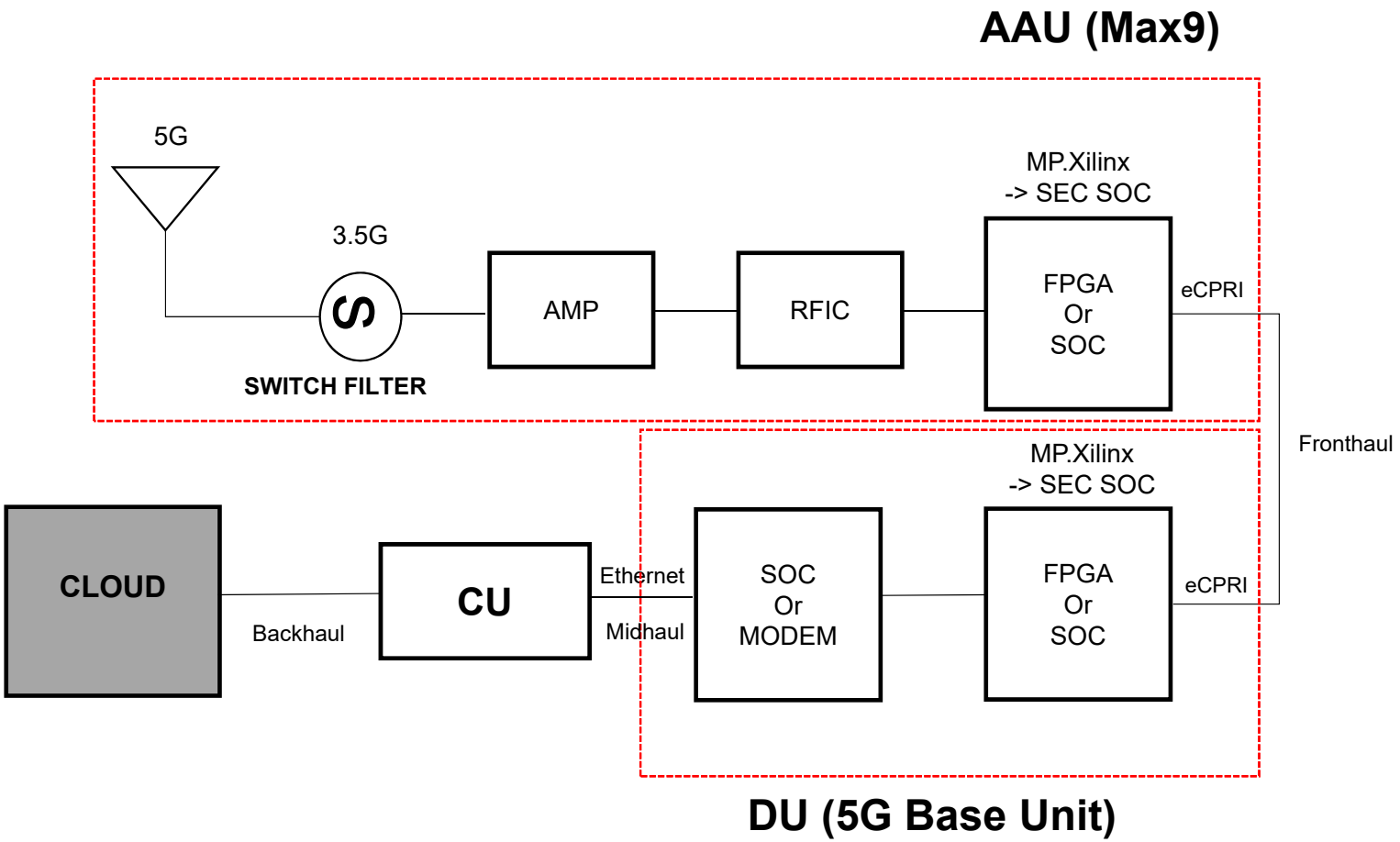
- **中低频段将提供连续性覆盖**
  - 5G 宏站数量为4G的1.2倍，达到320万个
- **毫米波高频段将作为热点区域或容量提升的覆盖。**
  - 毫米波高频段的小站数量保守估计将是宏站的2倍多，5G小站将达到640万个。

5G通讯产业链

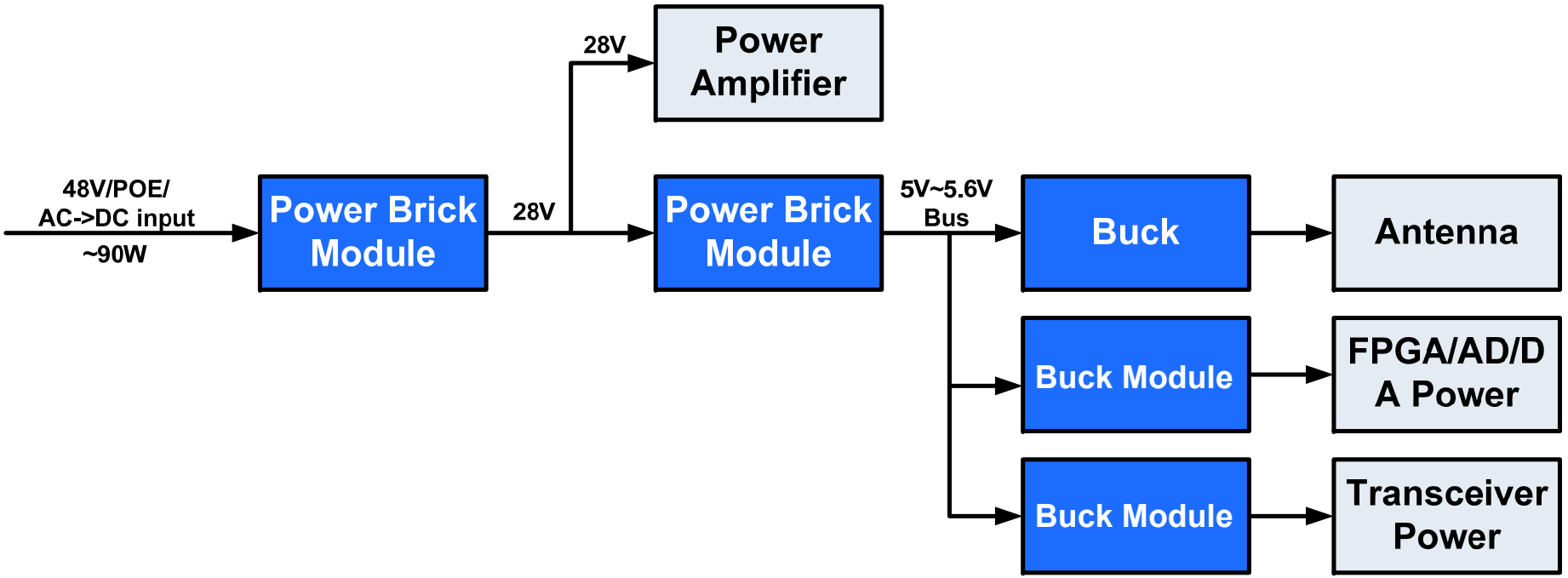
MPS电源模块提供的解决方案



5G CU/DU/AAU 系统架构



5G 小基站AAU 电源架构



5G基站电源设计的关键技术 – “大”与”小”

功耗“大”，体积“小”

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5G基站整机功耗大

从4G演进到5G，单位流量的功耗（Watt/Bit）大幅降低，但5G功耗相比4G大幅增长。预计在5G 时代，64T64R AAU最大功耗将会达到1000~1400W，BBU最大功耗将达到2000W左右。 5G时代，一站多频将是典型配置。预测5频以上站点占比将从2016年3%增加到2023年45%。一 站多频将导致整站最大功耗超过10kW，10频及10频以上站点功耗超过20kW，多运营商共享场景 下，功耗还将翻倍。

小基站AAU的功耗也将达到65W以上。对于一体型小基站，功耗会更大。

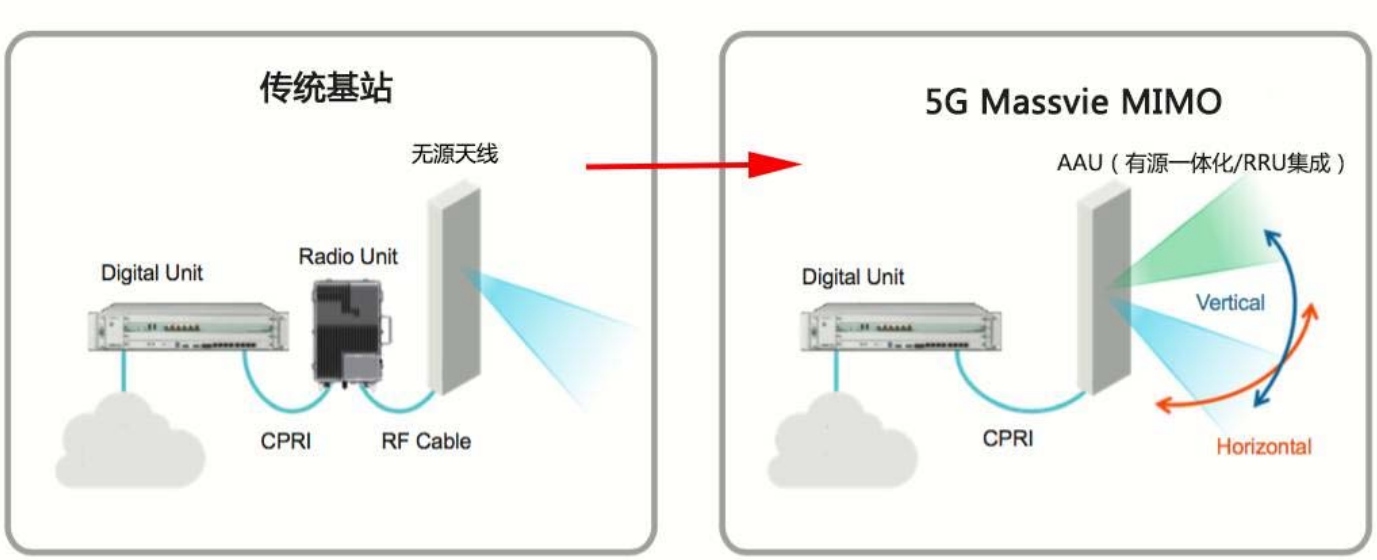
PA热耗: 65%

TRX热耗：15%

滤波器热耗：10%

一次电源热耗：10%

5G基站设备体积小



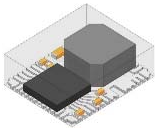
Huawei Lampsite

ZTE QCell

Ericsson Radio Dot

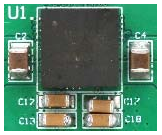
5G宏站与小基站，设备体积要远离以往的笨重粗犷，特别像室内场所的小基站又有外观要求，轻巧的体积外形是主流

电源模块为什么可以做的那么小？

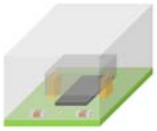


1. 单晶圆的功率+控制减小了芯片的面积

2. 倒装的封装工艺减小了芯片的占板面积



3. 提高开关频率减小电感体积

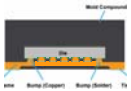


4. 电感/芯片的3D封装进一步提高功率密度

5. 多路输出模块减小了整体方案占板面积

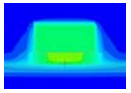
MPS电源模块独特设计帮助了散热

优化模块设计，减小功耗

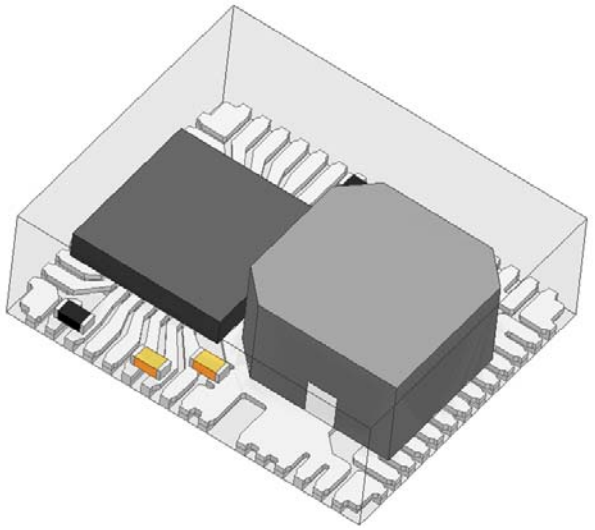


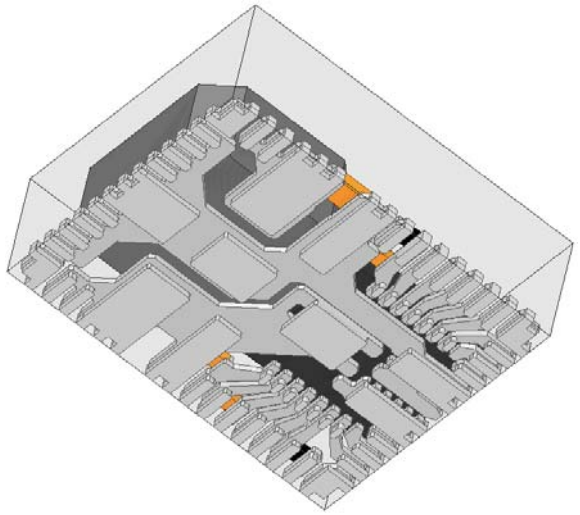
芯片倒装工艺降低了热阻

低高度的模块设计可以和主芯片共用散热器



3D封装帮助散热更加均匀

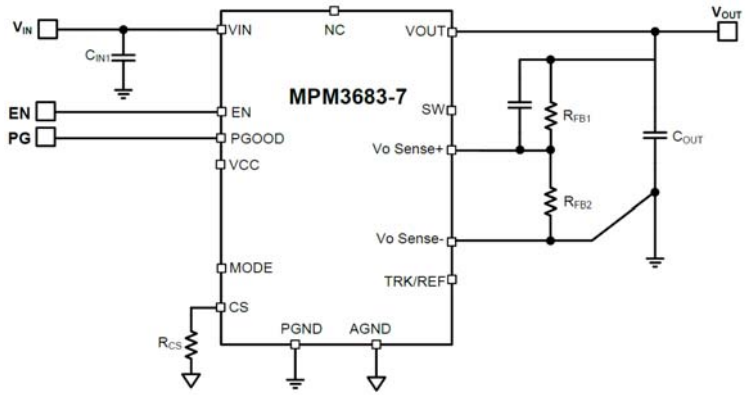


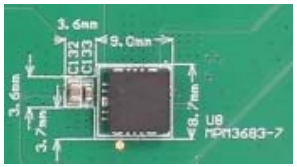


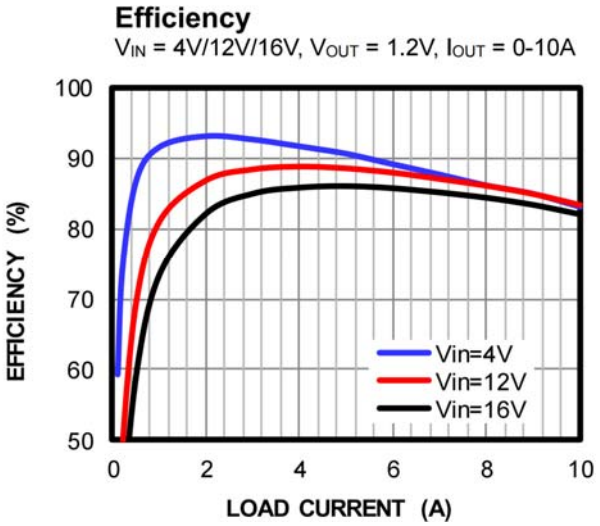
MPM3683-7 16V 8A Module in 7x7x4mm

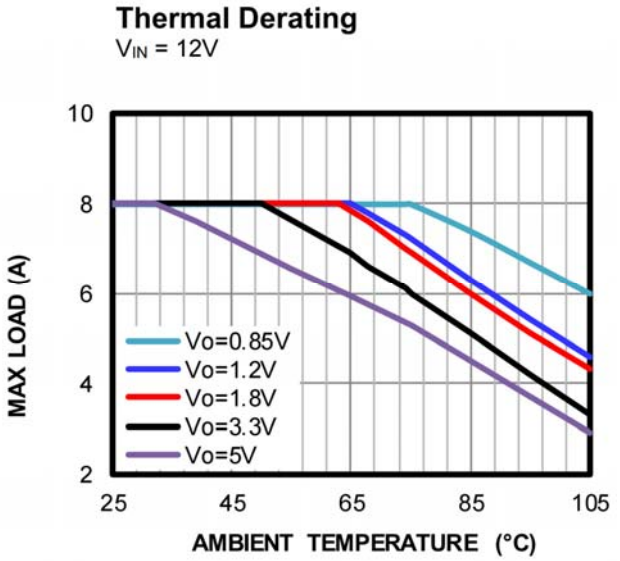
FEATURES

- 2.7V to 16V Input Range
- 0.6V to 5.5V Output Voltage
- Continuous 8A, peak 12A
- 3D QFN Package
- Remote Output Voltage Sensing
- ±1% Total Output Voltage Regulation
- COT for Ultra Fast Transient
- 89% Peak Efficiency 12V->1.2V
- 7x7x4mm QFN Package
- 600k/800k/1MHz FSW
- Selectable Soft-Start, CCM/DCM









5G基站电源设计的关键技术 – “多”与“少”

电源路数“多”，占板面积“少”

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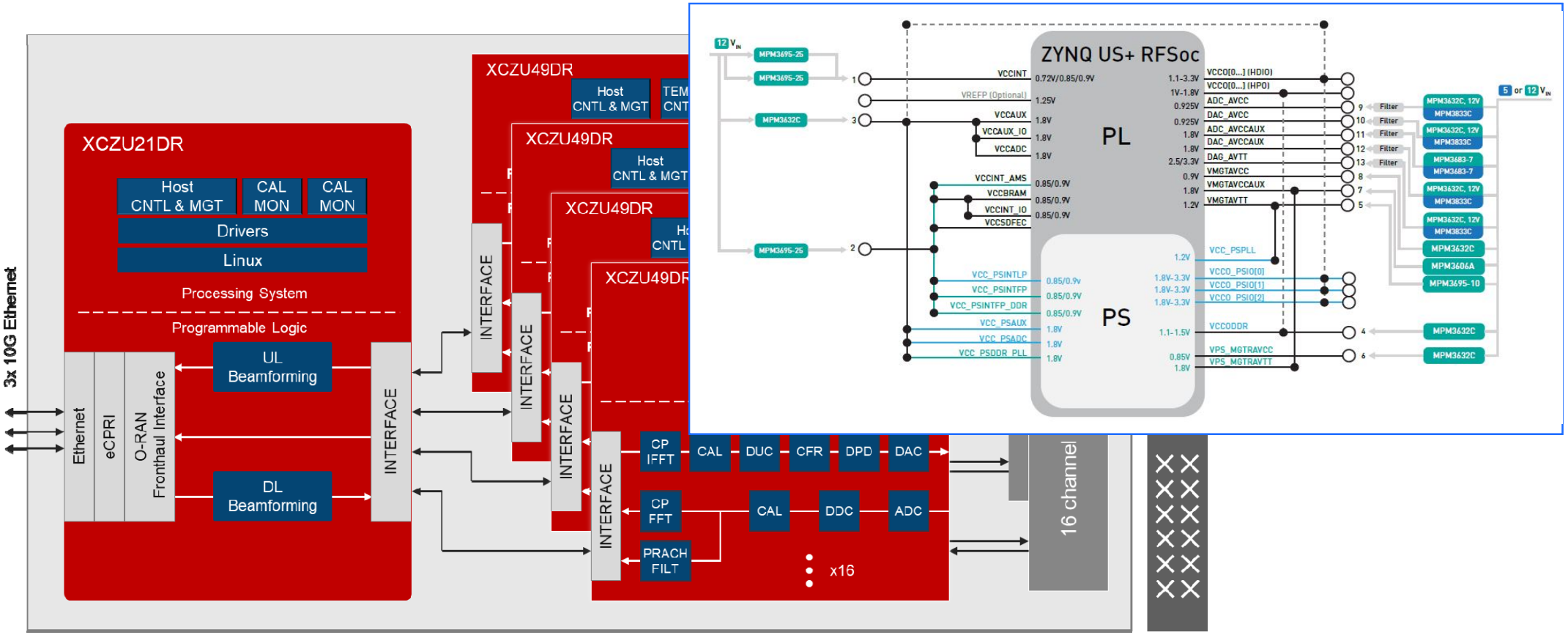
5G宏站RU Xilinx设计方案



- 64T/64R宏站AAU需要的POL电源多达60路以上
- 2T/2R小基站需要的POL电源也在10路以上

电源占板面积需要更“小”一些

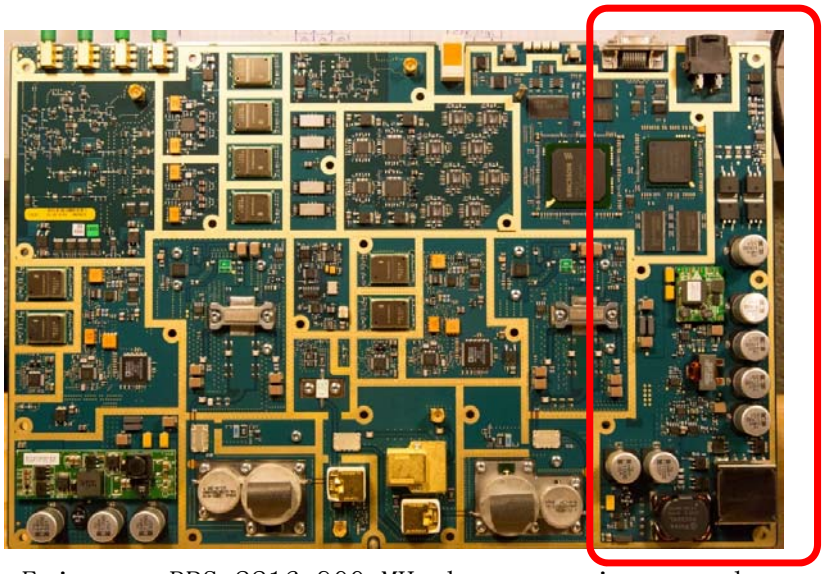
宏基站AAU

Microcell 抱杆

室内Nano Cell

室内Fetto Cell

www.qorvo.com



Ericsson RBS 2216 900 MHz base station teardown
http://kaizerpowerelectronics.dk/teardown/ericsson-rbs-2216-900-mhz-base-station-teardown/

- 基站小型化的趋势和外观的要求
- 减小负载点电源（POL）占板面积
- 减小开关电源高噪声环路对信号线布局的影响

5G基站电源设计的关键技术 – “短”与“长”

产品设计周期“短”，运行寿命“长”

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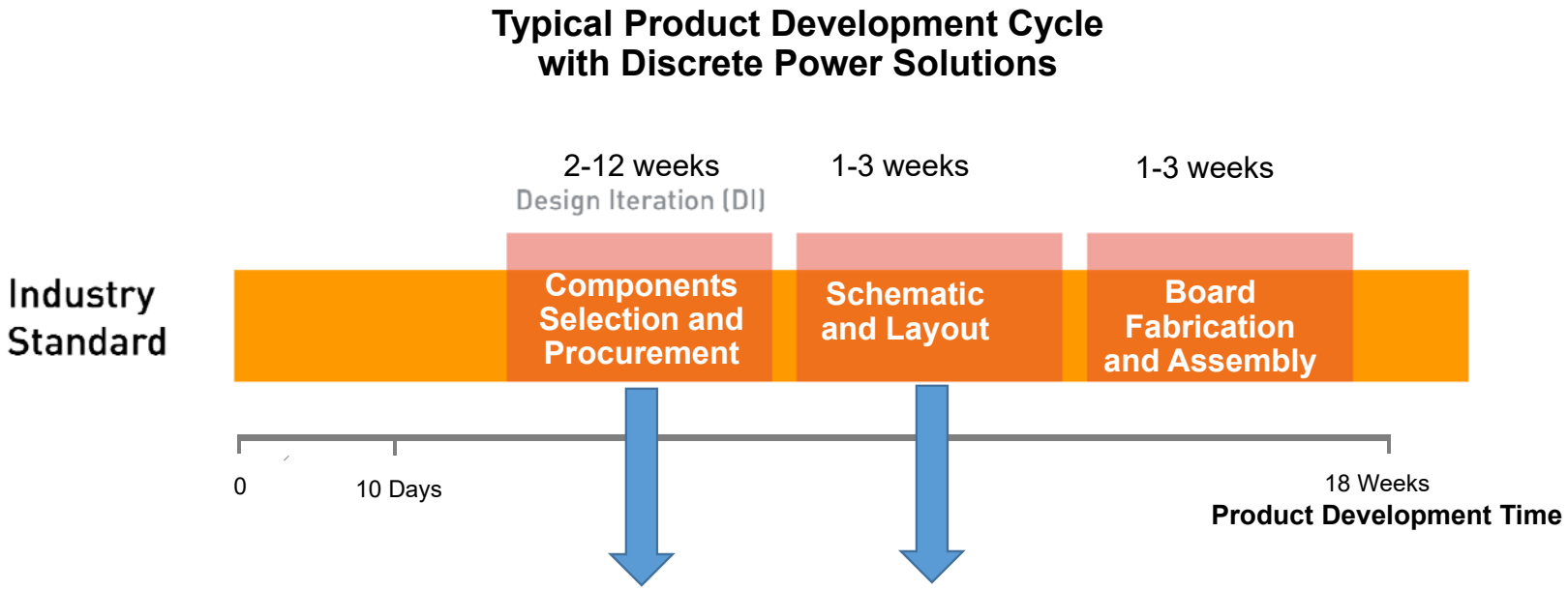
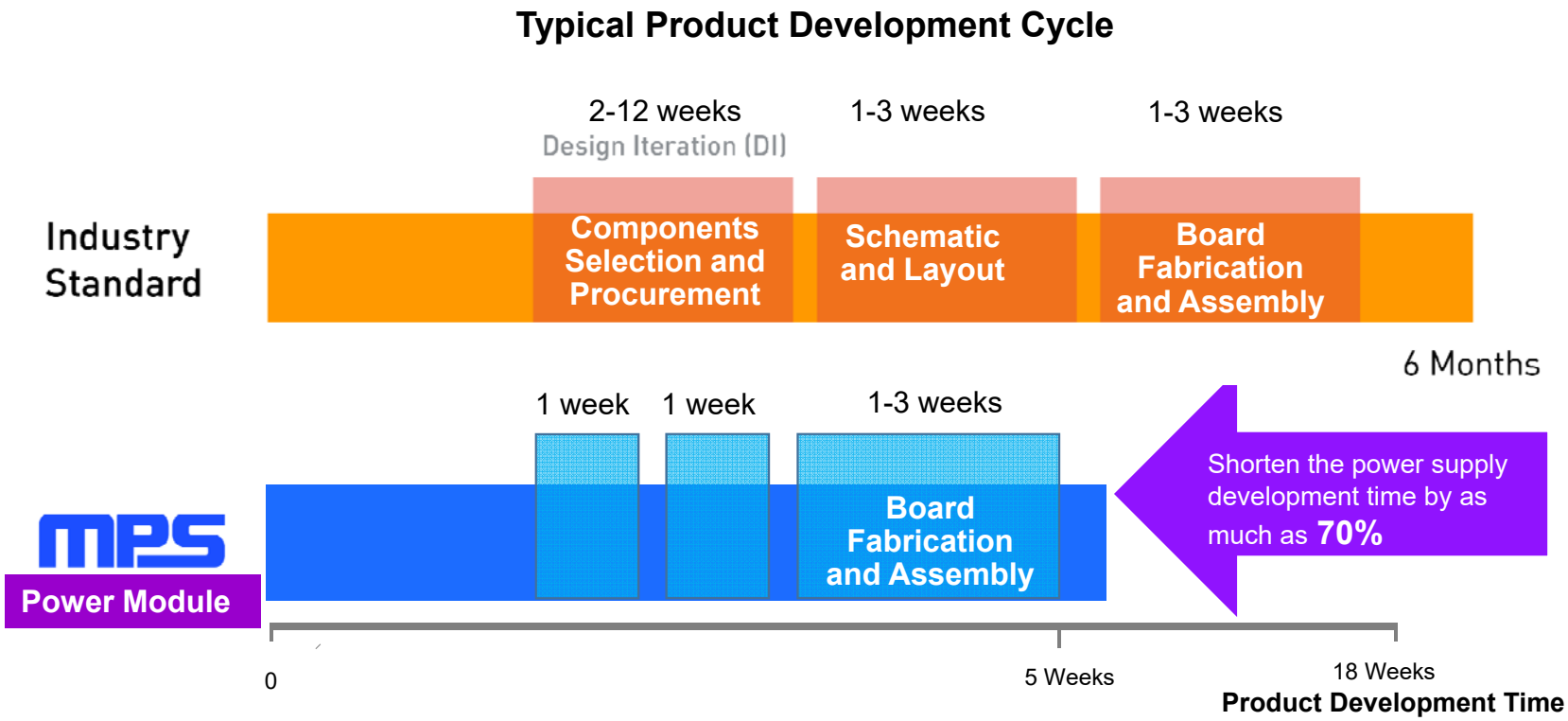
开发验证分立电源方案往往需要18周以上的周期



- 需要优化挑器件，包括芯片，电感等
- 需要根据电感/电容选择合适的环路补偿
- 复杂的原理图以及PCB布线
- PCB布线的风险，有可能需要多次制板验证

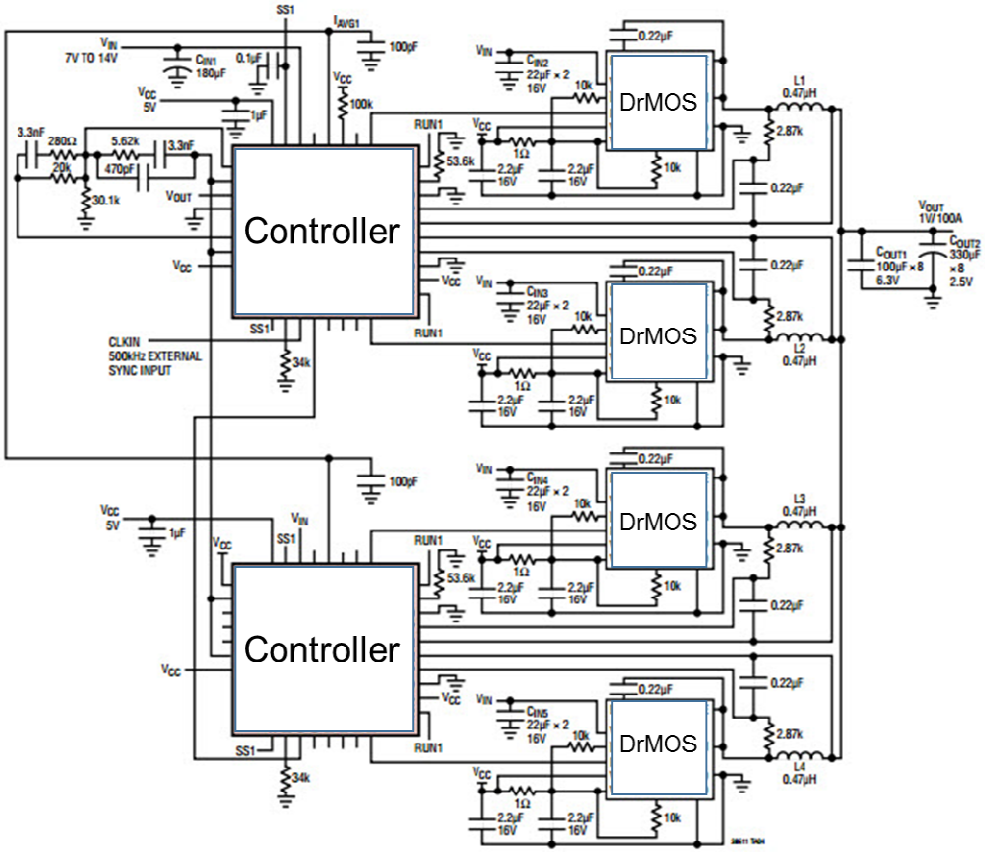
电源模块极大的缩短的开发周期



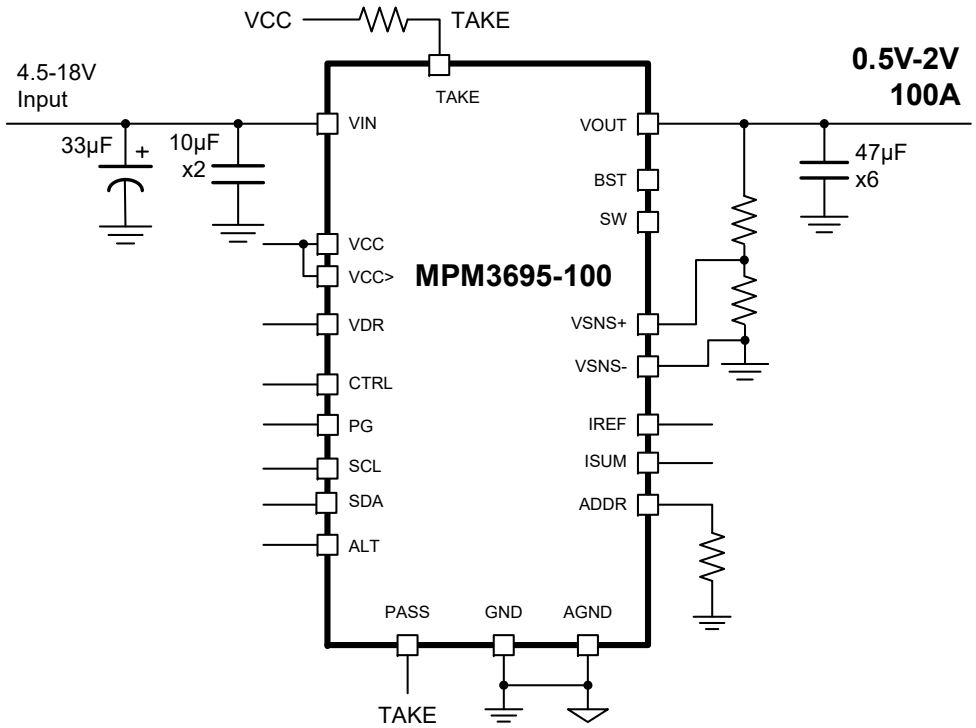
- 电源模块提供了高集成度的方案
- 优化的性能
- 大大简化的原理图和PCB布板
- 极少的外围元器件

电源模块简化了设计的复杂度 – 100A设计举例

100A分立方案（Controller+DrMOS）典型应用图

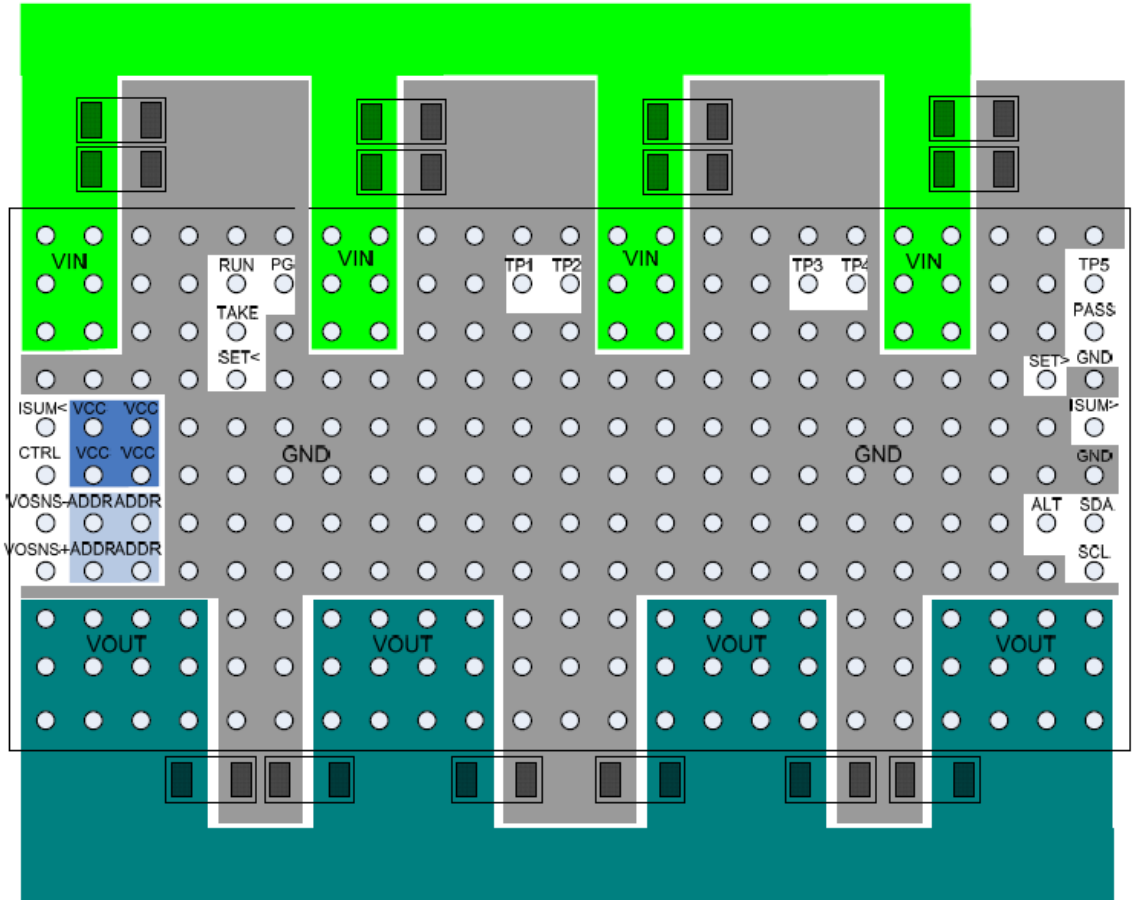


MPS 100A模块典型应用图



电源模块简化了PCB布板的风险以及复杂度 – 100A设计举例

实例: **MPM3695-100, 带PMBus，可并联的100A电源模块，15x30x5.3mm BGA封装**



- 模块集成了控制器，功率**MOSFET**，电感以及滤波电容
- 外围仅需输入输出电容
- 及其简单的**PCB**布线
- 优化的模块管脚分布

MPS电源模块的质量管控和高可靠性

- Mature/High-Quality MPS parts inside.
- Overall FIT rate<0.2 fits.
- High-Quality Fabrication Control.

  3,079 lots/1,078,356pcs passed MPS STRM(3*Reflow+TCC96+AC48)

	ABBR	SPEC	Device Hours or Cycles
Temperature, Bias, and Operating Life (125°C for standard and 150°C for automotive)	HTOL	JESD22-A108	32,045,000
Accelerated Moisture Resistance- Unbiased Autoclave(121°C/100%RH)	AC	JESD22-A102	12,758,304
High Temperature Storage Life(150°C)	HTSL	JESD22-A103	784,687,000
Temperature Cycling(-65°C~150°C)	TC	JESD22-A104	42,828,000
Board Level Temperature Cycling(-45°C~125°C)	BLTC	IPC9701	5,220,700
Highly Accelerated Temperature and Humidity Stress Test (130°C/85%RH)	HAST	JESD22-A110	3,187,388
Steady State Temperature Humidity Bias Life Test(85°C/85%RH)	THB	JESD22-A101	5,104,000

5G基站电源设计的关键技术 – “动”与“静”

“动”态响应快，安“静”的低噪声电源

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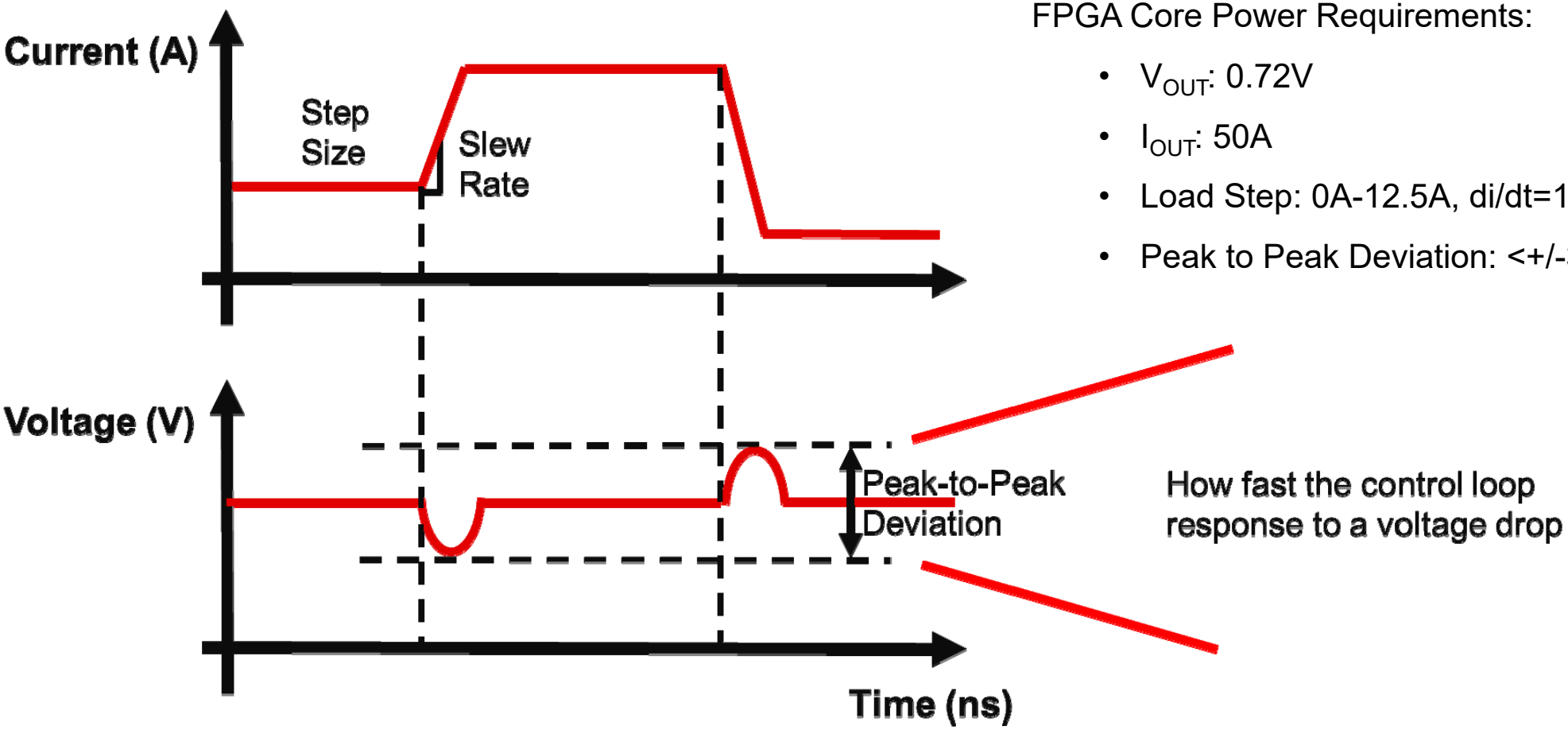
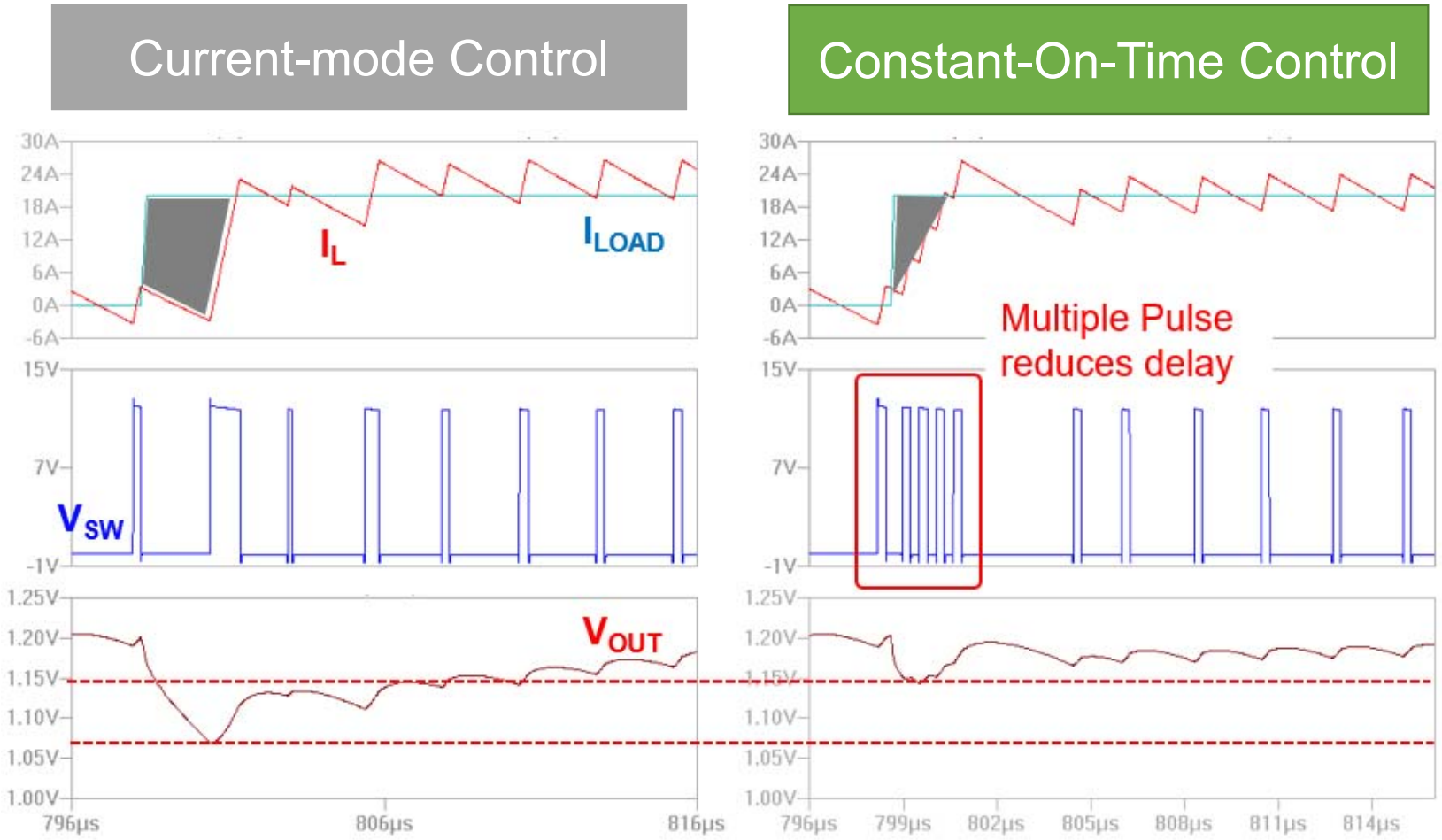
FPGA/ASIC 要求供电动态响应快



FPGA Core Power Requirements:

- V_{OUT}: 0.72V
- I_{OUT}: 50A
- Load Step: 0A-12.5A, di/dt=100A/μS
- Peak to Peak Deviation: <+/-3%

电源模块解决FPGA的供电问题 – 快速动态响应



基站电源中高速ADC/DAC的供电要求 – 安静，低噪声

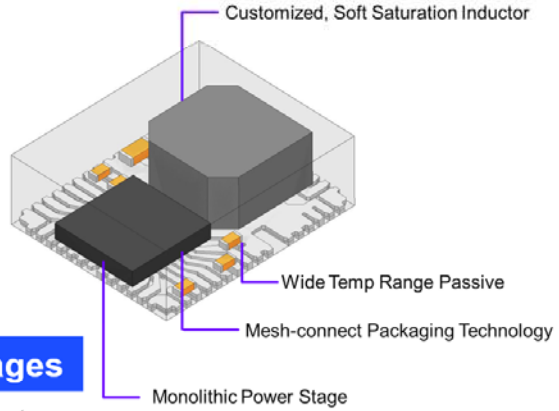
Enabling Excellent DAC/ADC Performance

XILINX Design Targets

- Replace low efficiency LDO with High Efficiency Switching Solution
- Offer easy to implement solution for customers to enable RFSoC DAC/ADC

MPS Solution: Power Modules

- Greater Efficiency & Increased Thermal Performance
  - (Optimal for passively cooled applications)
- Same Noise Performance as LDO
- Fast transient (for power cycling)



Key Advantages

- Simple board layout
- Small Solution Size
- Minimum components
- Fast Time to Market
- Complete power supply
- Better EMI & Noise performances

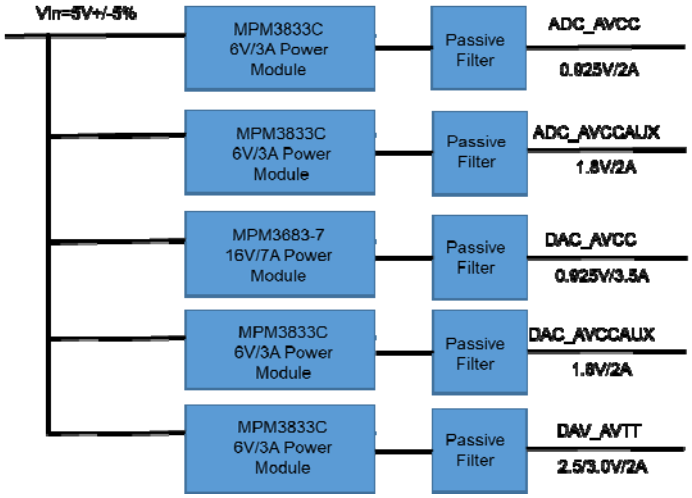
Featuring Power Modules

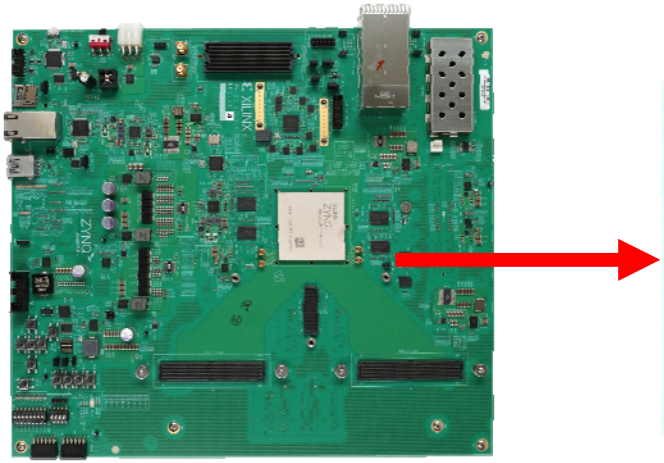
- MPM3833C
- MPM3683-7

https://forums.xilinx.com/t5/Adaptable-Advantage-Blog/Webinar-Designing-on-the-World-s-Only-Single-Chip-Adaptable/ba-p/1105645

MPS低噪声解决方案- EVREF0102

- MPS Solution – EVREF0102
  - o **Ultra-low noise - <1mV Ripple**
  - o **High Efficiency**
  - o **Fast Transient**
- Now on board Xilinx ZCU216 Gen3 board powering:
  - o 16x 14-bit 2.5GSPS ADCs
  - o 16x 14-bit 10.0GSPS DACs





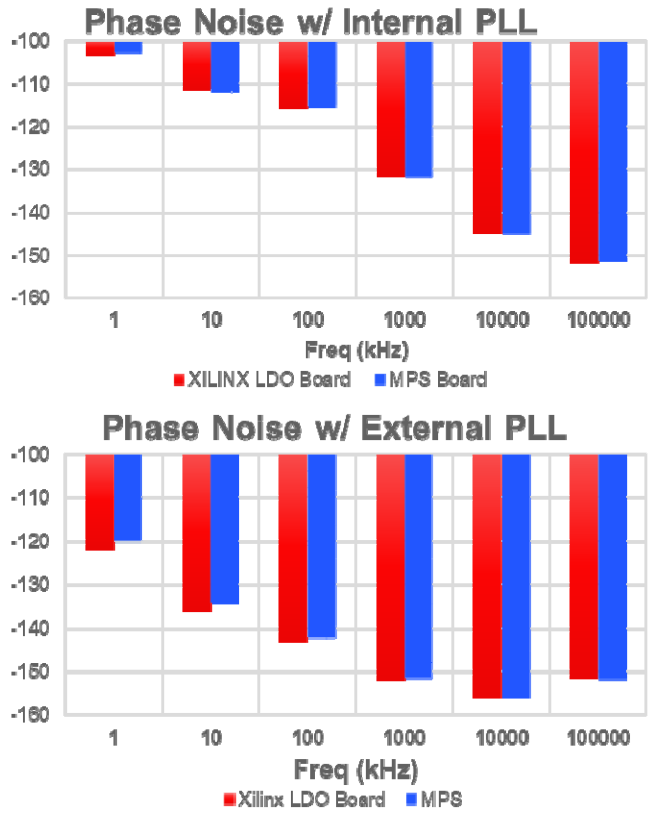
EVREF0102

Available for Evaluation

Xilinx Zynq US+ RFSoC ZCU216 Development kit

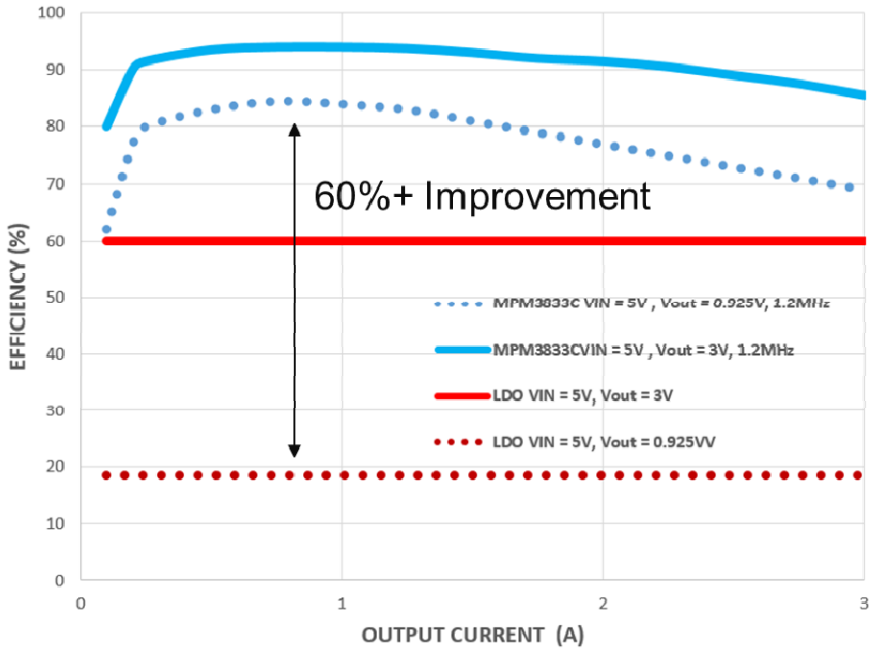
模块方案和LDO方案的噪声比较

Noise Comparison



Test performed at Xilinx lab on RF
12-bit 2GSPS ADCs and 14-bit 6.4GSPS DACs

Efficiency Comparison:



MPS电源模块介绍

Single Buck

Multi-out Buck

Boost & Buck-Boost

POE

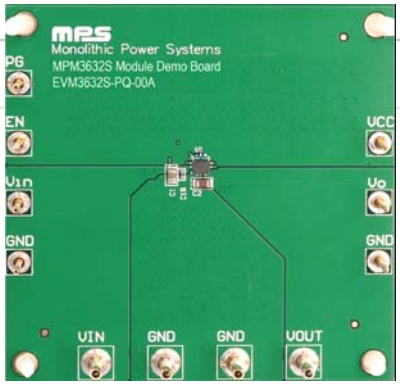
USB Charger

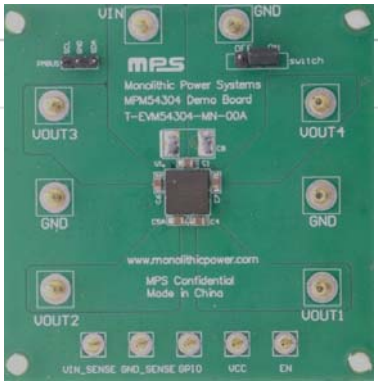
MPS电源模块在5G基站电源中的推荐产品

V_{IN} \ I_{OUT}	# of Output	1.2A	2A	3A	5A-6A	8A	10A	20A	36A/50A	100A
High Voltage (24-36V Input)	Single				MPM3596 PMBus, Parallel 10x10x4.4mm					
Medium Voltage (12V Input)	Single	MPM3610 CCM 3x5x1.6mm		MPM3632S CCM 3x3x1.45mm	MPM3650 Ext SS 4x6x1.6mm	MPM3683-7 Ext SS, CCM 7x7x4mm	MPM3695-10 PMBus, Parallel 8x8x2mm	MPM3695-25 PMBus, Parallel 10x12x4mm	MPM3690-30B/50B 16x16x5.18mm	MPM3695-100 PMBus, Parallel 15x30x5.18mm
	Multiple Output		MPM54304 2x3A+2x2A, I2C 7x7x2mm		MPM54504 4x5A 9x15x5.18mm	MPM81204 2x12A+2x5A 9.5x16x5.18mm		MPM82504 4x25A, PMBus, Parallel 15x30x5.18mm		
Low Input (3.3V, 5.5V Input)	Single	MPM3811 CCM 2.5x3.5x1.6mm	MPM3822C CCM 2.5x3.5x1.6mm	MPM3833C CCM 2.5x3.5x1.6mm	MPM3860 6A 4x6x1.6mm					

FPGA 其他电源轨供电 (3-18A) 方案

	MPM3860	MPM3632S	MPM54304	MPM3695-10
输入电压范围	3V-16V	3V-16V	3V-16V	3V-16V
输出电压范围	0.5V-5.5V	0.6V-5.5V	0.6V-3.3V	0.5V-3.3V
输出电流	6A	3A	2x3A+2x2A	10A
尺寸	4x6x1.6mm	3x3x1.45mm	7x7x2mm	8x8x2mm
效率（12V-1V）	90%	89%	89%	86%
I2C	No	No	Yes	Yes
可并联	No	No	Yes, 6A+4A	Yes, up to 20A



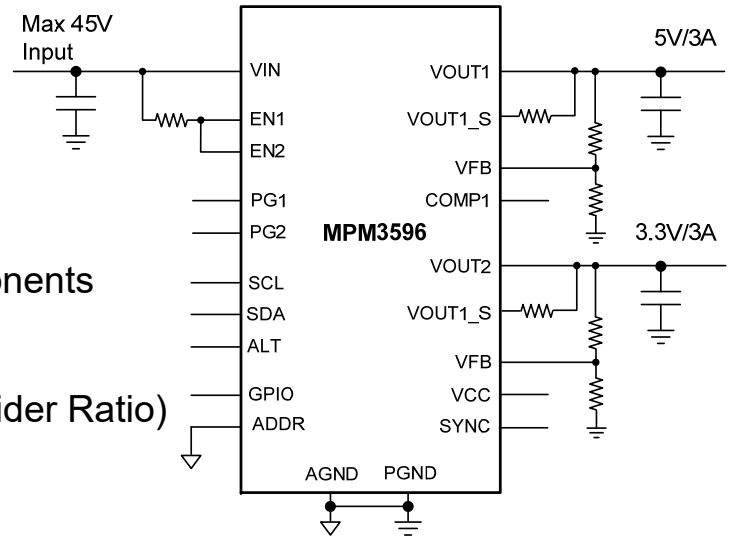


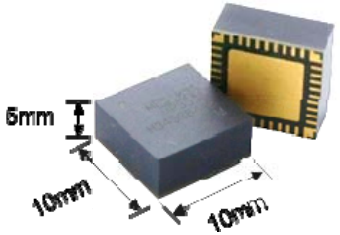
MPM3596 Introduction

FEATURES

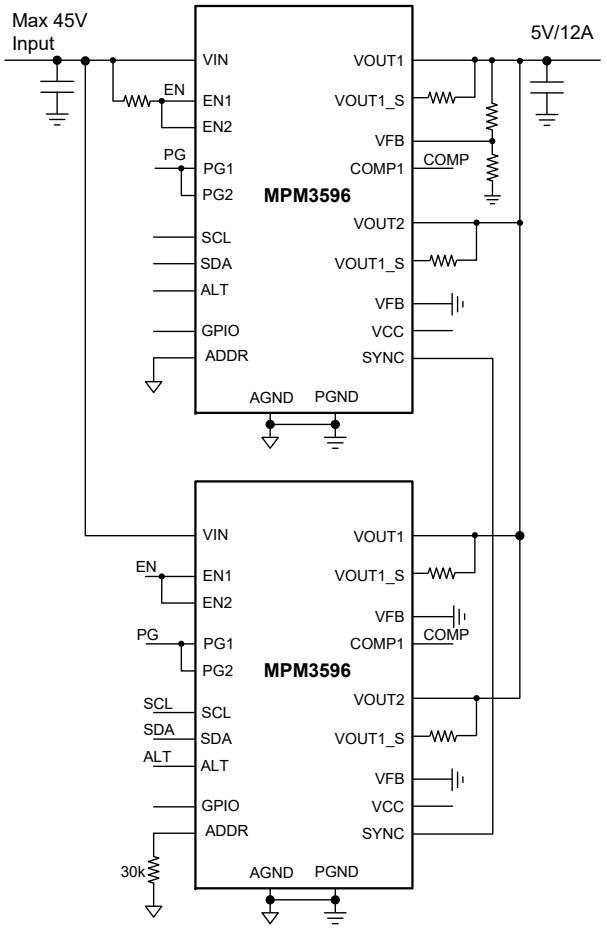
- Wide V_{IN} Range: 3.5V-45V
- V_{OUT} Range: 0.4V-24V
- Dual 3A, Single 6A
  - Parallel up to 36A
- LGA 10x10x4.4mm
- Small Solution Size, Minimum Ext Components
- Telemetry Read-back
  - o V_{IN}, V_{OUT}, I_{OUT}, Temp
- Change V_{OUT} on-the-fly (Step: 1.5mV*Divider Ratio)
- Low EMI
  - Dual Side Input Capacitors
  - Dithering /Frequency Spread Spectrum
- ±1% V_{OUT} Over Temp
- Peak Current Mode Control
- External Clock Synchronization
- Programmable MTP Registers including
  - o Switching Frequency
  - o Protection Threshold & Responses
  - o PWM/PFM
- OTP, OVP, UVP, OCP
- GPIO can be programmed as ADC input

Application Circuit: Dual Output





Application Circuit: Paralleling

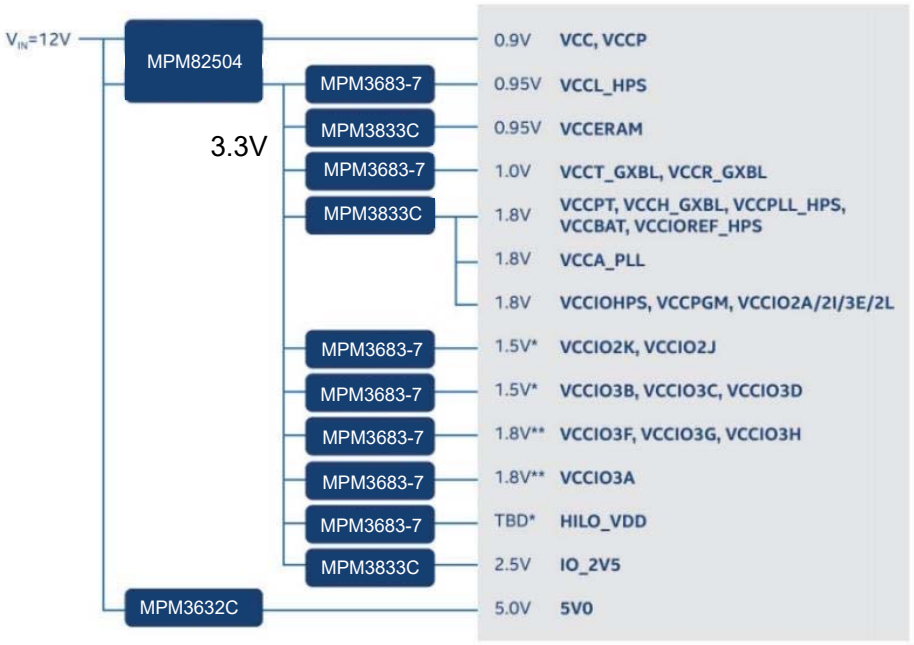


MPS在5G电源基站中的实际案例

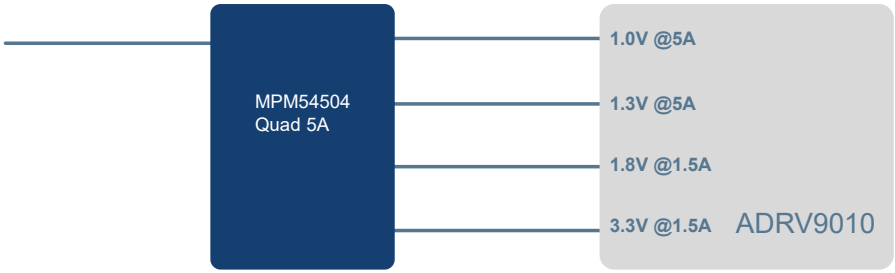
rev 20180330

Success Story – Intel Arria 10 Platform

5G Small Station



FPGA Power



Transceiver Power

Summary

- 5G 基站架构和电源需求综述
  - 5G网络架构与基站规划
  - 5G基站电源架构
- 5G基站电源设计的关键技术
  - “大”与“小”，“多”与“少”
  - “动”与“静”，“短”与“长”
- MPS电源模块产品介绍
  - 核电压供电
  - Transceiver供电
  - POL以及PoE供电
- 5G电源基站中的实际案例
  - Xilinx平台
  - Intel 平台

Thank You~