Meeting the Impedance Mask: Strategies for PDN Design and Optimization

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Introduction

In telecommunication applications, target impedance serves as a crucial benchmark for PDN design. It ensures that the die operates within an acceptable level of rail voltage noise, even under the worst-case transient current scenarios, by defining the maximum allowable PDN impedance for the power rail on the die.

This article will focus on the optimization techniques to meet the target impedance using the MPQ8785 point-of-load (PoL) device, all while providing valuable insights and practical guidance for designers seeking to optimize their power delivery networks (PDNs) for reliable and efficient power delivery.

Defining Target Impedance

With the rise of high-frequency signals and escalating power demands on boards, power designers are prioritizing noise-free power distribution that can efficiently supply power to the integrated circuit (IC). Controlling the power delivery network's impedance across a certain frequency range is one approach to guarantee proper operation of high-speed systems and meet performance demands. This impedance can generally be estimated by dividing the maximum allowed ripple voltage by the maximum expected current step load. The power delivery network's target impedance (Z_{TARGET}) can be calculated with Equation (1):

$$Z_{TARGET} = \frac{V_{SUPPLY} \times \text{Ripple Tolerance}}{I_{TRANSIENT}} \quad (1)$$

Achieving Z_{TARGET} across a wide frequency spectrum requires a power supply at lower frequencies, combined with strategically placed decoupling capacitors at middle and higher frequencies. Figure 1 shows the impedance frequency characteristics of multi-layer ceramic capacitors (MLCCs).

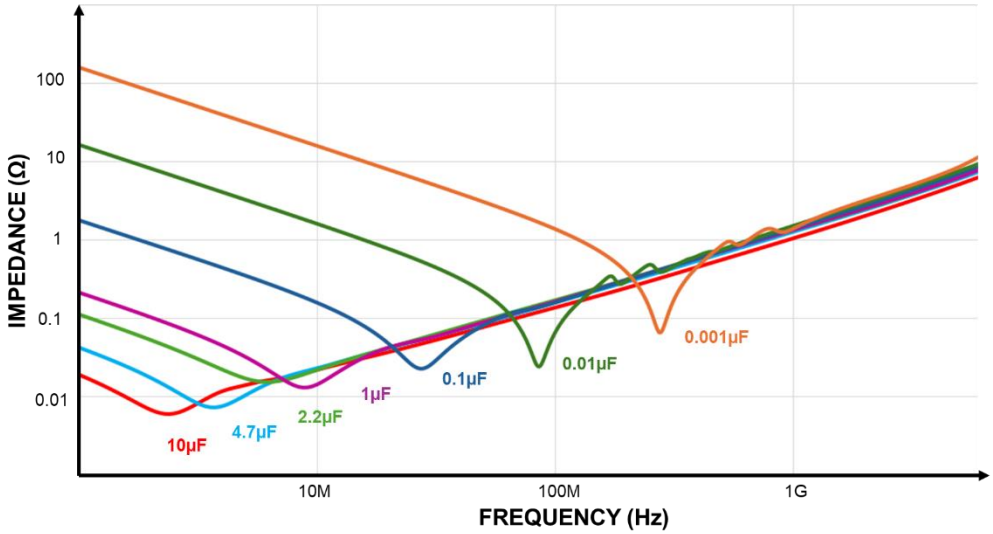

Figure 1: Impedance Frequency Characteristics of MLCCs

Maintaining the impedance below the calculated threshold ensures that even the most severe transient currents generated by the IC, as well as induced voltage noise, remain within acceptable operational boundaries.

Figure 2 shows the varying target impedance across different frequency ranges, based on data from a vendor website. [1] This means every element in the power distribution must be optimized at different frequencies.

Qualcomm® Snapdragon™ 410E (APQ 8016E) processor Device Specification *Electrical Specifications*

3.3.1 PDN system specification (PCB + baseband IC)

Table 3-5 lists the PCB + baseband IC PDN requirements. Meeting this specification requires the use of a commercial circuit simulator program (e.g., ADS) and the APQ8016E S-parameter model.

Table 3-5 PCB + baseband IC PDN impedance vs. frequency

Power domain	Required PCB routing inductance (caps shorted) [1]	Max impedance		
		DC to 10 Hz	10 Hz to 10 MHz	10–500 MHz
VDD_MEM	500 pH max.	11 mΩ	104 mΩ	250 mΩ
VDD_CORE	250 pH	5 mΩ	79 mΩ	160 mΩ
VDD_APC	200 pH	4 mΩ	45 mΩ	140 mΩ

Figure 2: Target Impedance Example

Understanding Power Delivery Network (PDN) Impedance

In theory, a power rail aims for the lowest possible PDN impedance. However, it is unrealistic to achieve an ideal zero-impedance state. A widely adopted strategy to minimize PDN impedance is placing various decoupling capacitors beneath the system-on-chip (SoC), which flattens the PDN impedance across all frequencies. This prevents voltage fluctuations and signal jitter on output signals, but it is not necessarily the most effective method to optimize power rail design.

Three-Stage Low-Pass Filter Approach

To further explore optimizing power rail design, the fundamentals of PDN design must be re-examined in addition to considering new approaches to achieve optimal performance. Figure 3 shows the PDN conceptualized as a three-stage low-pass filter, where each stage of this network plays a specific role in filtering and stabilizing the current drawn from the SoC die.

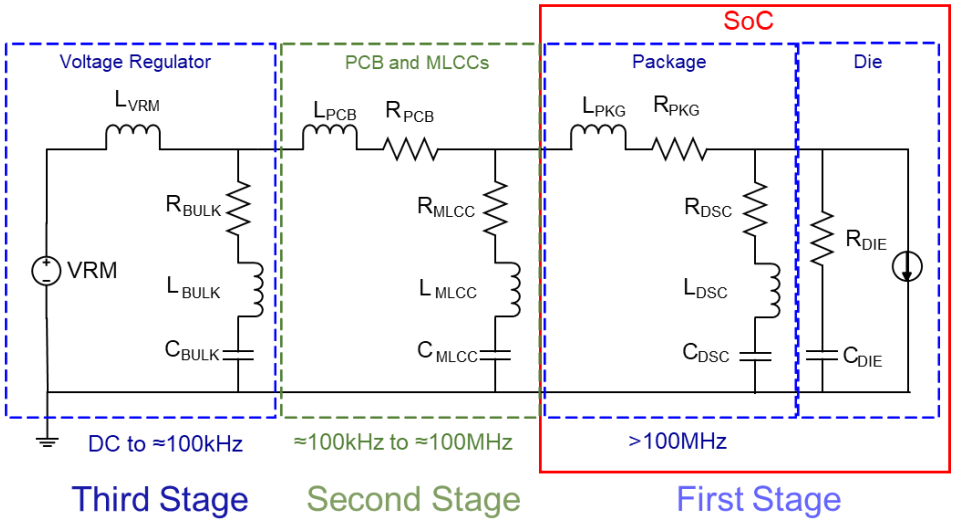

Figure 3: PDN Conceptualized as a Three-Stage Low-Pass Filter

The three-stage low-pass filter is described below:

1. Current drawn from the SoC die: The process begins with current being drawn from the SoC die. Any current drawn is filtered by the package, which interacts with die-side capacitors (DSCs). This initial filtering stage reduces the current's slew rate before it reaches the PCB socket.
2. PCB layout considerations and MLCCs: Once the current passes through the PCB ball grid arrays (BGAs), the second stage of filtering occurs as the current flows through the power planes on the PCB and encounters the MLCCs. During this stage, it is crucial to focus on selecting capacitors that effectively operate at specific frequencies. High-frequency capacitors placed beneath the SoC do not significantly influence lower frequency regulation.
3. Voltage regulator (VR) with power planes and bulk capacitors: The final stage involves the VR and bulk capacitors, which work together to stabilize the power supply by addressing lower-frequency noise.

The PDN's three-stage approach ensures that each component contributes to minimizing impedance across different frequency bands. This structured methodology is vital for achieving reliable and efficient power delivery in modern electronic systems.

Case Study: Telecom Evaluation Board Analysis

This in-depth examination uses a telecommunications-specific evaluation board from MPS, which demonstrates the capabilities of the MPQ8785, a high-frequency, synchronous buck converter, in a real-world setting. Moreover, this case study underlines the importance of capacitor selection and placement to meet the target impedance.

To initiate the process, PCB parasitic extraction is performed on the MPS evaluation board. Figure 4 shows a top view of the MPQ8785 evaluation board layout, where two ports are selected for analysis. Port 1 is positioned after the inductor, while Port 2 is connected to the SoC BGA.

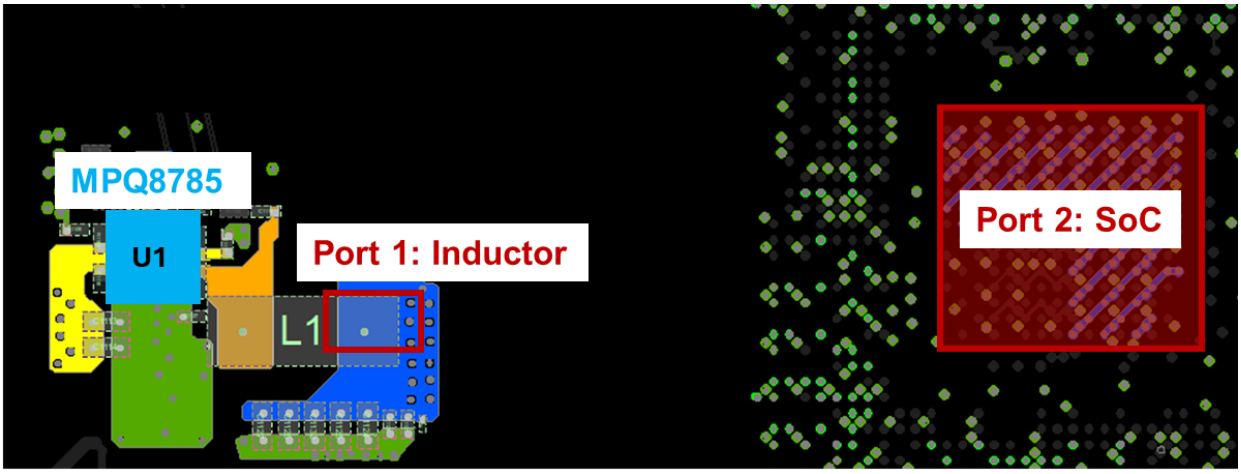

Figure 4: MPS Telecom Evaluation Board

Capacitor models from vendor websites are also included in this layout, including the equivalent series inductance (ESL) and equivalent series resistance (ESR) parasitics. As many capacitor models as possible are allocated beneath the SoC in the bottom of the PCB to maintain a flat impedance profile.

Table 1 shows the initial capacitor selection for different quantities of capacitors targeting different frequencies.

Table 1: Initial Capacitor Selection

Quantity	Capacitance
2	560pF
5	1nF
2	0.01µF
5	0.1µF
2	1µF
5	2.2µF
2	4.7µF
2	10µF
3	22µF

Figure 5 shows a comparison of the target impedance profile defined by the PDN mask for the core rails to the actual initial impedance measured on the MPQ8785 evaluation board using the initially selected capacitors. This graphical comparison enables a direct assessment of the impedance characteristics, facilitating the evaluation of the PDN performance.

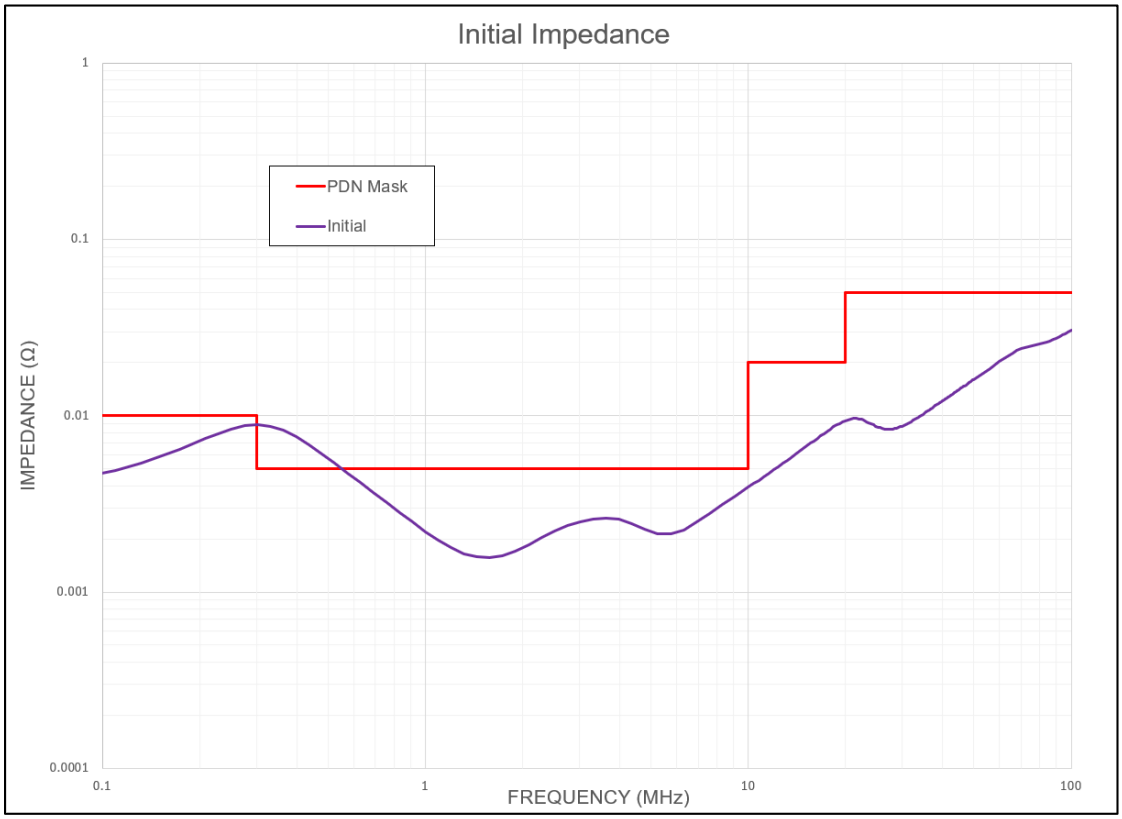

Figure 5: Target Impedance Profile vs. Initial Impedance

Based on the data from Figure 5, the impedance exceeds the specified limit within the 300kHz to 600kHz frequency range, indicating that additional capacitance is required to mitigate this issue. Introducing additional capacitors effectively reduces the impedance in this frequency band, ensuring compliance with the specification. Notably, high-frequency capacitors are also observed to have a negligible impact on the impedance at higher frequencies, suggesting that their contribution is limited to specific frequency ranges. This insight informs optimizing capacitor selection to achieve the desired impedance profile.

Through an extensive series of simulations that systematically evaluate various capacitor configurations, the optimal combination of capacitors required to satisfy the impedance mask requirements was successfully identified. Table 2 shows the results of this iterative process, outlining the optimal quantity of capacitors and total capacitance.

Table 2: Optimal Capacitor Selection

Quantity	Capacitance
5	10µF
5	22µF

The final capacitor selection ensures that the PDN impedance profile meets the specified mask, thereby ensuring reliable power delivery and performance. Figure 6 shows the final impedance with optimized capacitance.

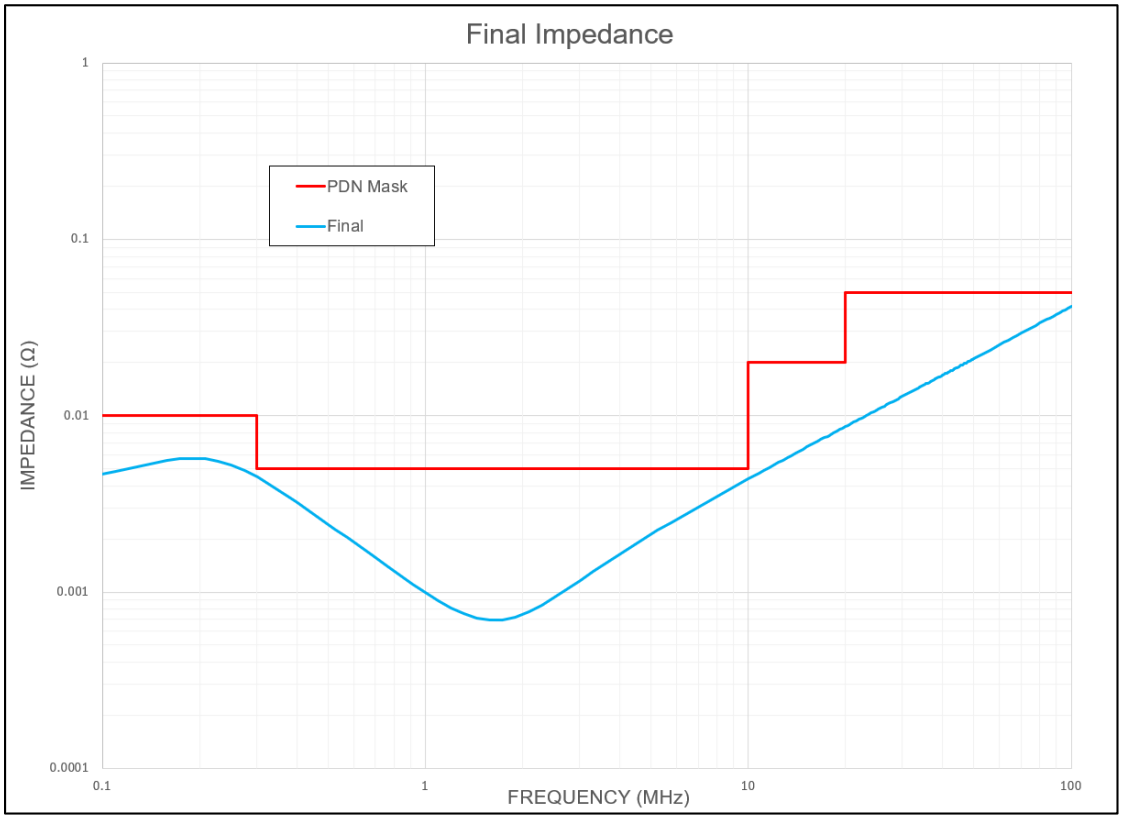

Figure 6: Final Impedance with Optimized Capacitance

With a sufficient margin at frequencies above 10MHz, capacitors that primarily affect higher frequencies can be eliminated. This strategic reduction minimizes the occupied area and decreases costs while maintaining compliance with all specifications. Performance, cost, and space considerations are effectively balanced by using the optimal combination of capacitors required to satisfy the impedance mask requirements, enabling robust PDN functionality across the operational frequency range.

To facilitate the case study, the impedance mask was modified within the 10MHz to 40MHz frequency range, decreasing its overall value to 10mΩ. Implementing 10 additional 0.1µF capacitors was beneficial to reduce impedance in the evaluation board, which then effectively reduced the impedance in the frequency range of interest.

Figure 7 shows the decreased impedance mask as well as the evaluation board's impedance response. The added capacitance successfully reduces the impedance within the specified frequency range.

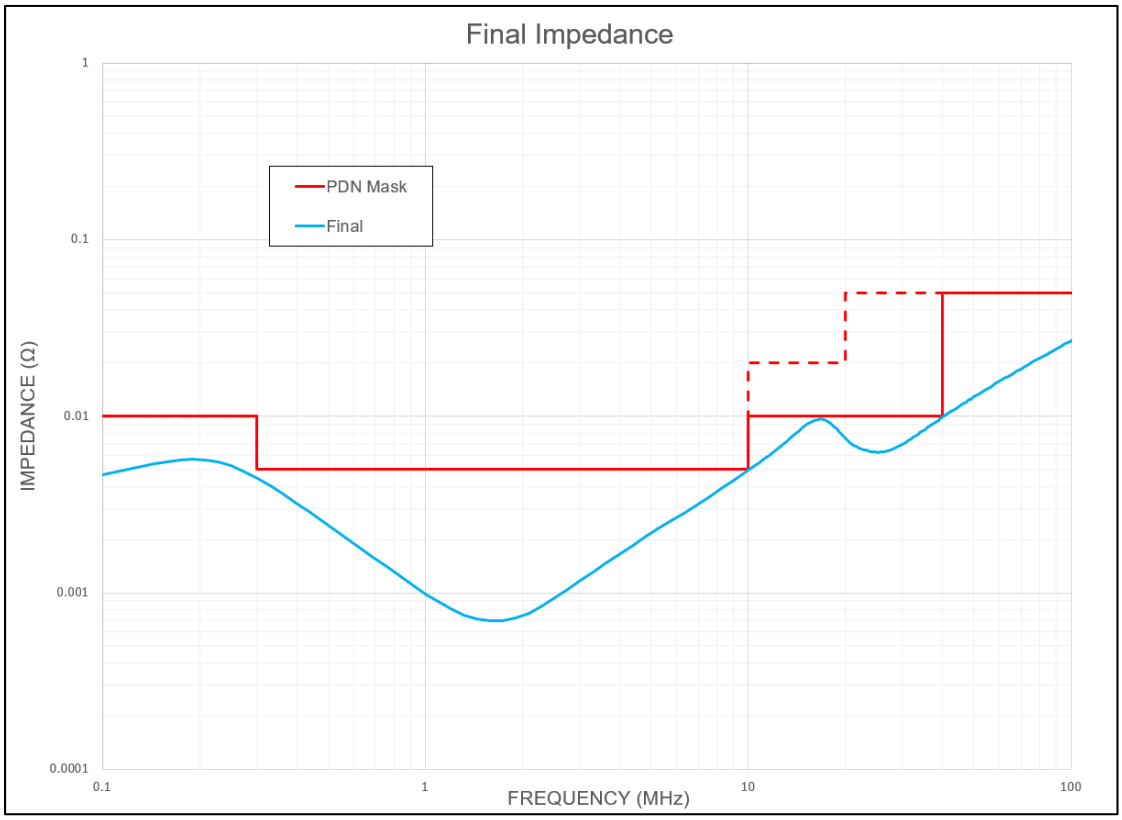

Figure 7: Impedance with Optimized Capacitance for Decreased PDN Mask

Conclusion

This article used the MPQ8785 evaluation board to optimize power delivery network (PDN) performance, ensuring compliance with the specified impedance mask. Through this optimization process, models were developed to predict the impact of various capacitor types on impedance across different frequencies, which facilitates the selection of suitable components.

Capacitor selection for optimized power rail design depends on the specific impedance mask and frequency range of interest. A random selection of capacitors for a wide variety of frequencies is insufficient for optimizing PDN performance. Furthermore, the physical layout must minimize parasitic effects that influence overall impedance characteristics, where special attention must be given to optimizing the layout of capacitors to mitigate these effects.

For more details, learn about MPS's wide selection of step-down converters.

References

1. Qualcomm Technologies, Inc., "Qualcomm® Snapdragon™ 410E (APQ 8016E) Processor Device Specification," Section 3.3.1, Table 3-5, pp. 55, Sep. 2016.