Application Note for Flyback Converter Using Variable Off-time Controller---HFC0300

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ABSTRACT

This paper presents design guidelines for flyback converter using variable off-time controller-HFC0300 from MPS as shown in Figure 1. Design of a flyback converter with variable off time (or quasi fixed on time) control is quite simple and straightforward through the step-by-step design procedure described in this application note. Experimental results based on the design example are presented in the last part.

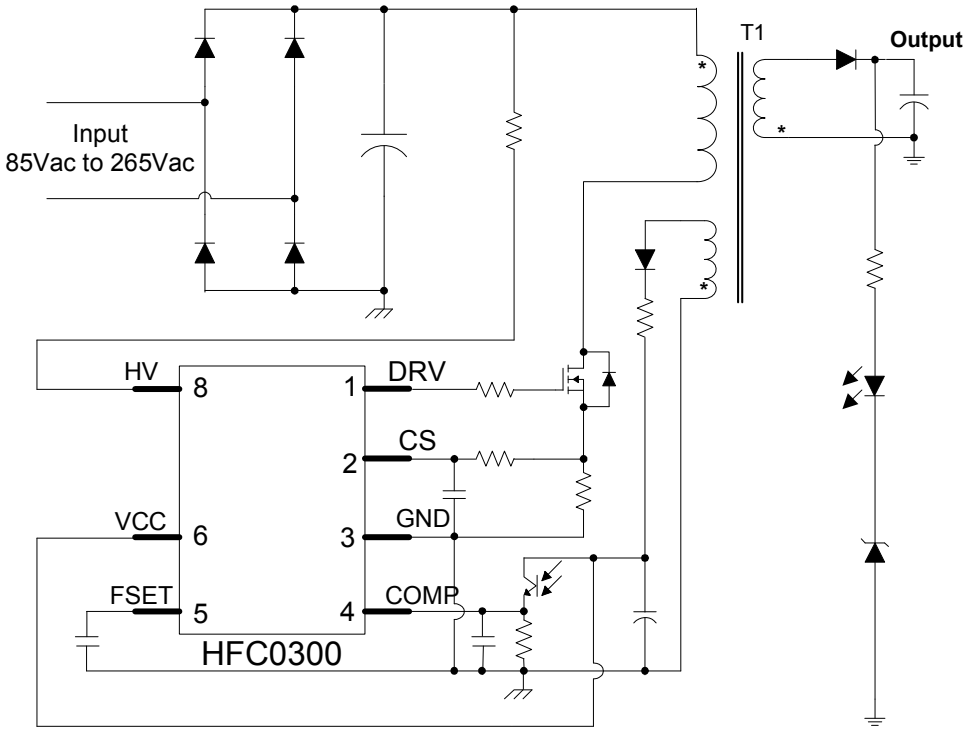

Figure 1— Flyback Converter Using Variable Off-time Controller--HFC0300

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1. HFC0300 INTRODUCTION

HFC0300 is a variable off-time controller which is integrated with a high voltage current source. Based on a fixed peak current technique, the controller decreases its frequency as the load becomes lighter. As a result, it offers excellent light load efficiency while optimizing the efficiency in other load conditions. When the output power falls below a given level, the controller enters the burst mode to further reduce the power loss at no load or light load condition. Internal Vcc Under Voltage Lockout (UVLO), Over Load Protection (OLP), Over Voltage Protection (OVP), Short Circuit Protection (SCP) and Thermal Shutdown (TSD) are all integrated in the IC to minimize the external component count. This paper presents practical design guidelines for an off-line flyback converter employing HFC0300. Step-by-step design procedure for off-time controlled flyback converter using HFC0300 is introduced in this application note, mainly including transformer design, output filter design and component selection.

2. VARIABLE OFF-TIME CONTROL INTRODUCTION

Variable Off-Time control is one of the variable frequency control scheme for flyback converter. By implementing a fixed peak current mode control, the peak current of the switch is fixed (quasi-fixed switch on time) and the off-time duration is regulated according to the required output power. During the on time of the MOSFET, the Drain current increases. Once the Drain current reaches the internal fixed peak current level, the MOSFET turns off. The feedback loop controls the frequency or the off time based on the output condition. So as the load decreases, the off time expands and the switching frequency also decreases. As the frequency decreases at the light load, the contribution of all the frequency-dependent losses accordingly goes down (gate drive loss, switching losses, core loss), naturally improving the efficiency.

Reducing the switching frequency will certainly force the converter to operate into the audible region. To prevent the transformer mechanical resonance, HFC0300 gradually reduces the peak current as the load becomes lighter.

Figure 2 shows the Drain-Source voltage waveform of primary switch in an off-time control flyback converter. During the on time of MOSFET, the Drain current increases linearly until the peak current level is reached. The MOSFET then turns off. The leakage inductance in the flyback transformer rings with the parasitic capacitance and causes a high voltage spike, which should be limited by a clamp circuit. When FSET Pin voltage reaches the level of COMP (feedback PIN), the switch turns on again and starts a new switching cycle.

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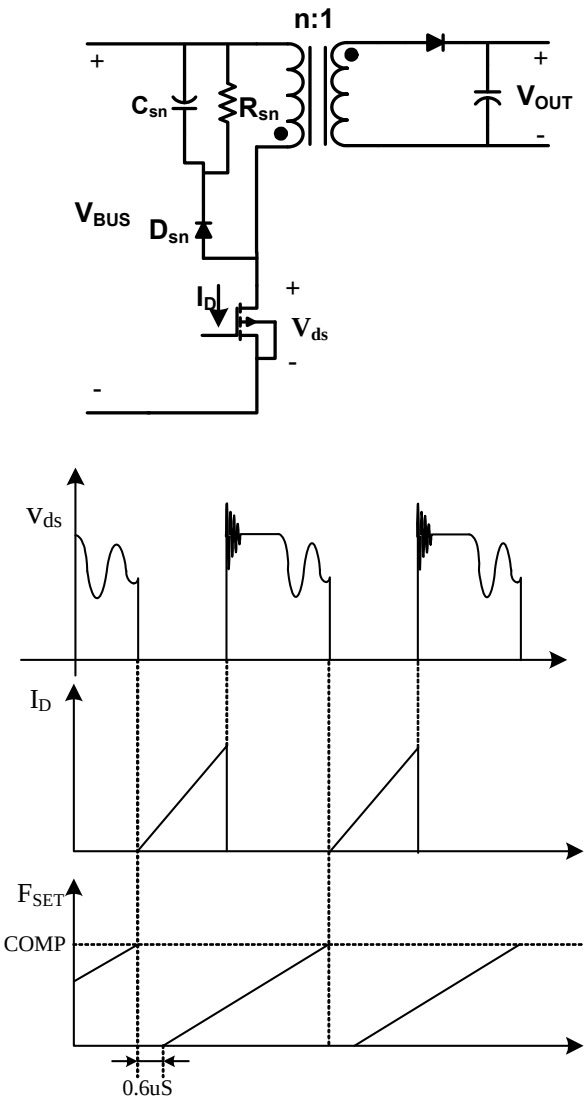

Figure 2— Key Waveforms of Off-Time Flyback Converter

3. DESIGN PROCEDURE

A. Predetermined Input and Output Specifications

- Input AC voltage range: $V_{ac(min)}$, $V_{ac(max)}$, for example $90V_{ac}$~$265V_{ac}$ RMS
- DC bus voltage range: $V_{in(max)}$, $V_{in(min)}$.
- Output: V_o , $I_{o(min)}$, $I_{o(max)}$, P_{out}
- Estimated efficiency: η, It is used to estimate the power conversion efficiency to calculate the maximum input power. Generally, η is set to be 0.8~0.9 according to different output applications.

Then the maximum input power can be given as:

$$P_{in} = \frac{P_{out}}{\eta} \quad (1)$$

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Figure 3 shows the typical DC bus voltage waveform. The DC input capacitor C_{in} is usually set as 2μF/W for the universal input condition. For 230V single range application, the capacitance can be half the value.

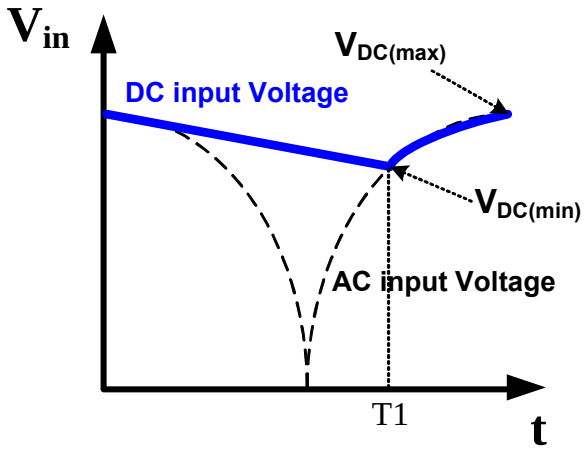

Figure 3— Input Voltage Waveform

From the waveform above, the AC input Voltage V_{AC} and DC input Voltage V_{DC} can be got as:

$$V_{DC}\left(V_{ac},t\right)=\sqrt{2\times V_{ac}^{2}-\frac{2\times P_{in}}{C_{in}}\times t} \tag{2}$$

By setting V_{AC}=V_{DC}, T1 where DC bus voltage reaches to its minimum value $V_{DC(min)}$ can be calculated as

$$V_{DC(min)}=V_{DC}\left(V_{ac(min)},T1\right) \tag{3}$$

Then, the minimum average DC input voltage $V_{in(min)}$ can be got as:

$$V_{in(min)}=\frac{\sqrt{2}\cdot V_{ac(min)}+V_{DC(min)}}{2} \tag{4}$$

The maximum average DC input voltage $V_{in(max)}$ can be got as:

$$V_{in(max)}=\sqrt{2}\cdot V_{ac(max)} \tag{5}$$

B. Determine the Startup Circuitry

Figure 3 shows the startup circuit. When power is on, the internal 2mA current source charges C1 through R1 connected to HV pin of HFC0300. Once VCC voltage reaches 11.7V, the internal high voltage current source (2mA) turns off and IC starts switching, then the auxiliary winding takes over the power supply. If VCC drops below 8.2V before the auxiliary winding takes over the power supply, the switching stops and the internal high voltage current source turns on again, which re-charges the VCC external capacitor C1, starting another start-up procedure(see Figure 4).

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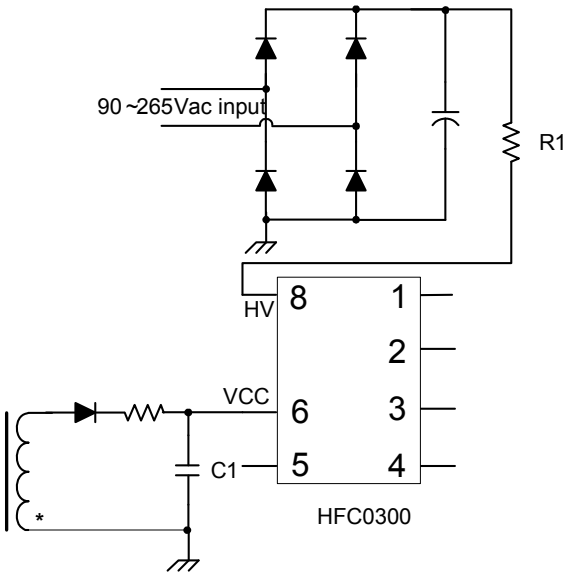

Figure 3— The Startup Circuit with HFC0300

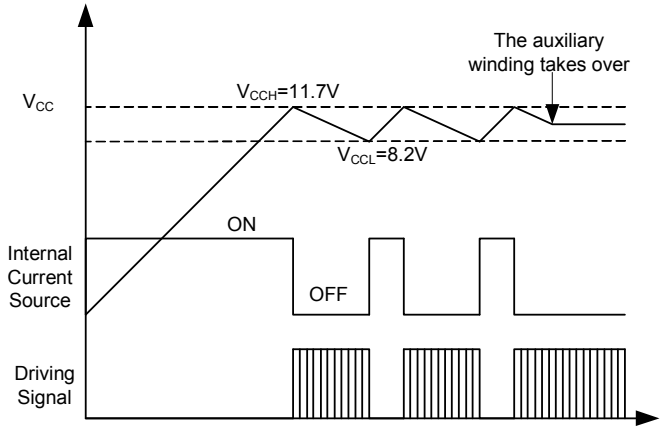

Figure 4— The Startup Waveform and VCC UVLO of HFC0300

C. Turns Ratio-N, Primary MOSFET and Secondary Rectifier Diode Selection

Figure 5 shows the typical voltage waveform of the primary MOSFET and secondary rectifier diode in a flyback converter. From the waveform, the primary MOSFET Drain-Source voltage rating V_{ds} can be got as equation (6):

$$V_{ds} = \frac{Vin(max) + N \cdot (V_{out} + V_F) + 60V}{k} \quad (6)$$

Where k is the derating factor which is typically selected as 0.9. V_F is the forward voltage of the rectifier diode, 60V spike voltage is assumed here.

The secondary rectifier diode voltage rating V_{ka} can be estimated as equation (7):

$$V_{ka} = \frac{\frac{Vin(max)}{N} + V_{out}}{k} \quad (7)$$

Where k is the derating factor which is typically selected as 0.9.

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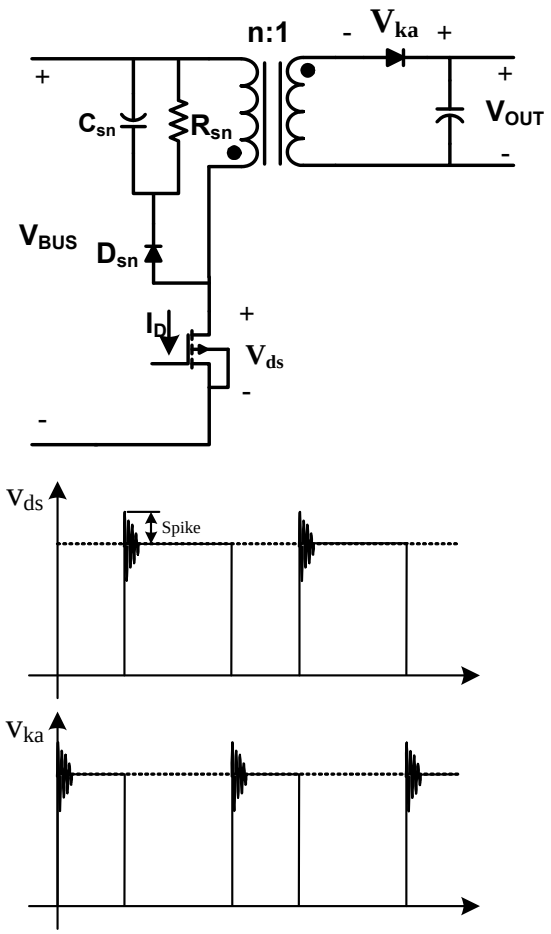

Figure 5— Voltage Stress of Primary MOSFET and Secondary Rectifier Diode

From equation (6) and (7), the voltage rating for primary MOSFET and secondary rectifier diode versus turns-ratio N can be calculated and shown in Figure 6.

For example, in 90Vac~265Vac input, 19V output adapter application, 650V MOSFET and 100V rectifier diode is preferred for better performance. From figure 7, N=6 is selected for the required voltage rating.

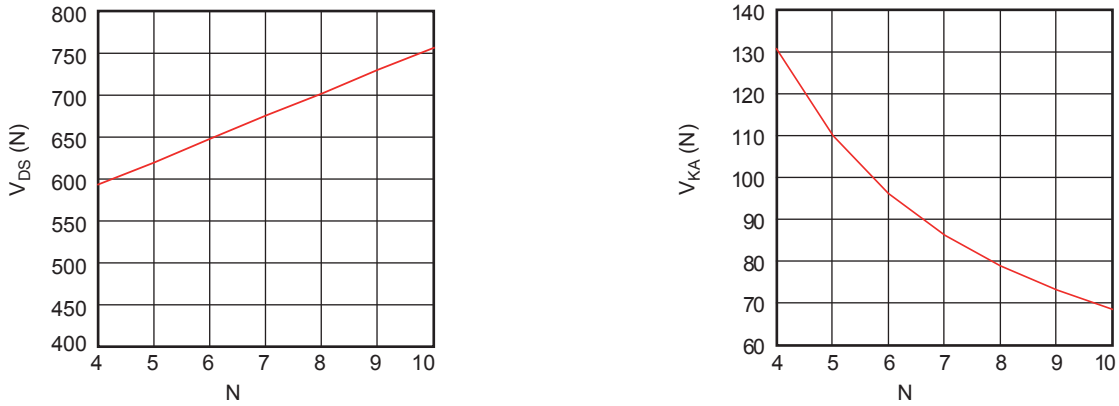

Figure 6— Voltage Stress Rating of Primary MOSFET and Secondary Rectifier Diode

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D. Current Sense Resistor

The peak current level is internally set to be 0.5V, so current sense resistor sets the primary side peak current, which also determines the operation mode of the converter, such as CCM, BCM or DCM. If power supply is designed to operate at BCM at low line input, it will operate at DCM at high line and the same load condition. The magnetizing inductor current (reflected to the primary side) and the Drain-Source voltage of the primary MOSFET is shown as Figure 8.

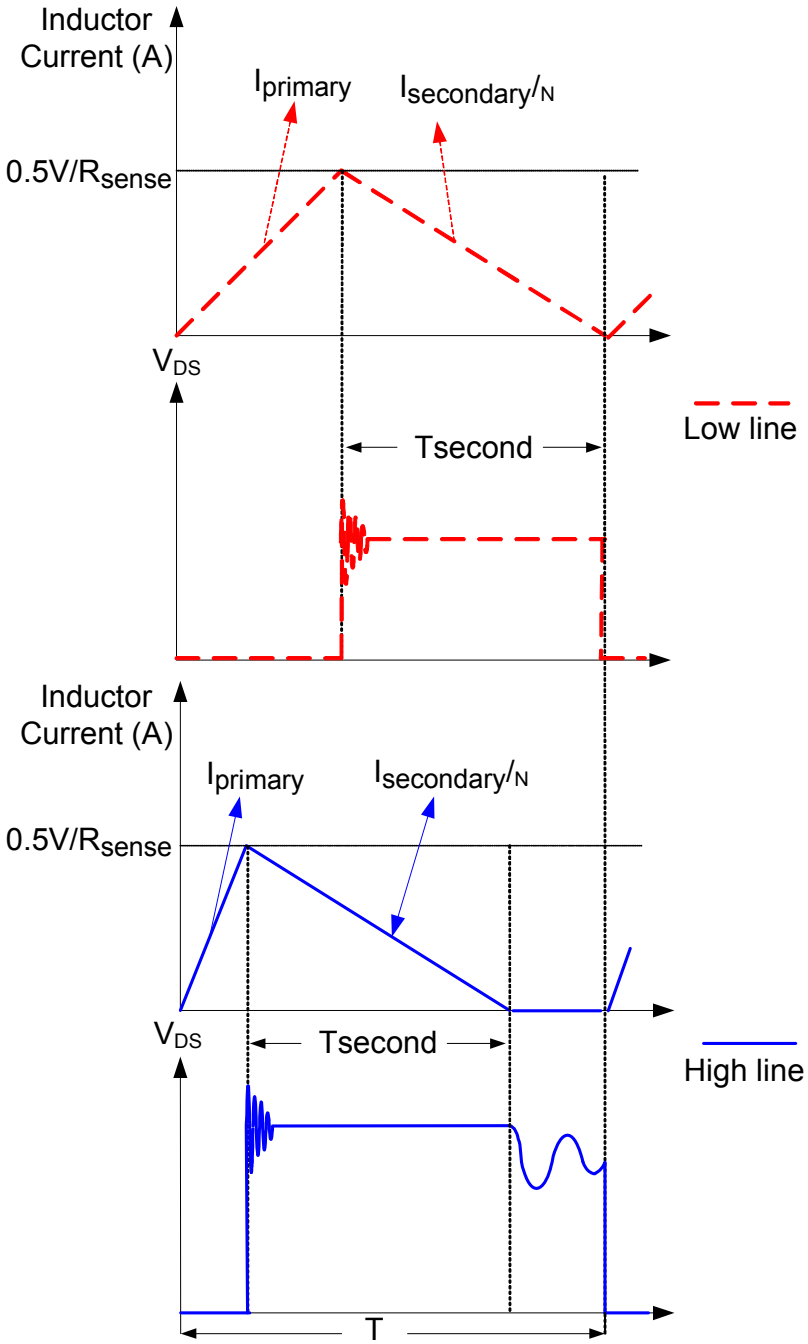

Figure 8— Inductor Current and Voltage of Primary MOSFET at Different Line

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The time duration of secondary current can be got as equation (8).

$$T_{second} = \frac{L_m * I_{peak}}{N * V_O} \tag{8}$$

Where L_m is primary magnetizing inductance, I_{peak} is primary peak current. Since I_{peak} is always the same at different input and same output conditions, so the time duration of secondary current is the same. The switching period can be calculated by equation (9).

$$T = \frac{N * I_{peak} * T_{second}}{2 * I_o} \tag{9}$$

From (9), the switching period also keeps the same at different input and same output conditions. Since the primary side switch on time decreases with the input voltage increasing, therefore, the higher the input line voltage, the deeper DCM mode it will enter. Usually, the parameters should be designed at the minimum input condition to guarantee the converter can deliver the required output power at minimum input condition.

Since N has been selected, so if the power supply is designed to operate at boundary current mode (BCM) at low line, the peak current can be calculated easily as equation (10).

$$I_{peak_BCM} = \frac{2I_o}{1-D} \tag{10}$$

Where D is the duty ratio of the switching, it can be got as equation (11).

$$D = \frac{(V_o + V_F) * N}{V_{in} + (V_o + V_F) * N} \tag{11}$$

If the peak current set by current sense resistor is larger than I_{peak_BCM}, the power supply will enter DCM. On the contrary, if the peak current set by current sense resistor is less than I_{peak_BCM}, the power supply will enter CCM as Figure 9. Here, we define K_{depth} as the depth of CCM.

$$K_{depth} = \frac{I_{valley}}{I_{peak}} \tag{12}$$

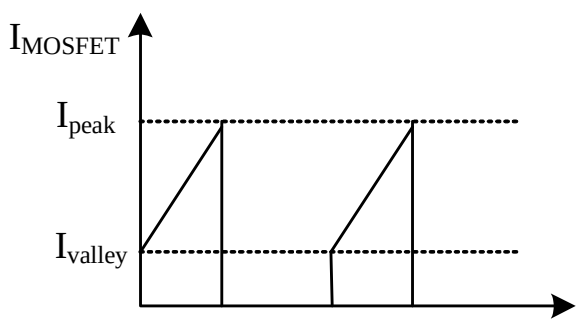

Figure 9— Primary Current at CCM

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So peak current can be got as equation (13).

$$I_{peak} = \frac{2I_o}{(1-D)*(1+K_{depth})*N} \tag{13}$$

Usually, BCM (boundary current mode) is preferred for the power level below 40W. CCM (continuous current mode) is selected when the power level is higher than 40W. The higher the power delivers, the deeper CCM should be adopted for higher efficiency and better thermal performance at full load. For example, for a 90W power supply, 0.5 could be chosen for K_{depth}.

So when a power supply SPEC is given, we need to determine the converter operation mode firstly, i.e. determine the K_{depth}. I_{peak} and I_{valley} can be calculated by equation (10) to (13). And the current sense resistor could be selected by equation (14).

$$R_{sense} = \frac{V_{peak}}{I_{peak}} \tag{14}$$

Where V_{peak} is the peak voltage threshold of the current resistor, it is a constant 0.5V for HFC0300.

The current resistor with the proper power rating should be chosen based on the power loss given in equation (15)

$$P_{sense} = \left[\left(\frac{I_{peak}+I_{valley}}{2}\right)^2 + \frac{1}{12}\left(I_{peak}-I_{valley}\right)^2\right]*D*R_{sense} \tag{15}$$

E. Primary side Inductance Lm

The power that a flyback converter can deliver is related to the energy stored in the primary side inductance Lm as given in equation (16) and (17) for CCM and DCM respectively.

$$\frac{1}{2}*L_m*(I_{peak}{}^2 - I_{valley}{}^2)*f_s = \frac{p_{o_CCM}}{\eta} \tag{16}$$

$$\frac{1}{2}*L_m*I_{peak}{}^2*f_s = \frac{p_{o_DCM}}{\eta} \tag{17}$$

In order to regulate the delivered power to the output, we can either adjust the peak current value (conventional peak current mode control) and/or adjust the switching frequency. HFC0300 regulates the output power by adjusting the switching frequency while keeping the peak current value constant. Thus, once the peak current is selected, the feedback loop automatically sets the switching frequency to get the desired output power.

Since I_{peak} and I_{valley} have been determined at the beginning of the design procedure, Lm can be calculated if fs is chosen. Offering a good EMI performance, a maximum frequency of 65kHz is usually a good choice because the conducted EMI noise at second harmonics (2*65kHz) is still not tested (conducted EMI frequency range:150kHz~30MHz)

As mentioned in section D, the switching frequency keeps the same ideally at different input line voltage and the same output power. Actually, there is slightly difference in the practical circuit. Since the peak current will be a little bit higher at high input than that at low input due to the inevitable propagation delay though the threshold is constant, the switching frequency will reaches its maximum at low line and full load condition. So we usually choose 65kHz as the frequency at low line and full load. As a result, all the calculation is carried at lowest line.

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F. Design of C_{FSET} and OLP function

The maximum frequency is set by the end of charge of the capacitor C_{FSET} connected to the FSET pin as shown in Fig 10. This capacitor is charged by a constant current source shortly after the primary side switch turns on (about 0.6us), and its voltage is compared with COMP voltage from feedback loop (see Figure 10). When this capacitor voltage reaches the threshold, the capacitor is rapidly discharged down to 0V, and a new period starts. To make the voltage at FSET pin fully discharged, it is internally about 0.6μs delay before the C_{FSET} is charged again (see Figure 11). Thus the switching frequency is regulated by the feedback loop like a VCO (voltage controlled oscillation). The capacitance connected to FSET pin is got as equation (18).

$$C_{FSET} = \frac{28uA * (\frac{1}{f_{max}} + 0.6us)}{0.88V} \tag{18}$$

Where fmax is the maximum frequency set by the capacitor connected to FSET pin.

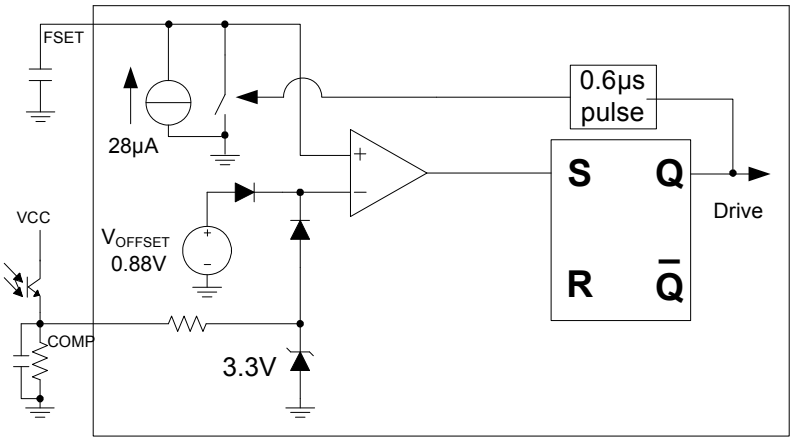

Figure 10— VCO (Voltage Controlled Oscillation) Operation

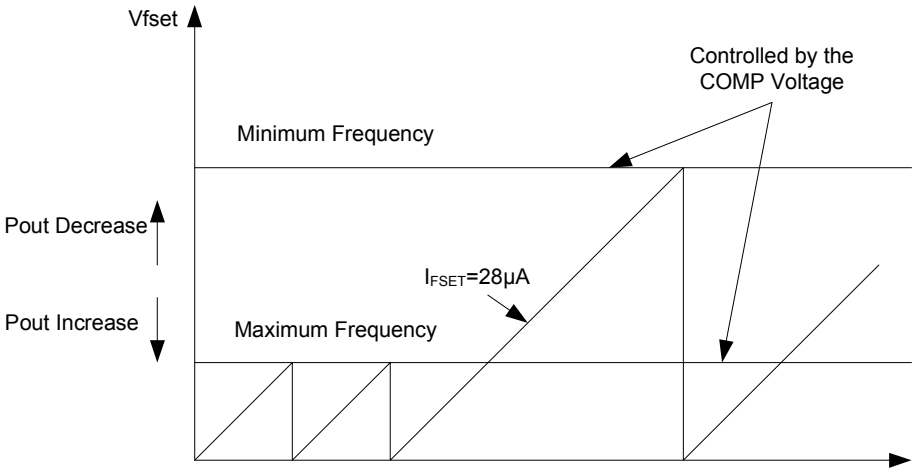

Figure 11— COMP Voltage adjusts the Switching Frequency

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As described as above section, the switching frequency reaches its maximum at low line and full load. We define this frequency as fs(65kHz selected here). We set maximum frequency (f_{max}) as about 110% fs. Frequency increases with the increasing of the output power. When the frequency reaches maximum frequency which is set by C_{FSET}, over power limitation takes place which makes output voltage can't be maintained, thus COMP is saturated and below OLP (over load protection) threshold (0.85V).

A unique digital timer method is employed in HFC0300 for over load protection (OLP). When COMP is lower than 0.85V which is considered as an error flag, the timer starts counting. If the error flag removes, the timer resets. If the timer overflows when the counting number reaches 6000, OLP will be triggered. This timer duration avoids triggering OLP function when the power supply is at start up or load transition phase. So output voltage should be established in less than 6000 switching cycles during startup.

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G. Transformer Design

G-1. Transformer Core Selection

An appropriate core for certain output power at the operating frequency needs to be selected. Ferrite is usually preferred for flyback transformer. The core area product (A_EA_W) which is the core magnetic cross-section area multiplied by window area available for winding, is widely used for an initial estimate of core size for a given application. A rough indication of the required A_EA_W (cm^4) is given by following equation [1]:

$$A_E \cdot A_W = \left(\frac{L_m \cdot I_p \cdot I_{rms} \times 10^4}{B_{max} \cdot K_u \cdot K_j \cdot f_s} \right)^{4/3} cm^4 \quad (19)$$

Where K_u is winding factor which is usually 0.25~0.3 for an off-line transformer. K_j is the current-density coefficient (typically 400~450 for ferrite core). I_{peak} and I_{rms} is the maximum peak current and RMS current of the primary inductance, B_{max} is the allowed maximum flux density in normal operation which is usually preset to be the saturation flux density of the core material (0.3T~0.4T). f_s is the switching frequency at low line and full load condition. RMS current is given by following equation.

$$I_{rms} = \sqrt{\left[\left(\frac{I_{peak} + I_{valley}}{2} \right)^2 + \frac{1}{12} \left(I_{peak} - I_{valley} \right)^2 \right] \cdot D} \quad (20)$$

For power supply at DCM, I_{valley} equals to 0.

G-2. Primary and Secondary Winding Turns

With a given core size, equation (21) defines a minimum value of N_P for the transformer primary winding to prevent the core from saturation:

$$N_p = \frac{L_m \cdot I_{peak}}{A_E \cdot B_{max}} \quad (21)$$

Where:

L_m is the primary side inductance of the transformer

B_{max} is the maximum allowable flux density

A_E is the effective cross sectional core

I_{peak} is the peak current in the primary side of the transformer

The maximum allowable flux density B_{max} should be smaller than the saturation flux density B_{sat}. Since B_{sat} decreases as the temperature increases, which should be considered in the design.

Secondary winding turns N_s is a function of N and N_P, which is given by equation (22).

$$N_s = \frac{N_p}{N} \quad (22)$$

G-3. Wire Size

Once all the winding turns are determined, the wire size should be properly chosen to minimize the winding conduction loss and leakage inductance. The winding loss depends on the RMS current value, the length and the cross section of wire, also the transformer structure.

The wire size could be determined by the RMS current of the winding. For a flyback converter, the RMS current on primary side is given by equation (23), and the RMS current on secondary side is given by equation (23).

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$$I_{sec_rms} = N * \sqrt{\left[\left(\frac{I_{peak}+I_{valley}}{2}\right)^2 + \frac{1}{12}\left(I_{peak}-I_{valley}\right)^2\right]\cdot(1-D)} \quad (23)$$

For flyback operated at DCM, I_{valley} equals to 0.
Then, the wire size required on primary and secondary side is got by equation (24) and equation (25)

$$S_{pri} = \frac{I_{pri_rms}}{J} \quad (24)$$

$$S_{sec} = \frac{I_{sec_rms}}{J} \quad (25)$$

Here J is the current density of the wire which is 450A/cm^2 typically.
Due to the skin effect and proximity effect of the conductor, the diameter of the wire should be less than 2*Δd (Δd: skin effect depth):

$$\Delta d = \sqrt{\frac{1}{\pi \cdot f_s \cdot \mu \cdot \sigma}} * 10^3 (mm) \quad (26)$$

Where μ is the magnetic permeability of the conductor, which usually equals to the permeability of vacuum for most conductor, i.e. $4\pi \times 10^{-7}$ H/m, σ is the conductivity of the wire (for copper, σ is typically 6×10^7 S/m at 0 deg, σ will increases as temperature increases, which means the Δd will get smaller).

If the required size of the winding is larger than Δd, multiple strands of thinner wire or Litz wire is usually adopted to minimize the AC resistance. The effective cross section area of multi-strands wire or Litz wire should be large enough to meet the requirement set by the current density.
After the wire sizes have been determined, it is necessary to check whether the window area with selected core can accommodate the windings calculated in the previous steps. The window area required by each winding should be calculated respectively and added together, the area for inter-winding insulation, bobbin and spaces existing between the turns should also be taken into consideration. The fill factor, means the winding area to the whole window area of the core, should be well below 1 due to these inter-winding insulation and spaces between turns. It is recommended that a fill factor no greater than about 30% be used. For transformers with multiple outputs this factor may need to be reduced further.

Based on these considerations, the total required window area is then compared to the available window area of a selected core. If the required window area is larger than the selected one, either wire size must be reduced, or a larger core must be chosen. Of course, a reduction in wire size increases the copper loss of the transformer.

G-4. Air Gap

With the selected core and winding turns, the air gap of the core is given as equation (27):

$$l_a = \frac{\mu_0 * N_p^2 * A_E}{L_m} - \frac{l_c}{\mu_r} \quad (27)$$

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Where A_E is the cross sectional area of the selected core, μ_0 is the permeability of vacuum which equals $4\pi \times 10^{-7}$ H/m. L_m and N_P is the primary winding inductance and turns respectively, l_c is the core magnetic path length and μ_r is the relative magnetic permeability of the core material. For Ferrite core, μ_r is very large, so l_a can be approximately calculated as equation (28).

$$l_a = \frac{\mu_0 * N_p^2 * A_e}{L_m} \tag{28}$$

H. Ramp Compensation Circuit

If the power supply is designed to operate at CCM and the duty cycle is larger than 0.5, the ramp compensation circuit should be added to avoid sub-oscillation with peak current mode control. Usually, the ramp compensation rate is selected as equation (29)

$$k = \alpha * \frac{V_0 * N * R_{sense}}{L_m} \tag{29}$$

Where:

α is the coefficient which is usually 0.5~1.0

R_{sense} is the value of primary sense resistor

For HFC0300 application, the external ramp compensation circuit shown in Fig 12 is recommended.

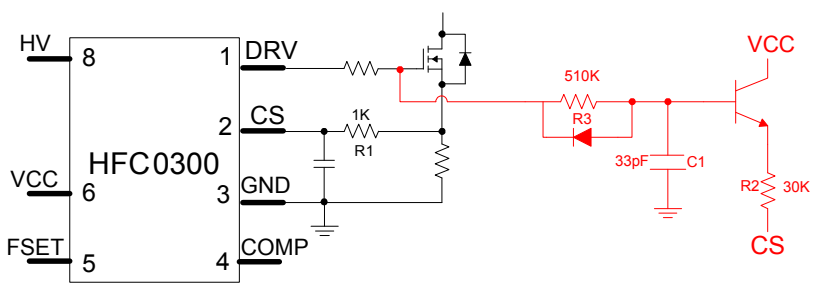

Figure 12— Ramp Compensation Circuit

The compensation rate added of above circuit could be got approximately as equation (28).

$$k \approx \frac{V_{DRV}}{\tau} * \frac{R_1}{R_2} \tag{30}$$

Where:

V_{DRV} is the drive voltage

$\tau = R_3 * C_1$

τ should be selected to be larger than the switching period, so the ramp added is linear approximately.

I. Design the RCD Snubber

The voltage spikes caused by the leakage inductance L_k during switch turn-off should be suppressed to an acceptable level to protect the switch. The RCD snubber is usually adopted to suppress the spike. The RCD clamp circuit and key waveforms are shown in Figure 13 and Figure 14 respectively. The RCD snubber circuit absorbs the energy in the leakage inductor when V_{ds} exceeds V_{in}+V_{sn}. It is assumed that

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the snubber capacitance is large enough thus its voltage is constant during one switching period.

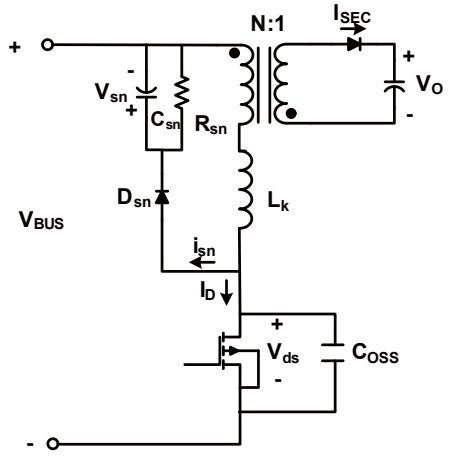

Figure 13— Flyback Converter with RCD Snubber

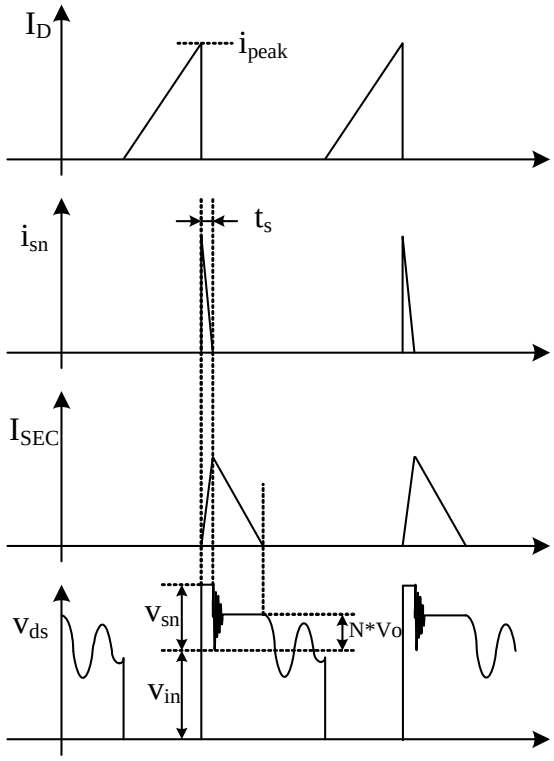

Figure 14— Key Waveforms

When the MOSFET turns off and V_{ds} is charged to $V_{in}+N*V_o$, the secondary diode turns on at the same time. The primary current continues to flow through the snubber diode (D_{sn}) to C_{sn}. The voltage stress of MOSFET is clamped to $V_{in}+V_{sn}$ .Therefore, the voltage across L_k is $V_{sn}-N*V_o$. The slope of i_{sn} is given by equation (31).

$$\frac{di_{sn}}{dt} = -\left(\frac{V_{sn} - N * V_o}{L_k}\right) \tag{31}$$

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Where i_{sn} is the current that flows into the snubber circuit, V_{sn} is the voltage across the snubber capacitor $C_{sn,}$ L_k is the leakage inductance of the main transformer. The time t_s is obtained by equation (32).

$$t_s = \frac{L_k}{V_{sn} - N * V_o} \times I_{peak} \tag{32}$$

Once V_{sn} is determined, the power dissipated in the snubber circuit is obtained by equation (33).

$$P_{sn} = V_{sn} \frac{i_{peak} \cdot t_s}{2} f_s = \frac{1}{2} L_k i_{peak}{}^2 \frac{V_{sn}}{V_{sn} - N * V_o} f_s \tag{33}$$

Where fs is the switching frequency. V_{sn} should be 1.5~2 times of $N*V_o$. Very small V_{sn} results in a severe loss in the snubber circuit, as indicated in equation (33).

On the other hand, since the power consumed in the snubber resistor (R_{sn}) is $V_{sn}{}^2/R_{sn,}$ the resistance is obtained by:

$$R_{sn} = \frac{V_{sn}{}^2}{\frac{1}{2} L_k i_{peak}{}^2 \frac{V_{sn}}{V_{sn} - N * V_o} f_s} \tag{34}$$

The snubber resistor with the proper rated power should be chosen based on the power loss. The maximum ripple of the snubber capacitor voltage is obtained equation (35).

$$\Delta V_{sn} = \frac{V_{sn}}{C_{sn} R_{sn} f_s} \tag{35}$$

Generally, 5~10% ripple is reasonable. Therefore, the snubber capacitance can be calculated.

J. Design the Output Filters

The voltage ripple at the output side can be estimated by:

$$\Delta V_o = \frac{I_o \cdot (T - T_{second})}{C_o} \tag{36}$$

Where T is switching period, C_o is output filter capacitance, and T_{second} is time duration of second current. The output capacitor can be electrolytic capacitor. If the electrolytic capacitor is used, due to its high ESR and ESL, a film capacitor or ceramic capacitor is usually paralleled to the electrolytic capacitor to provide a low impendence current path for high frequency current ripple. To further reduce the output voltage ripple, a small LC filter can be inserted between the output capacitor and output terminal.

4. DESIGN SUMMARY

- A detailed reference design of off-time controlled flyback converter with HFC0300 controller is shown in Figure 15. The input voltage is 90Vac to 265Vac and the output is 24V/1.5A.

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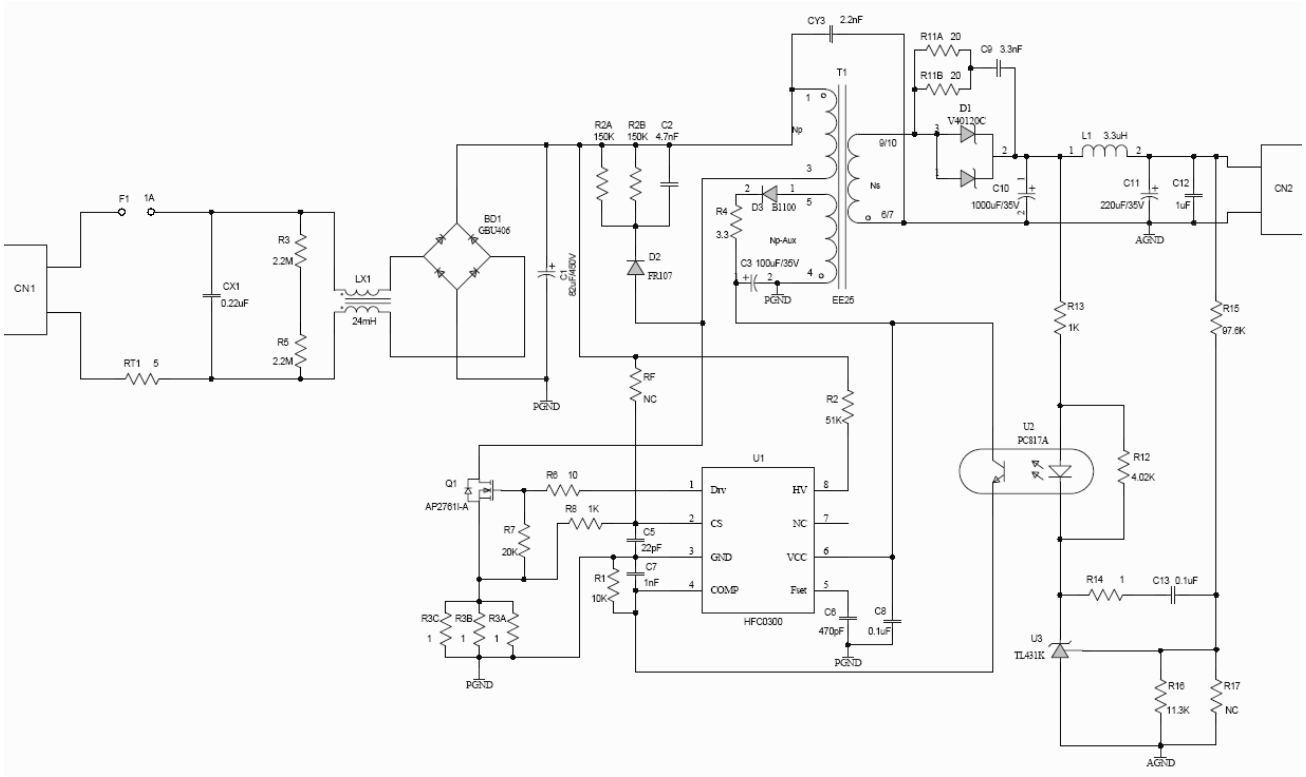

Figure 15— Schematic of Off-Time Flyback Converter with HFC0300

- The transformer used in this design has a turn ratio of 84:14:8 (N_p: N_s:N_{aux}) with 818uH primary inductance. The core selected is EE25. The wire structure is shown as Figure 16, 17 and Table 1.

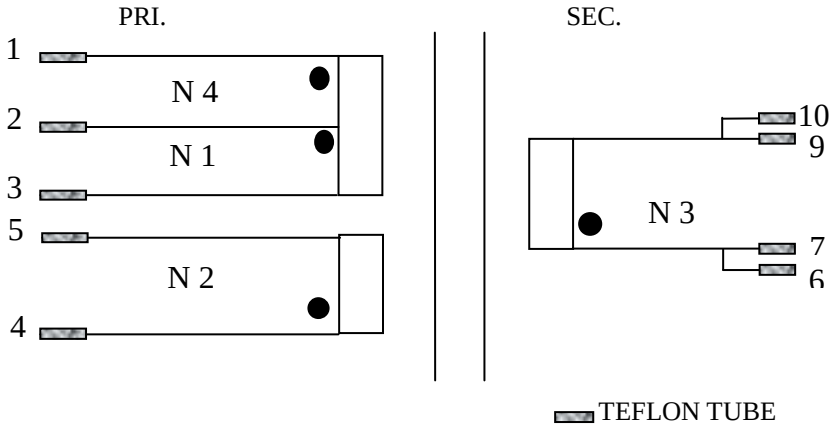

Figure 16— Connection Diagram

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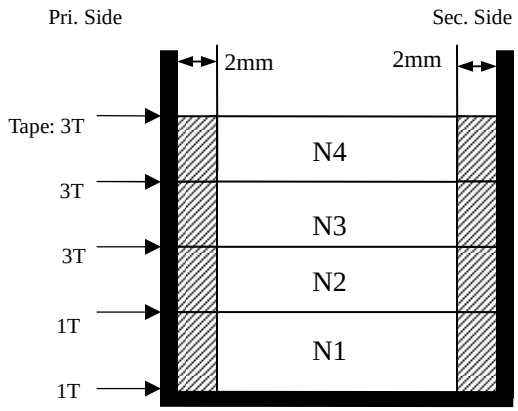

Figure 17— Winding Diagram

Tape(T)	Winding	Edge Tape (Pri.)	Terminal (start-end)	Edge Tape (Sec.)	Wire size (φ)	Turns (T)
1						
	N1	2mm	3—〉2	2mm	0.3mm*1	42
1						
	N2	2mm	5—〉4	2mm	0.2mm*1	8
3						
	N3	2mm	9,10—〉6,7	2mm	0.3mm*5	14
3						
	N4	2mm	2—〉1	2mm	0.3mm*1	42
3						

Table 1— Winding Order

5. EXPERIMENTAL VERIFICATION

To verify design procedure presented in this application note and the performance, a prototype based in Fig 15 is built and tested with specified input/output condition(Input: 90VAC~265VAC; Output: 24V/1.5A). The converter is designed to operate at BCM at 90Vac input and full load. Figure 18 and Figure 19 shows the current and Drain voltage waveform of primary MOSFET. Figure 20 shows the Burst Mode function of the controller at light load. To minimize power dissipation at no load or light load, the HFC0300 enters burst-mode operation. As the load decreases, the COMP voltage increases. The HF0300 skips switching cycles when the COMP voltage increases over the threshold VBURH—3.2V. And the output voltage starts to drop which causes the COMP voltage to decrease again. Once the COMP voltage falls below the threshold VBURL—3.1V, the switching resumes. The COMP voltage then falls and rises repeatedly. The burst mode operation alternately enables and disables switching cycles of the MOSFET thereby reducing switching loss in the no load or light load conditions.

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Figure 21 shows over load protection function. When COMP is low, the controller stops switching after 6000 switching cycles (about 100ms for this application)

Figure 22 shows the measured efficiency. From the efficiency curve, the efficiency is still high at light load condition due to decreased switching frequency. Also the power consumption at no load is given in Table 2. Due to the burst mode operation, the power loss at no load condition is very small, even at high line input.

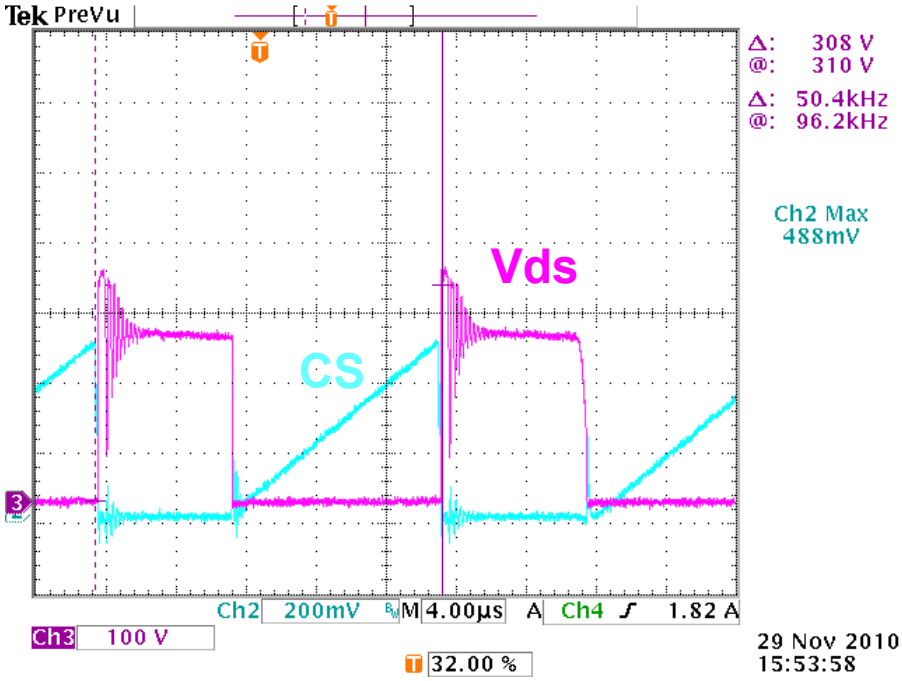

Figure 18— Drain Voltage and Current of MOSFET at Low Line Input (90Vac) (CH2: CS; CH3: Vds)

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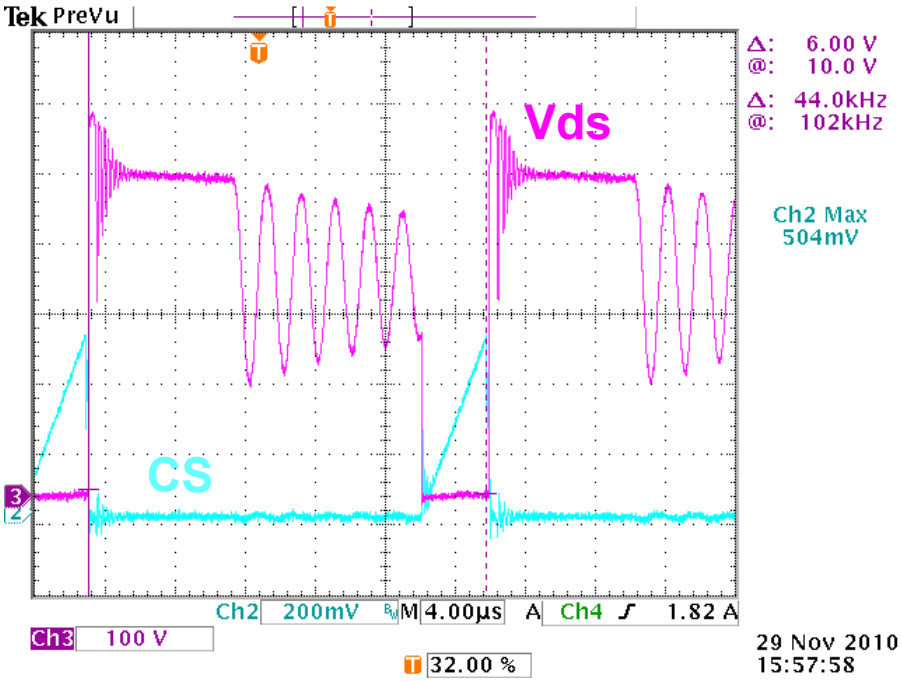

Figure 19— Drain Voltage and Current of MOSFET at High Line Input (230Vac) (CH2: CS; CH3: Vds)

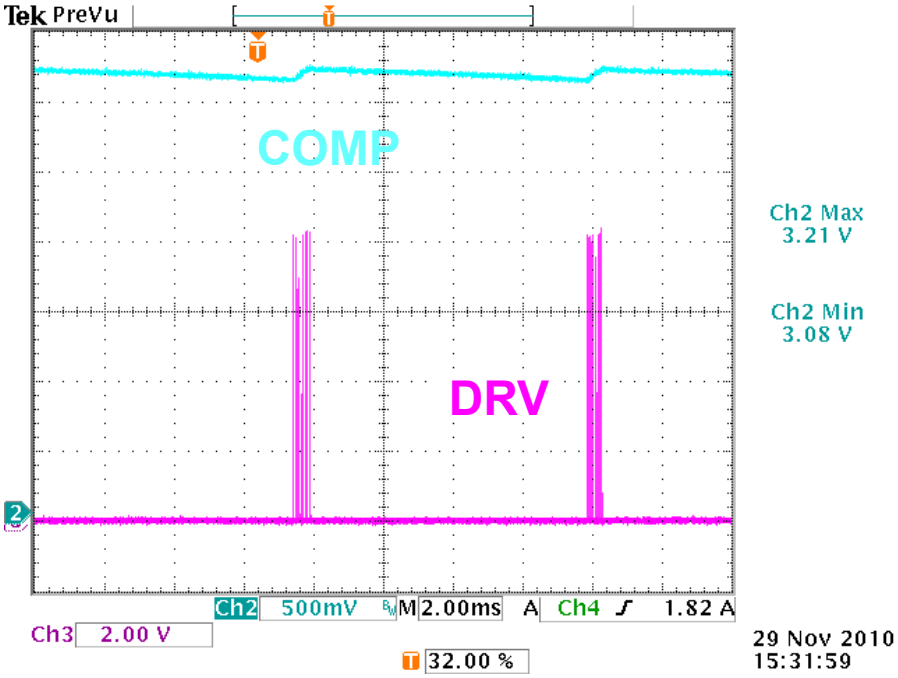

Figure 20— Burst Mode Function of HFC0300 (CH2: COMP; CH3: DRV)

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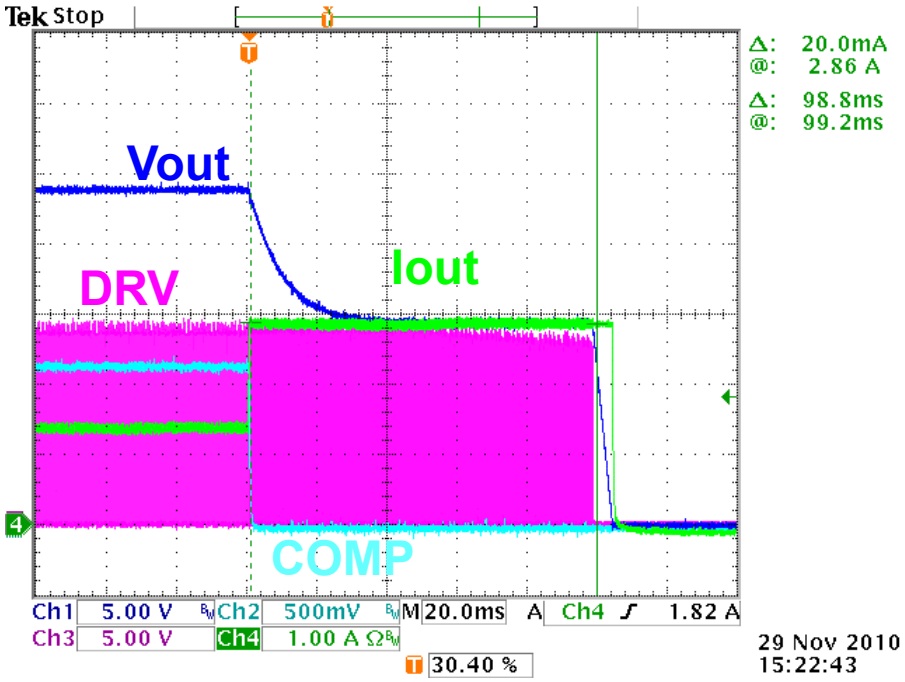

Figure 21— Over Load Protection of HFC0300

(CH1: Vout; CH2: COMP; CH3: DRV; CH4: Iout)

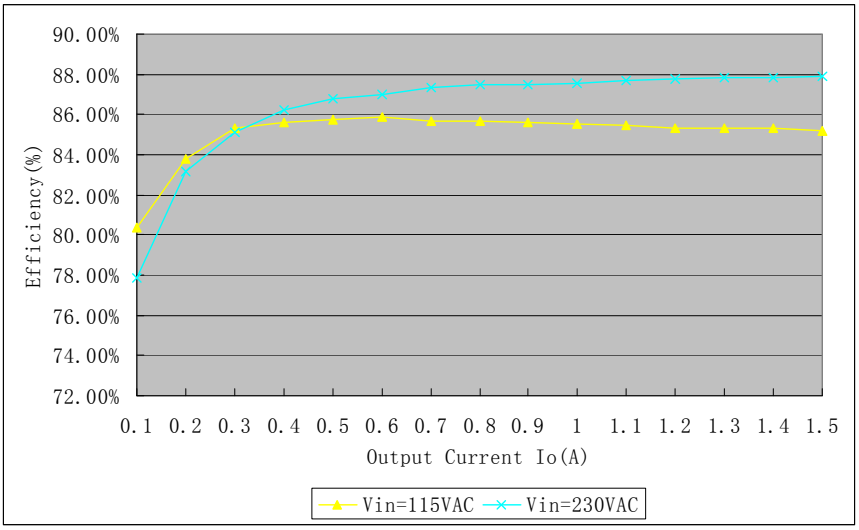

Figure 22— Measured Efficiency of the Prototype

Input voltage (Vac, RMS)	90	115	230	265
Power loss (mW)	74.4	77.2	110.1	121.9

Table 2— No Load Loss at Different Line Voltage

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6. REFERENCE

[1]. Lloyd H. Dixon, “Magnetics Design for Switching Power Supplies,” in Unitrode Magnetics Design Handbook, 1990.

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