



AN233

**Surface-Mount Guidelines for MPM Power
Modules with BGA/LGA Packages**

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ABSTRACT

This application note provides a comprehensive discussion on the key assembly considerations for MPM power module with BGA and LGA packages. It covers the design and manufacturing requirements to ensure optimal performance, reliability, and long-term usability in various electronic applications. Proper handling, PCB design, and rework strategies are crucial in mitigating defects and maximizing assembly efficiency.

Introduction

Ball grid array (BGA) and land grid array (LGA) packages are widely used in modern electronic assemblies due to their ability to support high-density integration. While BGA packages utilize solder balls for connection, LGA packages rely on direct pad contact. Ensuring proper assembly techniques for these packages is vital for product longevity and performance. This application note details the necessary steps to achieve a successful and robust assembly.

Package Construction

BGA and LGA Package Overview

The BGA package is designed with a solder ball matrix that facilitates mechanical and electrical connectivity. This design improves self-alignment during reflow soldering due to the surface tension of the molten solder balls. In contrast, LGA packages do not have pre-applied solder balls and instead depend on solder paste applied to the PCB (see Figure 1). The benefits of LGA packages include:

- Easier handling since no solder balls are required (leadless packages).
- A lower height compared to the same product designed with a BGA package due to not having solder balls in the construction.
- Flexibility. A single LGA power module product can feature pads with different sizes based on the pin requirements.

This makes LGA packages more sensitive to variations in stencil design and solder paste deposition.

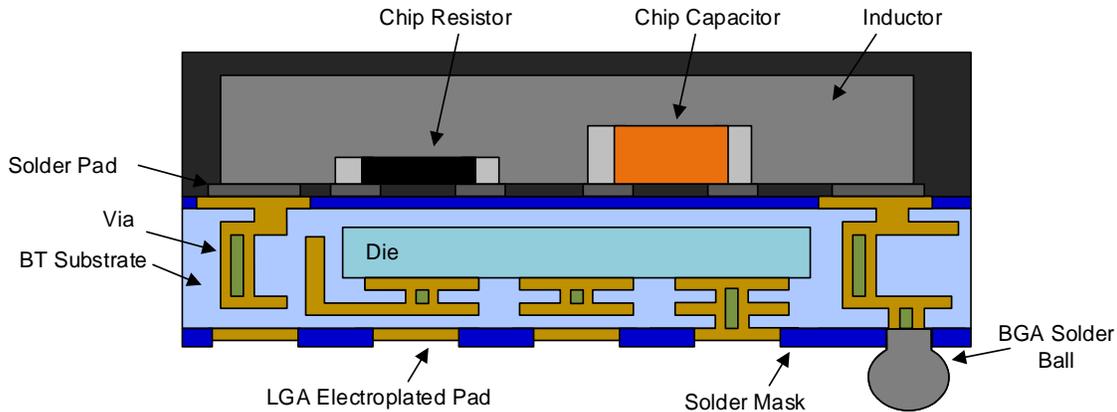


Figure 1: LGA and BGA Package Construction

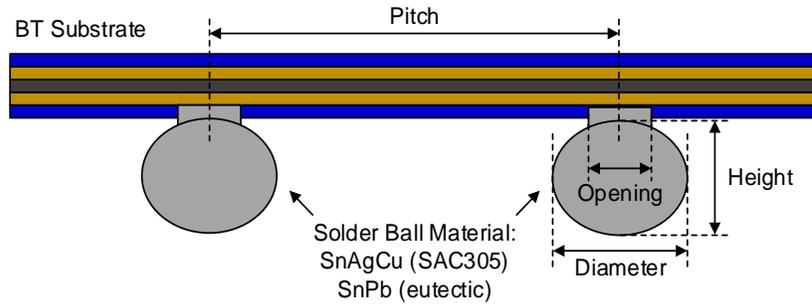
BGA Pad and Ball Geometry

BGA pad pitch varies between 0.65mm and 1.27mm, with corresponding pad and ball dimensions to ensure proper attachment (see Table 1).

Table 1: BGA Solder Ball Dimensions

BGA Pad Pitch (P)	Pad Opening (A)	Solder Ball Diameter (B)	Solder Ball Height (H)
0.65	0.35	0.30	0.25
0.80	0.40	0.45	0.35
1.00	0.45	0.50	0.37
1.27	0.63	0.75	0.60

The solder balls are typically composed of SnAgCu (SAC305) for lead-free applications or SnPb for legacy applications, with sizes tailored to specific pitch requirements (see Figure 2 on page 6).


Figure 2: BGA Solder Ball Geometry

LGA Pad Finishing

LGA pads are typically finished with electroplated nickel and gold or electroless nickel electroless palladium immersion gold (ENEPIG). These finishes enhance solderability and ensure consistent electrical connections. The nickel thickness ranges from 3 μm to 15 μm , while the gold layer is typically between 0.1 μm to 1.0 μm , ensuring reliable bonding to the solder paste (see Table 2).

Table 2: LGA Pad Finishing Dimensions

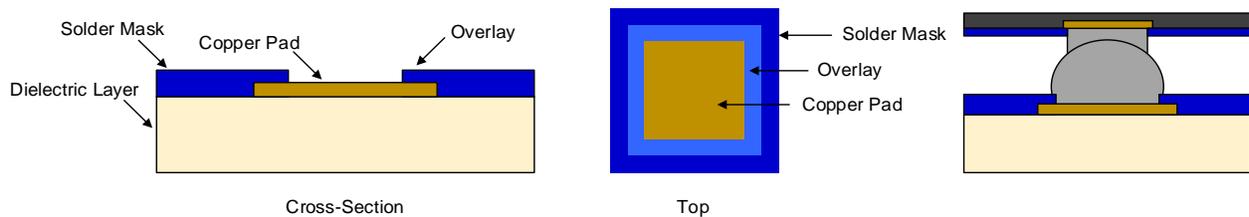
Finish Type	Nickel (Ni) Thickness	Gold (Au) Thickness	Palladium (Pd) Thickness
Electroplating	3 μm to 15 μm	0.1 μm to 1.0 μm	N/A
ENEPIG	2 μm to 8 μm	0.05 μm to 0.15 μm	0.05 μm to 0.15 μm

PCB Design Guidelines

A well-designed PCB is essential for ensuring reliable electrical connections, manufacturability, and long-term performance of BGA and LGA packages. Several aspects need to be carefully considered during the PCB layout process, including pad designs, solder mask definitions, and signal integrity.

SMD Pad Design

Solder mask defined (SMD) pad design features a solder mask layer partially laying on the edge of the PCB pad (see Figure 3). The solder mask opening is slightly smaller than the pad size, which creates an overlay area between the solder mask layer and the pad layer. SMD pad design offers several benefits — for example, the overlapping solder mask helps to prevent the pads from lifting off of the PCB surface due to thermal or mechanical stress. However, SMD pad design also presents drawbacks, namely that the overlapping area creates additional interfaces, which is not good for thermal-mechanical stress management during system-level application.


Figure 3: SMD Pad Diagram

NSMD Pad Design

For a non-solder mask defined (NSMD) pad, the solder mask layer is designed with a gap between the solder mask and copper pad (see Figure 4 on page 7). With this pad type, the copper pad area for solder paste printing is only defined by the dimension of copper pad itself, and not by the solder mask. Since NSMD pads have all the solder paste connected to the entire pad, NSMD pad designs feature better solder connections and solder joint reliability. However, the pad also tends to be easier to lift off from the PCB during assembly or under special operation conditions.

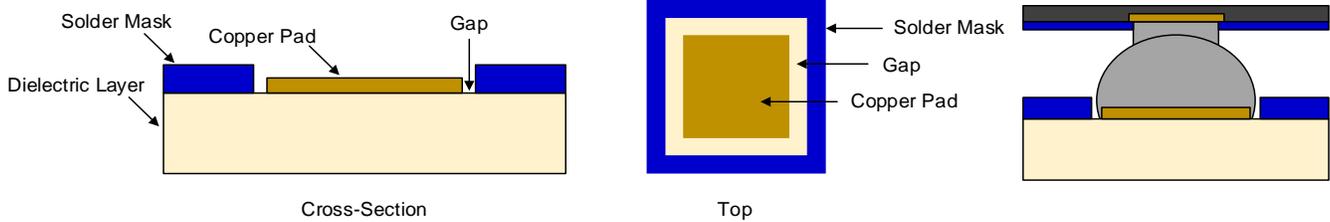

Figure 4: NSMD Pad Diagram

Table 3 and Table 4 show the dimensions of SMD and NSMD pads and solder mask openings. Table 3 shows the dimensions for BGA round pads, while Table 4 shows the dimensions for LGA square pads.

Table 3: BGA PCB Pad Layout (Round Pads)

Pitch (P) (mm)	SMD Pads - Metal Pad Size (B) (mm)	SMD Pads - Solder Mask Opening (A) (mm)	NSMD Pads - Metal Pad Size (B1) (mm)	NSMD Pads - Solder Mask Opening (A1) (mm)
0.65	≥ 0.45	0.35	0.35	≥ 0.45
0.80	≥ 0.50	0.40	0.40	≥ 0.50
1.00	≥ 0.60	0.50	0.50	≥ 0.60
1.27	≥ 0.73	0.63	0.63	≥ 0.73

Table 4: LGA PCB Pad Layout (Square Pads)

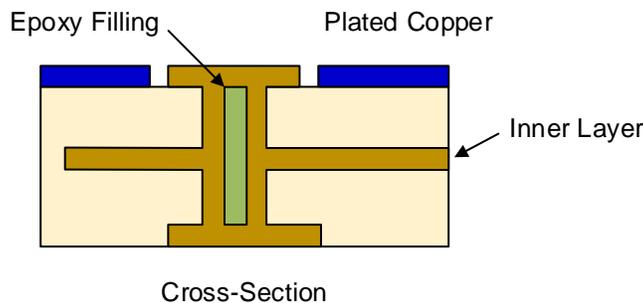
Pitch (P) (mm)	SMD Pads - Metal Pad Size (B) (mm)	SMD Pads - Solder Mask Opening (A) (mm)	NSMD Pads - Metal Pad Size (B1) (mm)	NSMD Pads - Solder Mask Opening (A1) (mm)
1.27	≥ 0.73	0.630	0.630	≥ 0.73

Via-in-Pad Design

To improve thermal management and electrical functions, through vias or buried vias are typically placed underneath the copper pad on the PCB; this is known as a “via-in-pad” design (see Figure 5). A via-in-pad design has impacts on the PCBA process, such as the solder paste print.

Open thermal vias can be placed directly under the pad. There are multiple methods to improve soldering performance:

- Move the via under the area covered by the solder mask, if the thermal and electrical performance is not significantly affected.
- Fill the vias with copper, epoxy, or other equivalent materials. Note that this approach may increase the cost of PCB manufacturing.


Figure 5: Via-in-Pad Structural Diagram

BGA PCB Pad Layout

For BGA packages, solder mask-defined (SMD) pads are generally recommended because they provide better control over solder joint formation. The pad size and solder mask openings must be carefully

defined to prevent solder bridging or insufficient attachment. It is important to maintain proper spacing between pads to ensure adequate solderability and reduce the risk of electrical shorts. The copper pad diameter should align with the ball size to achieve optimal wetting during the reflow process.

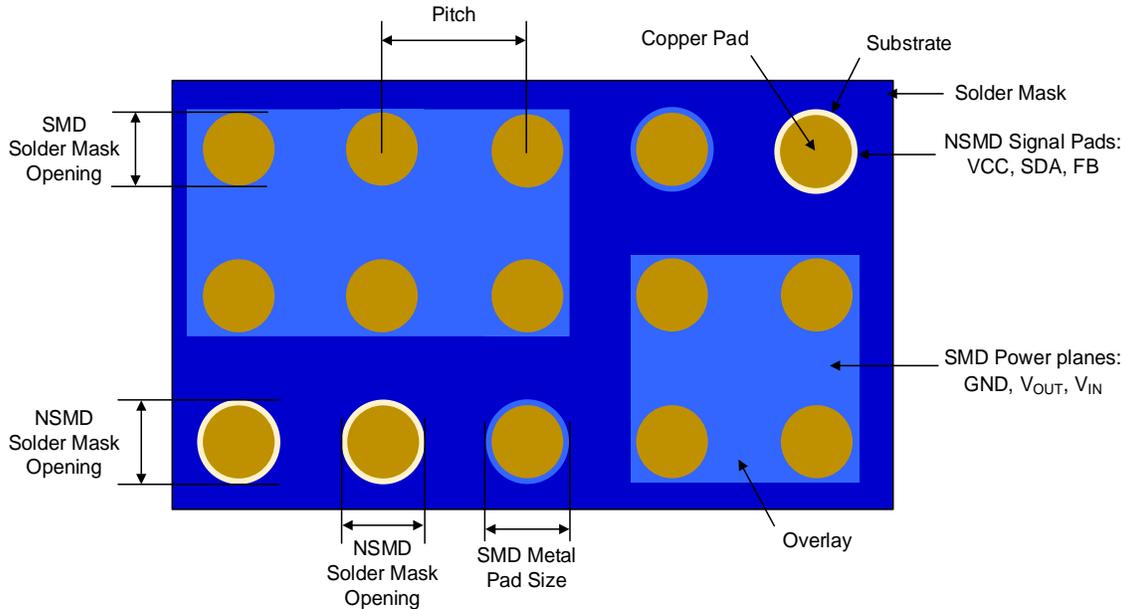


Figure 6: BGA SMD and NSMD Pad Recommendation

LGA PCB Pad Layout

A mixed pad design is typically recommended for better reliability when designing for MPS power modules in LGA packages, especially for high-current applications.

Because limited power goes through signal pins, they suffer less thermal and mechanical stresses, so an NSMD pad design is usually selected to enable better solder connections and solder joint reliability.

On the contrary, a large copper area is required for the power pads, especially for modules with high-power capability. Power pads are also subject to severe thermal and mechanical stresses, so an SMD pad design is recommended.

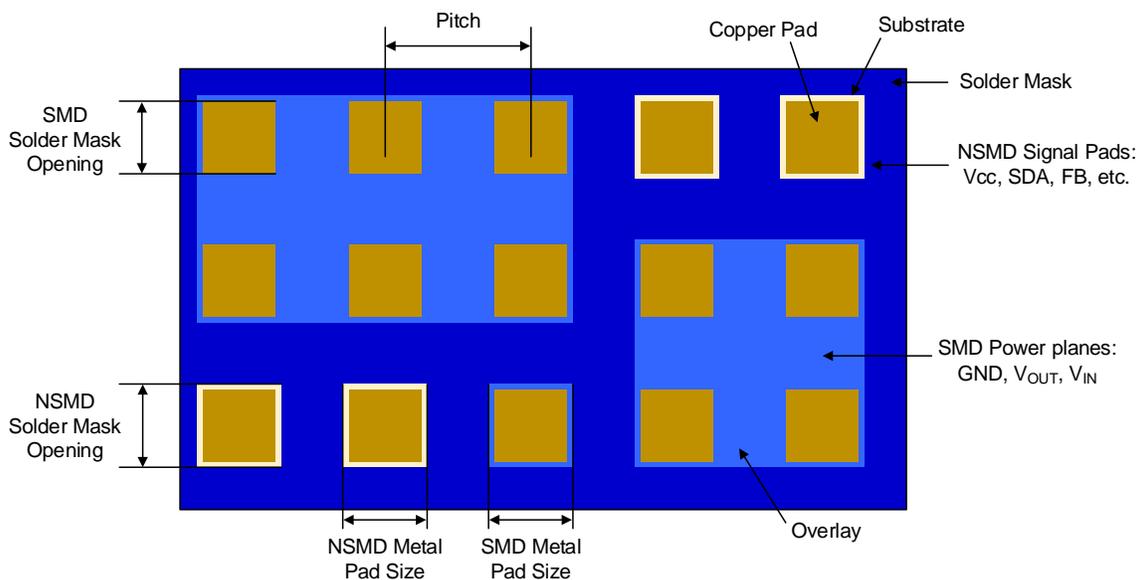


Figure 7: LGA SMD and NSMD Pad Recommendation

Figure 8 shows a PCB design example with a mixed pad design. This design is for the MPM54304, which has a LGA-33 (7mmx7mmx2mm) package. All of the power pads — including the large GND pad in the middle — utilize SMD design. Meanwhile, all the signal pads — including FB, SDA, and SCL — utilize NSMD design.

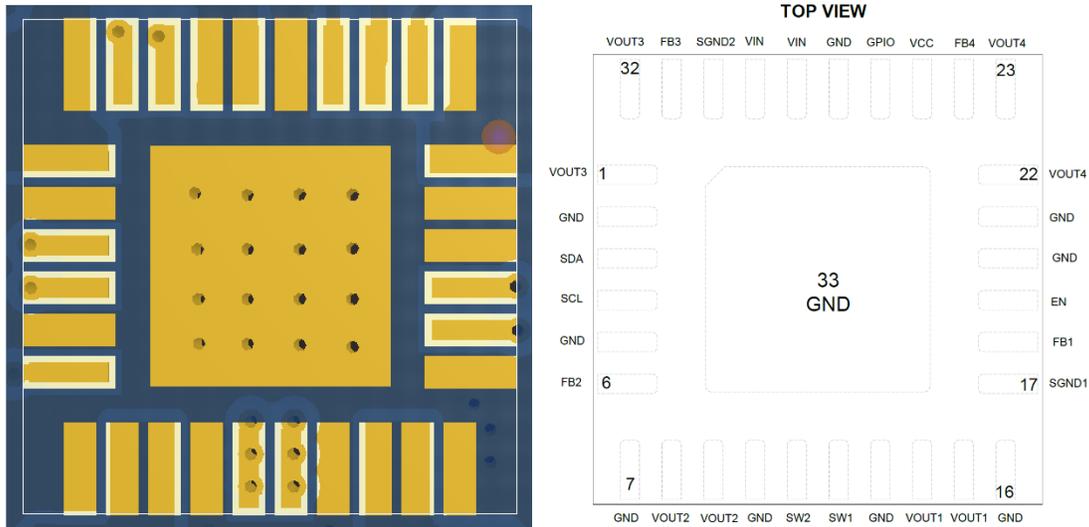


Figure 8: MPM54304 Footprint Example

PCB Plane Separation and Isolator Pad Design

To maintain signal integrity and prevent unintended electrical interactions, PCB plane separation should be properly designed (see Figure 9). High-frequency applications require controlled impedance routing, and power and ground planes should be positioned strategically to minimize noise and interference.

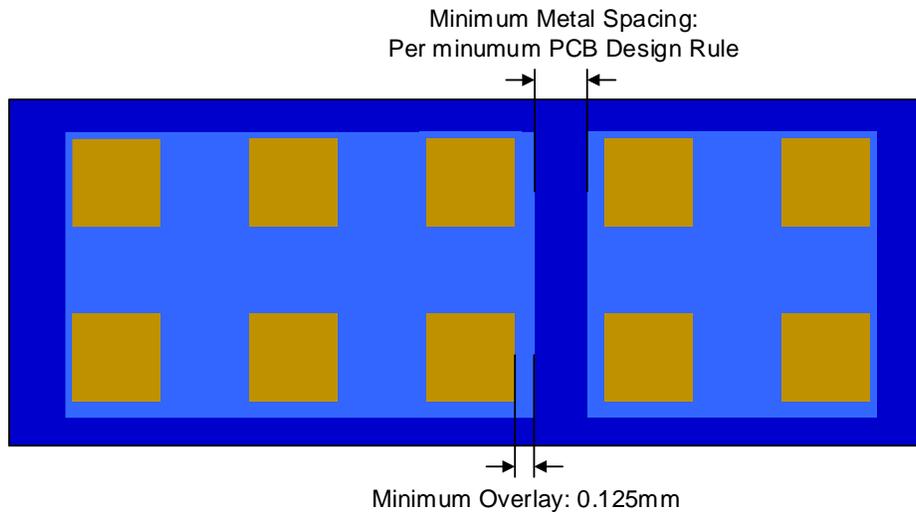


Figure 9: Plane Separation Recommendation

Via Placement and Routing Considerations

For BGAs and LGAs, via placement is crucial to maintaining signal integrity and manufacturing feasibility. Vias should not be placed too close to pad edges, as this can lead to solder wicking and weak solder joints. In high-density applications, via-in-pad technology can be used but requires appropriate via filling and capping techniques to prevent solder voids. Routing should be optimized to minimize trace length and impedance discontinuities, ensuring stable electrical performance (see Figure 10 on page 10).

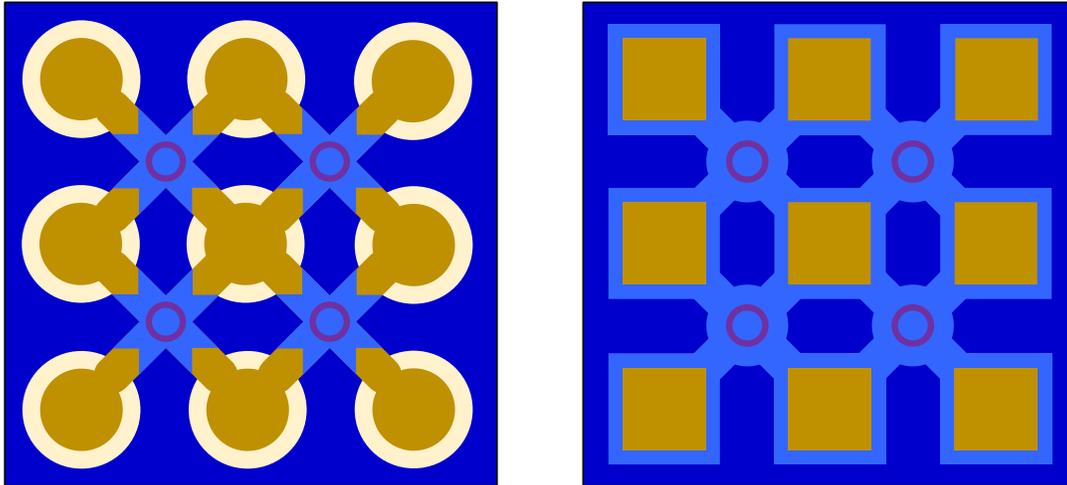


Figure 10: LGA and BGA Thermal Relief via Layout Recommendation

Solder Paste Application Considerations

For both BGA and LGA packages, precise solder paste application is essential. Inconsistent solder paste deposition can lead to open connections or excessive voiding. The stencil thickness, aperture size, and paste type should be carefully selected to achieve uniform and reliable solder joints. For ultra-fine pitch components, step stencils or electroformed stencils may be required to control paste volume accurately.

Moisture Sensitivity Considerations

All plastic IC packages tend to absorb moisture. During surface-mount assembly, this moisture can vaporize when subjected to the heat associated with solder reflow operations. Vaporization creates internal stresses that can cause the plastic molding compound to crack. This cracking process is commonly referred to as the “popcorn effect.”

Cracks in the plastic molding may cause internal damage or may allow contamination to penetrate to the die, which can reduce the semiconductor device’s reliability.

Since plastic packages absorb moisture, care must be taken to prevent exposure to humid conditions greater than 10% relative humidity (RH) for extended periods of time prior to surface mount reflow processing. If exposed to excessive moisture, the devices should be baked to remove moisture prior to solder reflow operations.

All MPS surface-mount ICs have a moisture sensitivity level and peak reflow classification. This information is displayed on the reel, moisture barrier bag (MBB), and box packing. MPS power modules conform to IPC/JEDEC J-STD-020 standards, with an MSL rating of either 3 or 4. Figure 11 on page 11 shows an example of the labels used in MPS shipments.

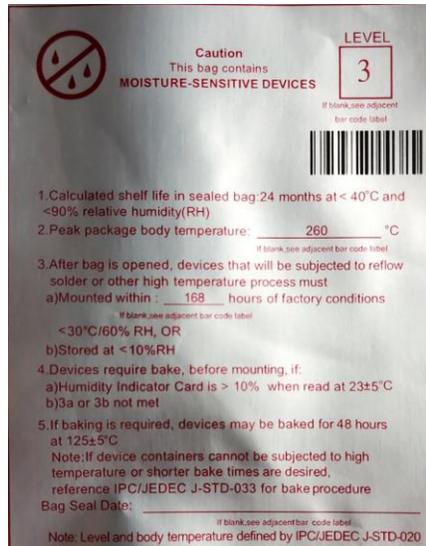


Figure 11: MSL and Moisture Label Examples

Dry Packing Requirements

Table 5 shows the dry-packing requirements for the various moisture sensitivity levels.

Table 5: Dry Packing Requirements

MSL Level	Dry Before Bag	MBB with HIC	Desiccant	MSID Label	Caution Label
1	Optional	Optional	Optional	Not Required	Not required if classified at 220°C to 225°C. Required if classified at temperature other than 220°C to 225 °C.
2	Optional	Required	Required	Required	Required
2a-5a	Required	Required	Required	Required	Required
6	Optional	Optional	Optional	Required	Required

Floor Life

The floor life of SMDs will be modified by environmental conditions other than 30°C/60% RH (see Table 6).

Table 6: Moisture Classification Level and Floor Life

MSL Level	Floor Life (Out of Bag) at ≤30°C/60% RH
1	Unlimited
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.

Drying of SMD Devices

SMD devices classified at MSL Levels 2 through 5a exceeds floor life may be adequately dried by baking according to Table 7 on page 12 (for re-bake prior to reflow) or Table 8 on page 13 (for drying prior to dry packing).

Table 7: Reference Conditions for Drying Mounted or Unmounted SMD Packages (User Bake: Floor Life Begins Counting at Time = 0 After Bake) ⁽¹⁾

Package Body ⁽³⁾	MSL Level	Bake at 125°C +10/-0°C <5% RH		Bake at 90°C +8/-0°C ≤5% RH		Bake at 40°C +5/-0°C ≤5% RH	
		Exceeding Floor Life by >72h	Exceeding Floor Life by <72h	Exceeding Floor Life by >72h	Exceeding Floor Life by <72h	Exceeding Floor Life by >72h	Exceeding Floor Life by <72h
Thickness ≤0.5 mm ⁽⁵⁾	2	Not Required ⁽⁴⁾	Not required ⁽⁴⁾	Not required ⁽⁴⁾	Not required ⁽⁴⁾	Not required ⁽⁴⁾	Not required ⁽⁴⁾
	2a	1 hour	1 hour	2 hours	1 hour	12 hours	8 hours
	3	1 hour	1 hour	3 hours	1 hour	22 hours	8 hours
	4	1 hour	1 hour	3 hours	1 hour	22 hours	8 hours
	5	1 hour	1 hour	3 hours	1 hour	23 hours	8 hours
	5a	1 hour	1 hour	4 hours	1 hour	26 hours	8 hours
Thickness >0.5mm, ≤0.8 mm ⁽⁵⁾	2	Not required ⁽⁴⁾	Not required ⁽⁴⁾	Not required ⁽⁴⁾	Not required ⁽⁴⁾	Not required ⁽⁴⁾	Not required ⁽⁴⁾
	2a	4 hours	3 hours	15 hours	13 hours	4 days	3 days
	3	4 hours	3 hours	15 hours	13 hours	4 days	3 days
	4	4 hours	3 hours	16 hours	13 hours	4 days	3 days
	5	4 hours	3 hours	16 hours	13 hours	4 days	3 days
	5a	4 hours	3 hours	16 hours	13 hours	4 days	3 days
Thickness >0.8mm, ≤1.4 mm ⁽⁵⁾	2	Not required ⁽⁴⁾	Not required ⁽⁴⁾	Not required ⁽⁴⁾	Not required ⁽⁴⁾	Not required ⁽⁴⁾	Not required ⁽⁴⁾
	2a	8 hours	6 hours	25 hours	20 hours	8 days	7 days
	3	8 hours	6 hours	25 hours	20 hours	8 days	7 days
	4	9 hours	6 hours	27 hours	20 hours	10 days	7 days
	5	10 hours	6 hours	28 hours	20 hours	11 days	7 days
	5a	11 hours	6 hours	30 hours	20 hours	12 days	7 days
Thickness >1.4 mm, ≤2.0 mm	2	18 hours	15 hours	63 hours	2 days	25days	20 days
	2a	21 hours	16 hours	3 days	2 days	29 days	22 days
	3	27 hours	17 hours	4 days	2 days	37 days	23 days
	4	34 hours	20 hours	5 days	3 days	47 days	28 days
	5	40 hours	25 hours	6 days	4 days	57 days	35 days
	5a	48 hours	40 hours	8 days	6 days	79 days	56 days
Thickness >2.0mm, ≤4.5mm	2	48 hours	48 hours	10 days	7 days	79 days	67 days
	2a	48 hours	48 hours	10 days	7 days	79 days	67 days
	3	48 hours	48 hours	10 days	8 days	79 days	67 days
	4	48 hours	48 hours	10 days	10 days	79 days	67 days
	5	48 hours	48 hours	10 days	10 days	79 days	67 days
	5a	48 hours	48 hours	10 days	10 days	79 days	67 days
Exception for BGA Package 17mmx17mm or Any Stacked Die Package	2 -5a	96 hours ^{(2) (5)}	As above per package thickness and moisture level	Not applicable	As above per package thickness and moisture level	Not applicable	As above per package thickness and moisture level

Notes:

- 1) Table 7 and Table 8 on page 13 are based on the worst-case molded lead frame SMD packages. In most cases this data is applicable to other non-hermetic surface mount SMD packages. Users may reduce the actual bake time if technically justified (e.g. absorption/ desorption data, etc.). If parts have been exposed to > 60% RH, it may be necessary to increase the bake time by tracking desorption data to ensure that parts are dry.
- 2) For BGA packages >(17mmx17mm) that do not have internal planes that block the moisture diffusion path in the substrate, readers may use bake times based on the thickness/moisture level portion of the table.
- 3) If baking packages >4.5mm thick is required, refer to IPC/JEDEC J-SDT-033 appendix B.
- 4) Baking is not required if the floor life exposure is limited to < 30°C and < 60% RH for thin (<1.4mm) MSL2 devices. This is due to the moisture diffusion behavior of the thin devices, which were fully saturated after the absorption at MSL 2 (168 hours at 85°C/60% RH).
- 5) The bake times specified are conservative for packages without blocking planes or stacked die. For a stacked die or BGA package with internal planes that impede moisture diffusion, the actual bake time may be longer than what is required in Table 7.

Table 8 on page 13 shows default baking times.

Table 8: Default Baking Times Used Prior to Dry-Pack that were Exposed to Conditions $\leq 60\%$ RH (MET = 24h) ⁽¹⁾ ⁽⁶⁾

Package Body Thickness	Level	Bake at 125°C +10/-0°C	Bake at 150°C +10/-0°C
$\leq 1.4\text{mm}$	2	7 hours	3 hours
	2a	8 hours	4 hours
	3	16 hours	8 hours
	4	21 hours	10 hours
	5	24 hours	12 hours
	5a	28 hours	14 hours
$> 1.4\text{mm}, \leq 2.0\text{mm}$	2	18 hours	9 hours
	2a	23 hours	11 hours
	3	43 hours	21 hours
	4	48 hours	24 hours
	5	48 hours	24 hours
	5a	48 hours	24 hours
$> 2.0\text{mm}, \leq 4.5\text{mm}$	2	48 hours	24 hours
	2a	48 hours	24 hours
	3	48 hours	24 hours
	4	48 hours	24 hours
	5	48 hours	24 hours
	5a	48 hours	24 hours

Note:

6) If baking packages $> 4.5\text{mm}$ thick is required, see appendix B in IPC/JEDEC J-SDT-033.

Table 9 shows how to reset or pause the floor-life clock.

Table 9: Resetting or Pausing the Floor-Life Clock at User Site

MSL Level	Exposure Time at Temp/Humidity	Floor Life	Desiccator Time at Relative Humidity	Bake	Reset Shelf Life
2, 2a, 3, 4, 5, 5a	Anytime, $\leq 40^\circ\text{C}/85\%$ RH	Reset	N/A	See Table 7 on page 12	Dry pack after bake
2, 2a, 3, 4, 5, 5a	$>$ floor life, $\leq 30^\circ\text{C}/60\%$ RH	Reset	N/A	See Table 7 on page 12	Dry pack after bake
2, 2a, 3	$> 12\text{hrs}$, $\leq 30^\circ\text{C}/60\%$ RH	Reset	N/A	See Table 7 on page 12	Dry pack after bake
2, 2a, 3	$\leq 12\text{hrs}$, $\leq 30^\circ\text{C}/60\%$ RH	Reset	5x exposure time $\leq 10\%$ RH	N/A	N/A
2, 2a, 3	Cumulative time $<$ floor life, $\leq 30^\circ\text{C}/60\%$ RH	Pause	Anytime $\leq 10\%$ RH	N/A	N/A
4, 5, 5a	$> 8\text{hrs}$, $\leq 30^\circ\text{C}/60\%$ RH	Reset	N/A	See Table 7 on page 12	Dry pack after bake
4, 5, 5a	$\leq 8\text{hrs}$, $\leq 30^\circ\text{C}/60\%$ RH	Reset	10x exposure time $\leq 5\%$ RH	N/A	N/A

Shelf Life

MPS warrants the shelf life of its analog IC devices for five years based on the production date code, assuming the integrity of the seal has not been compromised during that time period and has been stored in environment of $< 40^\circ\text{C}/90\%$ RH.

Refer to the MPS International Ltd. Standard Terms and Conditions for other warranties applied to its products.

Board Assembly Process

Stencil Design

The stencil design is important for the assembly process of LGA-based MPS power modules, as it controls the thickness and volume of the solder paste applied on each LGA pad. Various processes and key parameters must be considered as part of the stencil design. When transferring solder paste, a state-of-the-art stencil with high-quality openings should always be favored in production.

The most common stencil thickness recommendation is between 4mil and 5.6mil, and the aperture on the stencil must follow the specifications of each package. For larger pads, (>1mm²), the aperture should be designed with multiple openings for better solder paste distribution. Table 10 shows the recommended stencil dimensions for a BGA package. Table 11 shows the recommended stencil dimensions for an LGA package with square pads. Table 12 shows the recommended stencil dimensions for an LGA package with round pads.

Table 10: Recommended Stencil Dimensions (BGA)

BGA Pad Pitch (mm)	Pad Opening (mm)	Stencil Opening (mm)	Stencil Thickness (mils)
0.65	0.35	0.33	4
0.80	0.40	0.38	4
1.00	0.50	0.48	4
1.27	0.63	0.60	4

Table 11: Recommended Stencil Dimensions (LGA — Square Pads)

LGA Pad Pitch (mm)	Pad Opening (mm)	Stencil Opening (mm)	Stencil Thickness (mils)
1.27	0.63	0.60	5
1.27	0.89	0.84	5
1.27	0.76	0.72	5

Table 12: Recommended Stencil Dimensions (LGA — Round Pads)

LGA Pad Pitch (mm)	Pad Opening (mm)	Stencil Opening (mm)	Stencil Thickness (mils)
0.65	0.35	0.33	4
0.80	0.40	0.38	4
1.00	0.50	0.48	5
1.27	0.63	0.60	5

PCB Surface Finish

PCB manufacturing is typically capable of various surface finishes based on the use requirements. Options include the following:

- Organic solderability preservative (OSP)
- Electroless nickel, immersion gold (ENIG)
- Electroplated nickel and gold
- Immersion silver
- Immersion tin

The design engineer, customer, or end user can choose their preferred surface finish based on the system requirements. MPS recommends using OSP, ENIG, and immersion tin for the best results. Each PCB finish must be evaluated according to the solder joint's reliability and manufacturing process.

Solder Paste

It is recommended to use SAC305 solder paste to comply with non-lead regulations for electronic products, as well as follow Rohs/REACH environmental directives. Type IV, no-clean solder paste is recommended for use with LGA-based MPS power modules.

Screen Printing

The solder paste's transfer efficiency from the stencil to the board during the printing process is determined by a large number of variables, including (but not limited to) the squeegee speed, pressure, and angle (see Figure 12). MPS recommends always following the solder paste supplier's recommendations for these parameters.

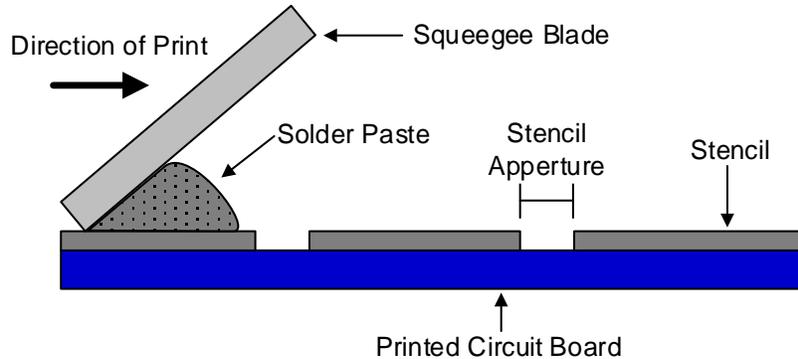


Figure 12: Screen Printer Diagram

Component Placement

The placement of LGA components is important for good assembly quality. It is recommended to use an automatic pick-and-place machine with a vision system. The accuracy for component placement should be adjusted to a maximum of $\pm 30\mu\text{m}$.

Reflow Profiles

The reflow profile is a critical factor in ensuring strong solder joints and preventing defects such as voiding, tombstoning, or cold solder joints. The recommended reflow profile must be carefully followed to achieve consistent results.

There are no special requirements for reflow soldering LGA components, but in the absence of other instructions, the reflow profile must follow the JEDEC standards. The JEDEC reflow profile sets different stages of SMT heating during component board assembly. Each stage has a minimum and maximum temperature range and time value range, which are used as guidelines for optimizing the temperature profile associated with the specific printed circuit assembly. Keep in mind that each assembly is customized and requires a unique reflow profile to achieve nominal results across the entire board. For more details, refer to the IPC/JEDEC J-STD-020D standard.

The actual profile parameters also depend upon the solder paste that is used. Follow the recommendations from the paste manufacturers.

It is recommended to use dry air as the reflow atmosphere, although Nitrogen can also be used. It is also recommended to monitor the temperature profile of the package's top surface to ensure that the package's peak temperature does not exceed the MSL classification(s) of individual devices.

An 8-zone reflow oven (or greater) with oxygen level control is recommended. MPS power modules cannot be reflowed more than three times. All MPS power modules are designed to withstand lead-free peak reflow temperatures.

Figure 13 on page 16 shows the typical recommended reflow profile. The profile includes several temperature zones, which each play a critical role in ensuring correct solder quality.

Temperature Zones

A typical reflow process consists of four main zones, described below.

- **Preheat Zone:** Gradually raises the temperature to avoid thermal shock.
- **Soak Zone:** Maintains a steady temperature to activate flux and evenly distribute heat.
- **Reflow Zone:** The peak temperature melts the solder, forming reliable joints.
- **Cooling Zone:** Gradually reduces the temperature to solidify solder joints.

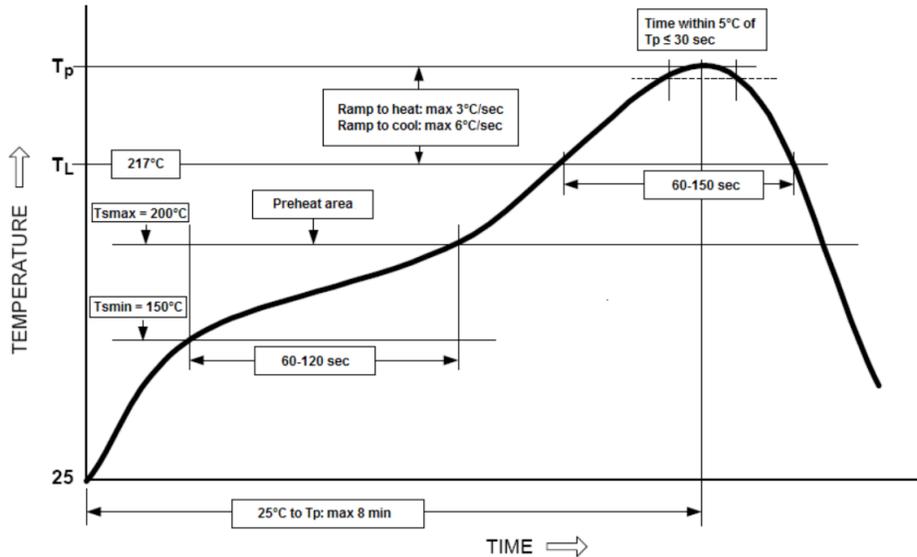


Figure 13: Temperature Profile Example

Table 13 shows the typical reflow profile parameters. The recommended profile and parameters meet IPC/JEDEC J-STD-020 specifications.

Table 13: Pb-Free Process — Package Peak Reflow Temperature

Package Thickness	Volume, <350mm ³	Volume, 350mm ³ to 2000mm ³	Volume, ≥ 2000mm ³
< 1.6mm	260 +0/-5°C	260 +0/-5°C	260 +0/-5°C
1.6mm to 2.5mm	260 +0/-5°C	250 +0/-5°C	245 +0/-5°C
≥ 2.5mm	250 +0/-5°C	245 +0/-5°C	245 +0/-5°C

Table 14: Reflow Profile

Profile Feature		Lead-Free Solder	Leaded Solder
Preheat	Min Soak Temperature (T _{SMIN})	150°C	100°C
	Max Soak Temperature (T _{SMAX})	200°C	150°C
	Soak Time (t _s)	60sec to 120sec	60sec to 120sec
Reflow	Liquidus Temperature (T _L)	217°C	183°C
	Time Above Liquidus (t)	30sec to 90sec	30sec to 90sec
Peak Package Body Temperature (T _P)		See Table 13	See Table 13
Time within 5°C of Peak Temp (t _P)		30sec max	30sec max
Average Ramp Up Rate (T _{SMAX} to T _P)		2.5°C/sec max	2.5°C/sec max
Ramp Down Rate		2.5°C/sec max (lower rate recommended)	2.5°C/sec max (lower rate recommended)
Time 25°C to Peak Temp		8min max	8min max

Cleaning

Since no-clean solder paste is typically used for MPS power modules in LGA packages, no cleaning procedure is required for MPS power module products.

If water-soluble paste has been used for an MPS power module, it is recommended to use a saponifier and/or deionized (DI) water spray system for the cleaning process. After cleaning, be sure to dry the board.

Refer to and follow the solder paste supplier's guidelines for cleaning.

Solder Joint Voids

Minimizing voids in solder joints is critical for electrical and thermal performance. Currently, there are no standards for solder joint voids for bottom-terminated components. MPS recommends a 25% maximum solder void for signal pads, and a 50% maximum solder void for large/thermal pads.

The solder paste manufacturer's recommended temperature profile is usually designed to optimize the activity of the flux and minimize voiding. However, in cases where excessive voids are observed, there are certain void-reduction strategies that can be utilized.

Void Reduction Strategies

Minimizing voids in solder joints is critical for electrical and thermal performance. The best practices include the following:

- Using low-voiding solder paste formulations.
- Adjusting reflow profile soak times to allow for better outgassing.
- Implementing vacuum-assisted reflow when necessary.
- Optimizing stencil design to control paste volume.
- Splitting larger pads into 0.5mmx0.5mm pads to facilitate outgassing.

The Effect of Stencil Design on Void Reduction

Voids in solder joints occur due to outgassing within the molten solder paste. As the flux turns to gas, it creates bubbles that may not be able to escape from the solder joint, leading to the apparition of voids. This phenomenon is directly proportional to the amount of solder paste used to create the solder joint, so large pads are particularly vulnerable to solder voids. Figure 14 shows a stencil design for MPM3695-25 where the power pads have one single large opening. Figure 14 also shows the X-ray of the resulting solder joints, where large voids are clearly visible.

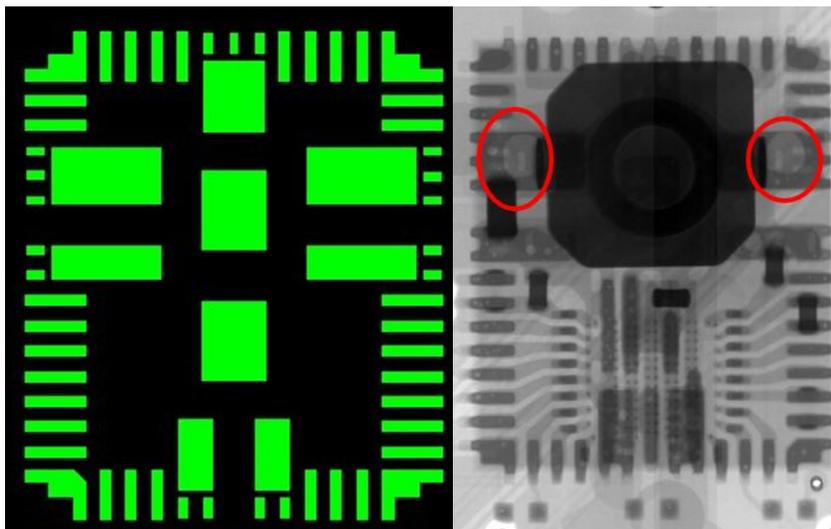


Figure 14: Single-Opening Stencil and X-Ray

Alternatively, the same process was followed using a stencil design which broke up the larger pads into smaller openings, with resulted in much smaller voids (see Figure 15)

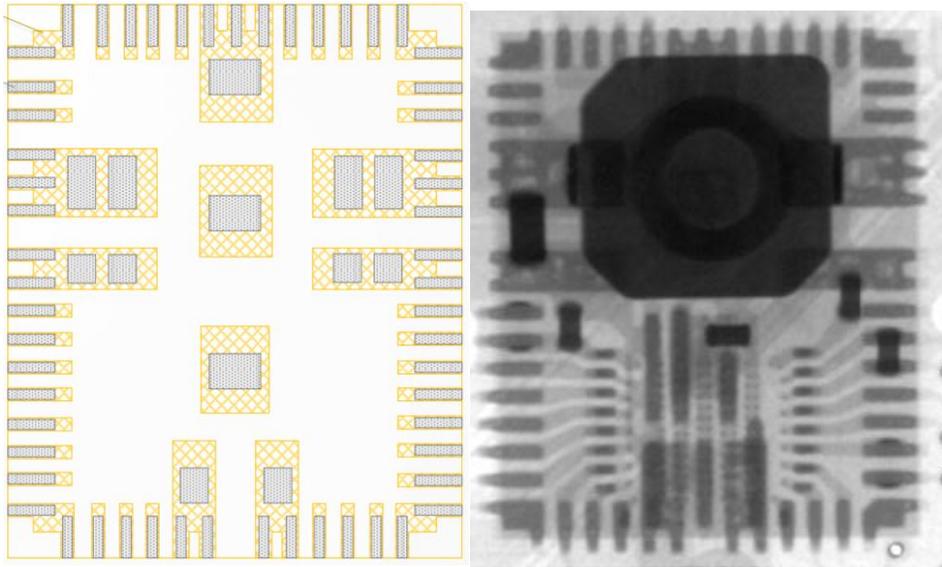


Figure 15: Multiple-Opening Stencil and X-Ray

Second-Side Assembly

For double-sided PCB assembly, it is crucial to assess component weight relative to the pad area. A component weight/total pad area ratio $\leq 0.0465\text{gr/mm}^2$ can be used as for guidance to determine component candidacy for second-side reflow.

Second-side reflow is not recommended for certain MPS devices, including isolated power modules, parts with exposed heatsinks, and thickness exceeding 4mm.

Rework Guidelines

Since LGA package-based parts are not easy to handle, directly repairing failed solder joints is not recommended. Instead, it is recommended to employ a rework procedure to deliver enhanced rework results at the system level.

Pre-Rework

Before the rework, identify the failure(s) and/or defect(s) of the part.

Bake the board with the failed LGA part for 48 hours at 125°C before removing MPS power modules. This helps prevent delamination of the molding compound from substrate of the part. It also helps prevent damage to the adjacent parts on the board.

Component Removal

It is recommended to use a rework station capable of profiling the top and bottom of the power module. To melt the solder joints on the LGA package part, keep the bottom temperature as low as possible but ensure that the solder has reached its liquidation temperature.

Any removed components should not be used.

Site Redress

After the part is removed, remove any residual solder material with an appropriate vacuum nozzle or solder wick braid, and clean the site with appropriate liquid. Isopropyl alcohol (IPA) is recommended for this use.

Solder Paste Printing

The solder paste must be printed on the PCB pads for removed parts. If possible, use a mini-stencil designed specifically for the relevant part to print solder paste with similar parameters. For more details, see the Solder Paste section on page 14. If a mini-stencil is not available, a standard solder-dispensing system can also be used, but the operator must pay attention to the volume of solder paste while dispensing.

Placement and Reflow of New Component

The new component must be handled following the MSL guidelines according to the J-STD-033 standard.

The reflow profile for the reworked component(s) must ensure adequate soaking time, as well as time above the melting point of the solder paste. Profile the temperature with thermocouples.

After the component is soldered, inspect the solder joints using an X-ray or other vision system.

The temperature profile applied at the component must never exceed the maximum temperature based on J-STD-020 standards.

Special Considerations***Dual Component on Package Handling***

When handling dual-component BGA packages, custom SMT nozzles may be required for pick-and-place operations. Proper alignment and placement force settings help prevent component shift during assembly.

Mechanical Load for Heatsink Attachment

Mechanical stress must be minimized by applying uniform pressure perpendicular to the package surface. The maximum permissible force is 350psi.

FREQUENTLY ASKED QUESTIONS (FAQs)

What is the recommended stencil opening and thickness?

Typically, a thickness of 4mils to 5.6mils is recommended depending on the pad size and package type. See the Stencil Design section on page 14 for more details.

What type of solder paste should be used?

No-clean and water-soluble solder pastes are acceptable. Type IV paste is typically recommended.

Can the PCB be cleaned effectively?

Yes, both inline and rotary aqueous cleaning systems have been successfully used. The choice of cleaning method should be compatible with the selected solder paste.

How to inspect solder joints?

X-ray inspection is the most effective method. Systems such as 5DX, YXLON, or Dage X-ray allow for a detailed analysis of solder joint integrity.

Can the module be assembled on both sides of a PCB?

It depends on the module. Some MPS modules are not suitable for second-side reflow due to their weight, size, or thermal constraints. See the Second-Side Assembly section on page 18 for more details.

What causes shorting (e.g. VIN to GND or VOUT to GND)?

Shorts can occur due to solder bridging, misplaced components, or internal defects. X-ray inspection can help identify the issue.

How to prevent shorting inside the module?

Monitor the floor life of the components. If a component has exceeded its MSL floor life (168 hours for MSL 3, 72 hours for MSL 4), bake it at 125°C for 48 hours. Ensure that the reflow temperature does not exceed package specifications.

Can removed devices be reused?

No, once a power module has been removed from the PCB, it should not be reused. A fresh module should always be used for replacement.

What is the maximum mechanical force that can be exerted on a module?

The maximum recommended force depends on the package size. For example, a 15mmx15mm package with a full array of 144 pins (1.27mm pitch) should not exceed 120lbs of applied force.

Can an MPS module be placed directly under another module in a two-sided assembly?

Although MPS Modules can be placed on the bottom in a two-sided assembly, placing it directly beneath another module is not recommended, as it can affect thermal dissipation and mechanical stability. It is best to avoid placing one module directly under another on a PCB.

CONCLUSION

This application note outlines the best practices for assembling MPS power modules with BGA and LGA packages. Proper storage, PCB design, reflow profiling, and rework procedures are critical to ensuring reliable assembly and long-term performance. By following these guidelines, manufacturers can enhance product quality and minimize defects in high-density electronic applications.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/23/2025	Initial Release	-
1.01	3/4/2026	Updated “usally” to “usually” in LGA PCB Pad Layout section.	8
		Updated the second Table 11 to Table 12.	14
		Added a period to the final bullet point in the Void Reduction Strategies section.	17
		Fixed capitalization error in Site Redress section.	18

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