Zero Delay PWM Control

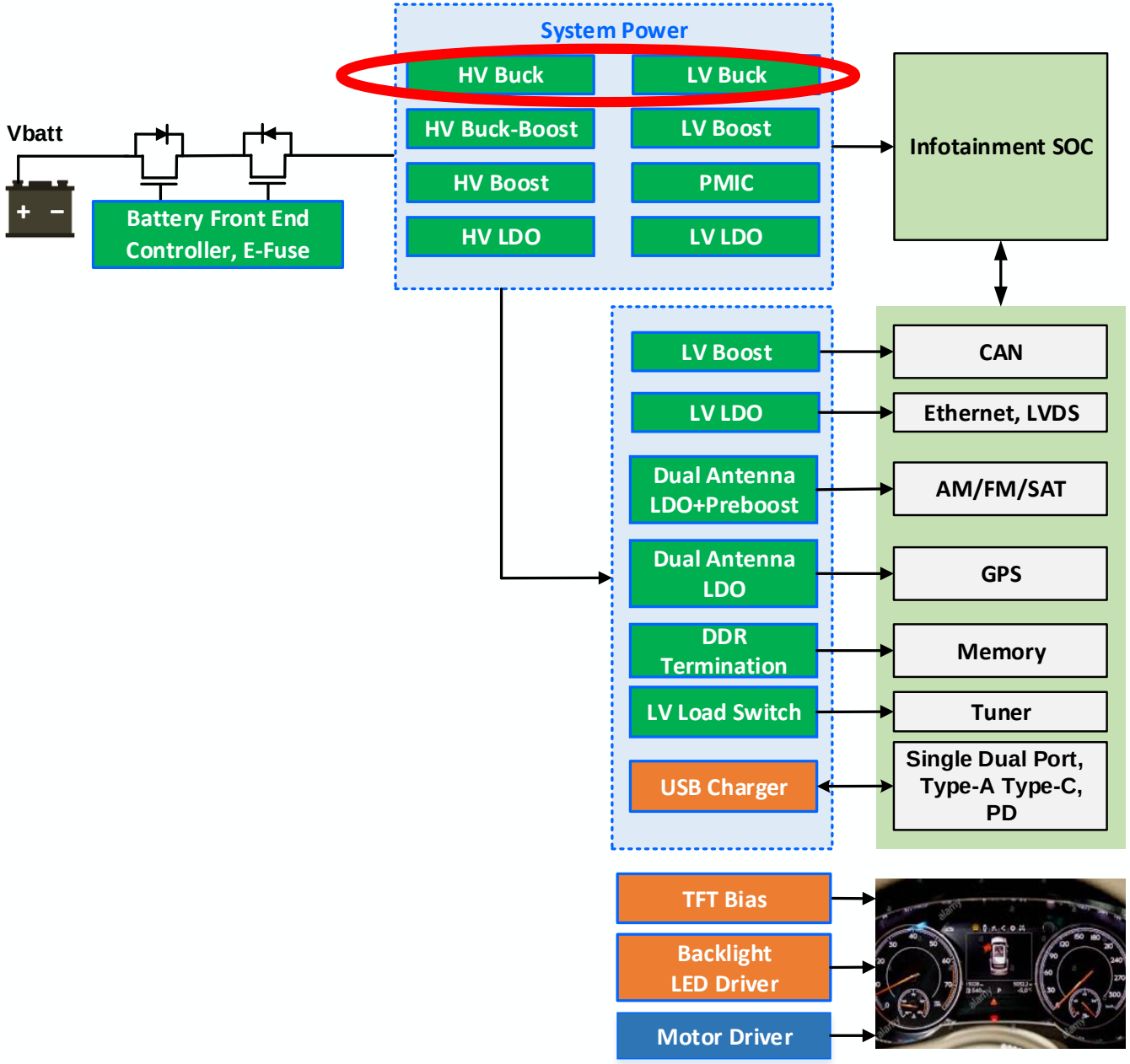
Introduction and Comparison with other control methods

May 2024

Agenda

- Background
- Voltage Mode
- Peak Current Mode
- Constant On-Time
- Zero Delay PWM
  - Block Diagram/Operation
  - Hardware Results
  - Pros and Cons

Background


System Power
HV Buck
LV Buck
HV Buck-Boost
LV Boost
HV Boost
PMIC
HV LDO
LV LDO
Vbatt
Battery Front End Controller, E-Fuse
Infotainment SOC
LV Boost
LV LDO
Dual Antenna LDO+Preboost
Dual Antenna LDO
DDR Termination
LV Load Switch
USB Charger
CAN
Ethernet, LVDS
AM/FM/SAT
GPS
Memory
Tuner
Single Dual Port, Type-A Type-C, PD
TFT Bias
Backlight LED Driver
Motor Driver

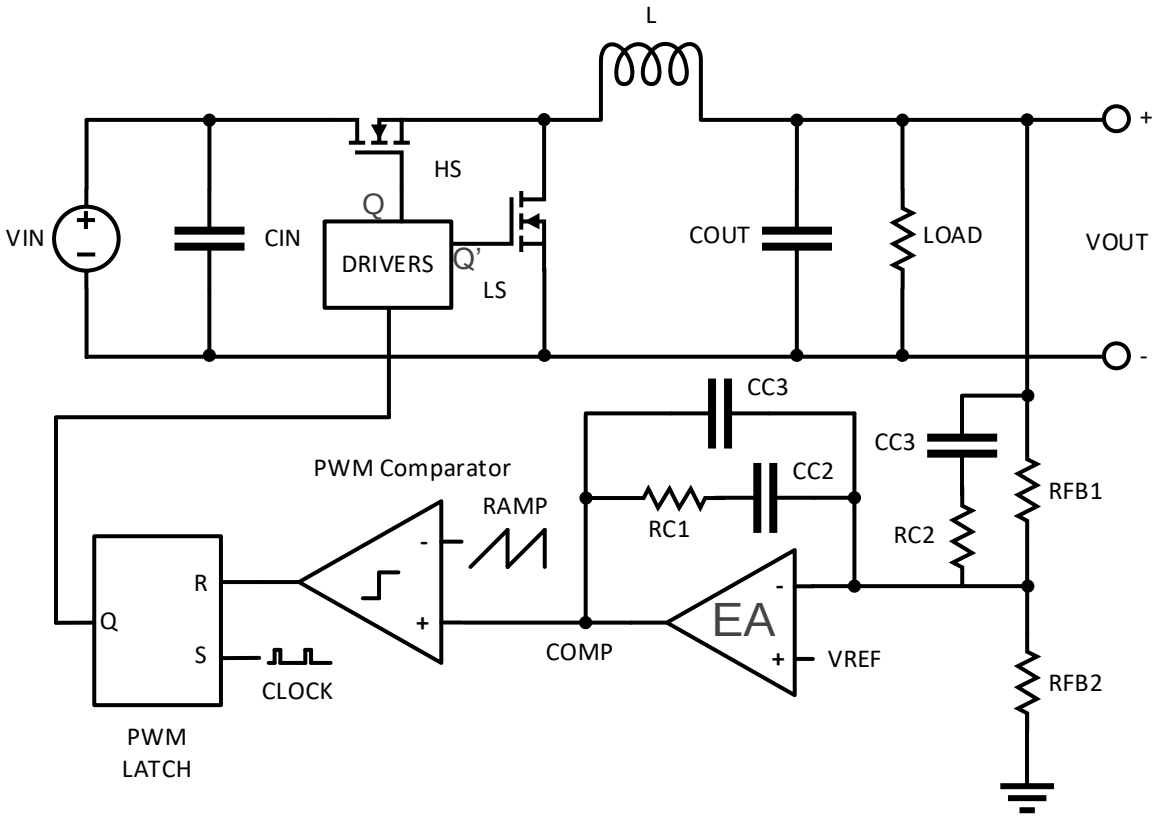
Background

- ~ 5 years ago, automotive applications were low power (<20W) and could be covered with a 3 or 4A buck.
  - >6A were infrequently require.
  - Transient requirements were not stringent.
- As computing requirements increased, POLs/LV bucks using COT were very common
- COT considered for off-battery/HV bucks, but customers were hesitant due to EMI
  - Peak Current Mode control was ubiquitous, but lacks load transient performance

- Additionally, MPS also had difficulty covering 18V -> 3.3V @ 2.2MHz with spread spectrum
  - Large minimum on time gated the ability for a large conversion ratio at >2MHz fsw

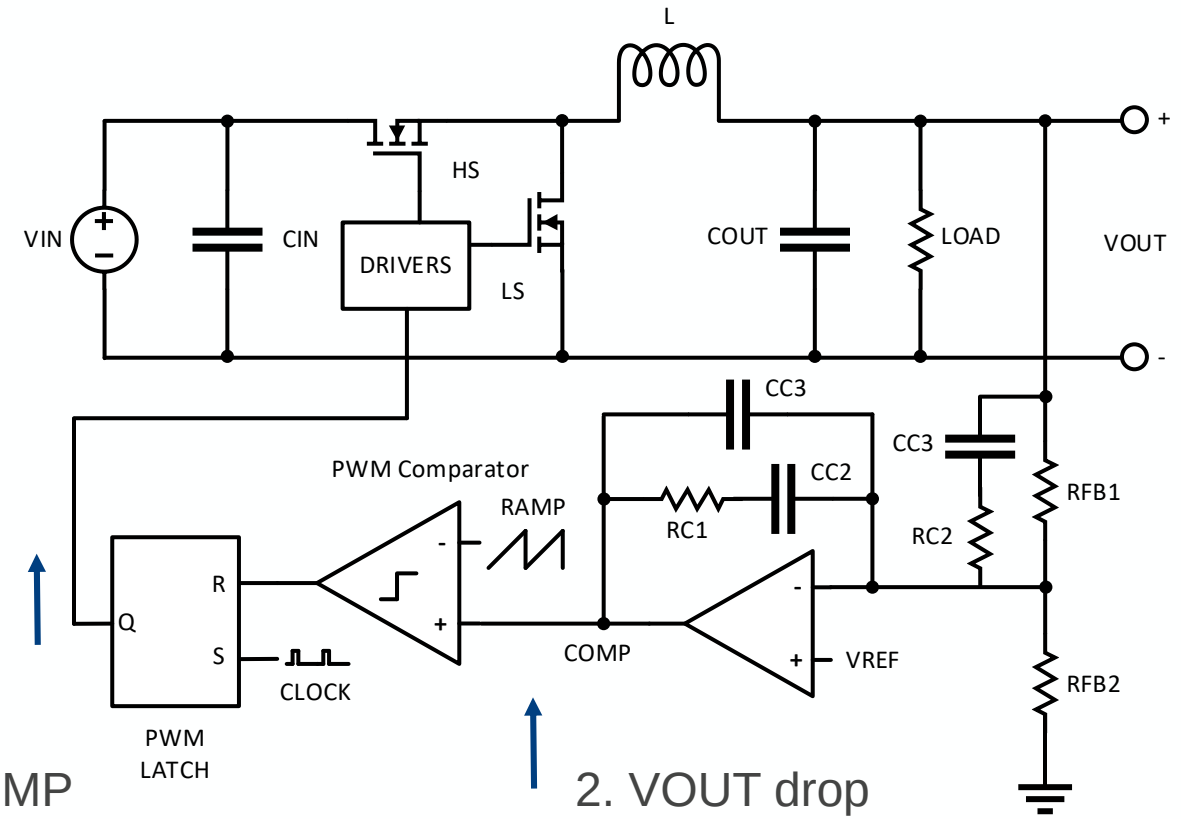
GOAL: Create a control topology that combined the dynamic benefits of COT with fixed frequency operation while allowing for a narrow on time.

Voltage Mode Control – Operation



- Clock turns on HS
- Ramp was generated by clock
- Output Voltage is compared to VREF to generate COMP signal.
- COMP signal is compared to ramp to generate the LS on signal

Voltage Mode Control – Load Transient Operation



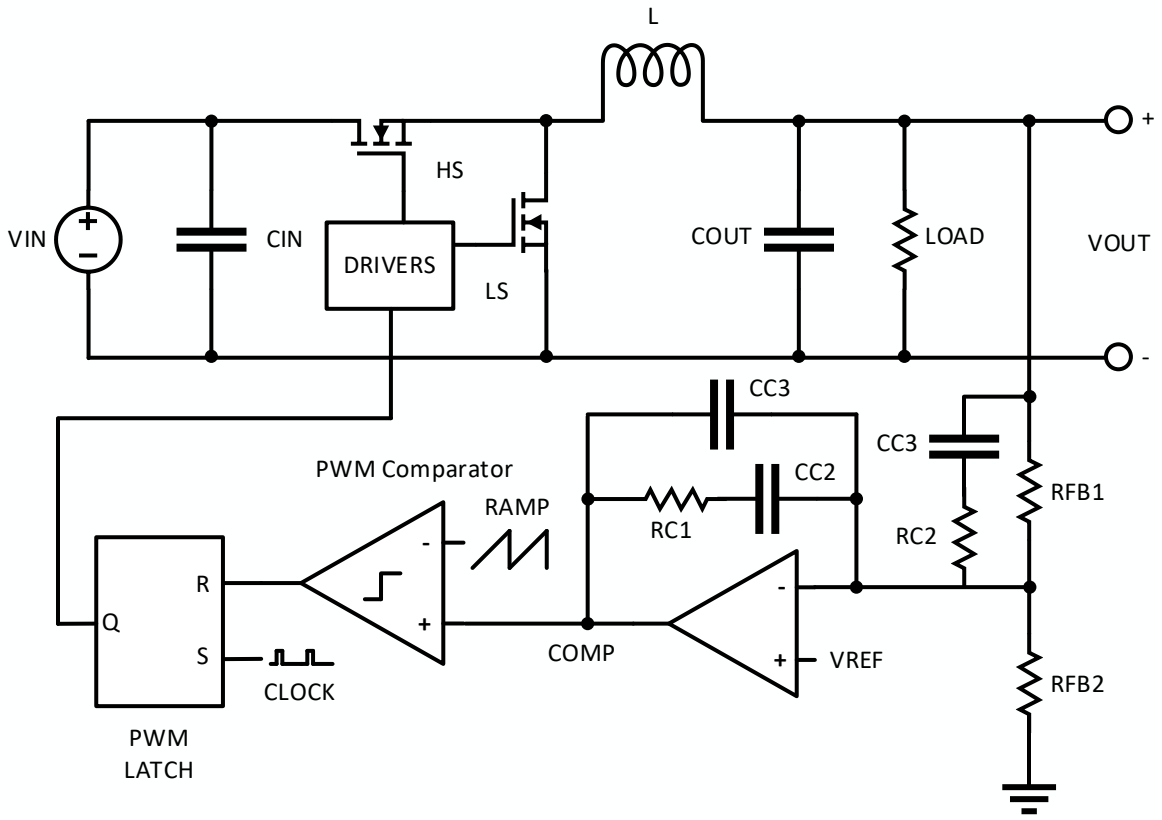
Legend
Fast Change:
Slow change:

1. Sudden load current increase causes VOUT to drop

2. VOUT drop causes COMP to increase

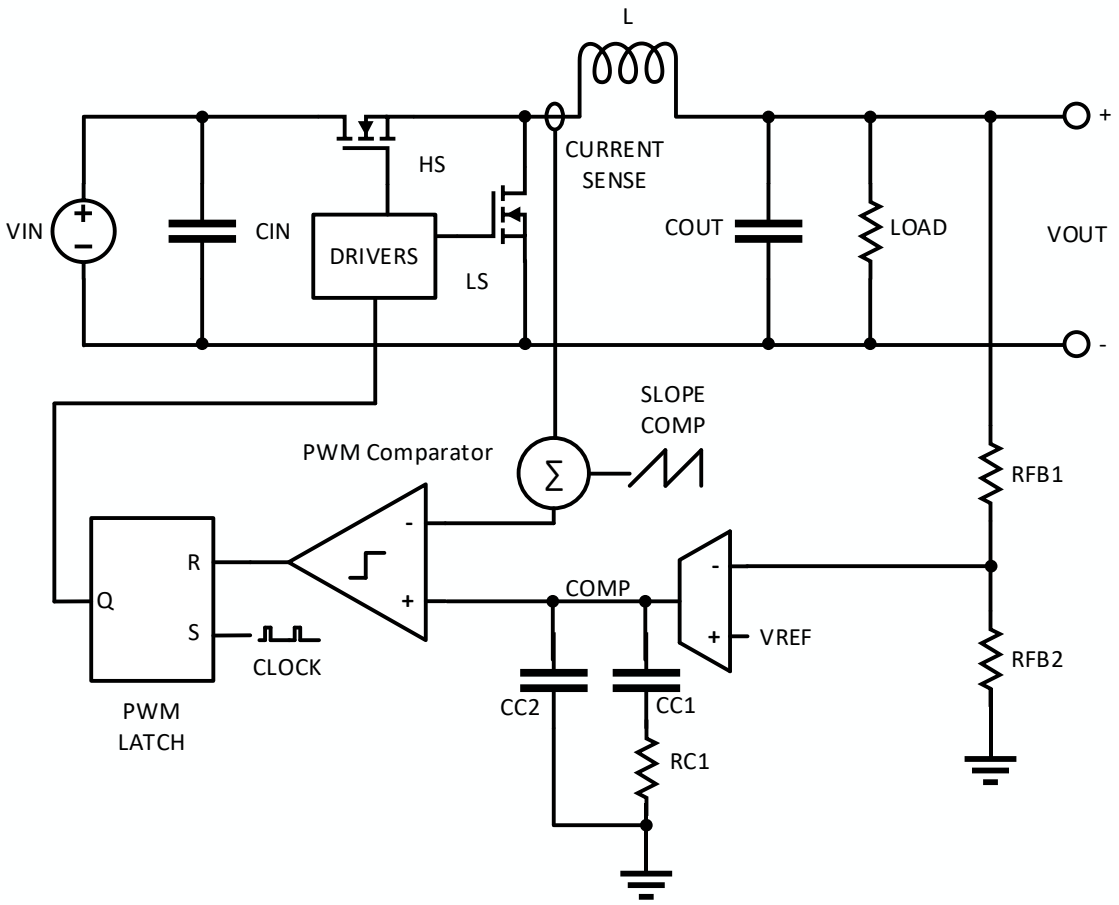
3. COMP increases causes duty cycle to increase

Voltage Mode Control – Pros and Cons



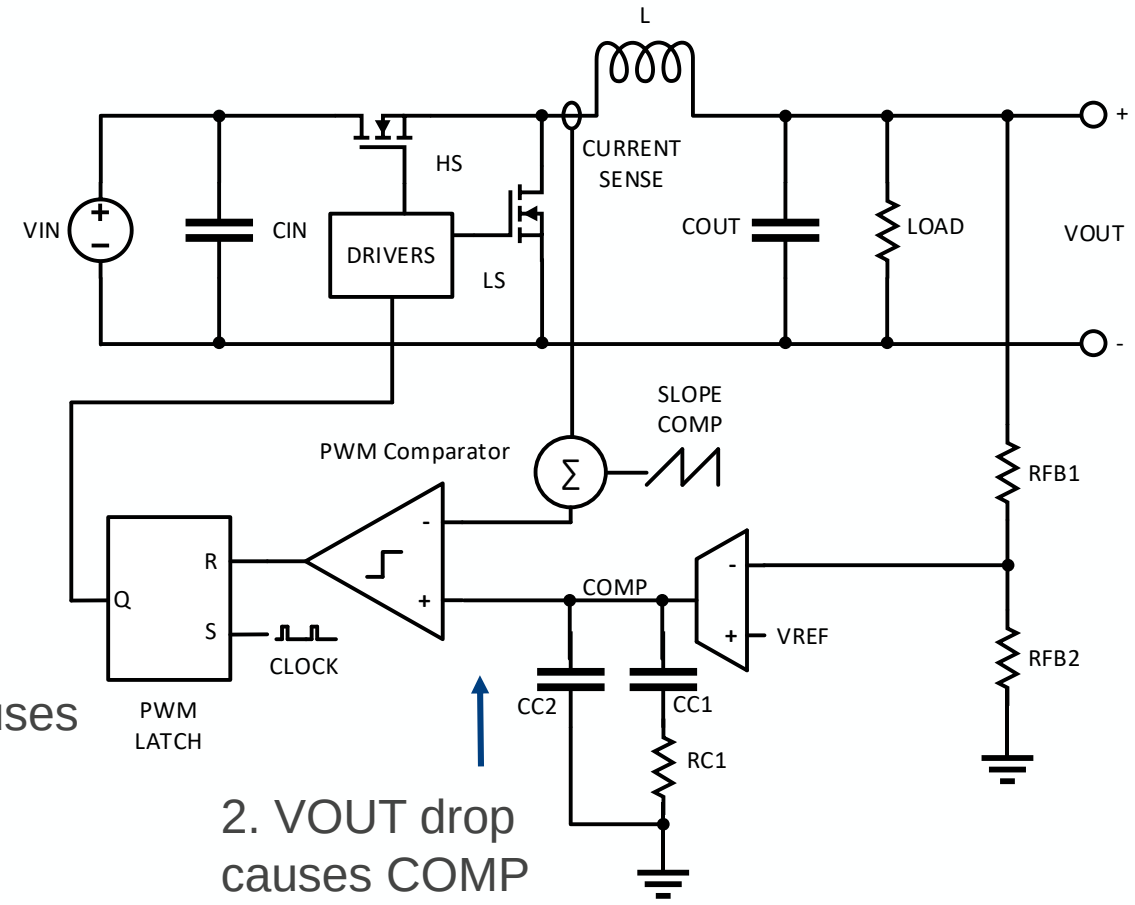
+ Simplest Control Method
+ Good noise immunity no current noise
- Due to undamped LC output filter, requires high ESR capacitors or type III compensation
- Load transient performance is okay
- Line transient is poor, unless line feedforward is used on the ramp

Peak Current Mode Control - Operation



- Output voltage is compared to VREF to generate COMP signal.
- COMP signal is compared to sensed current.
- Most implementations add a slope compensation ramp to the current signal

Peak Current Mode Control – Load Transient Operation



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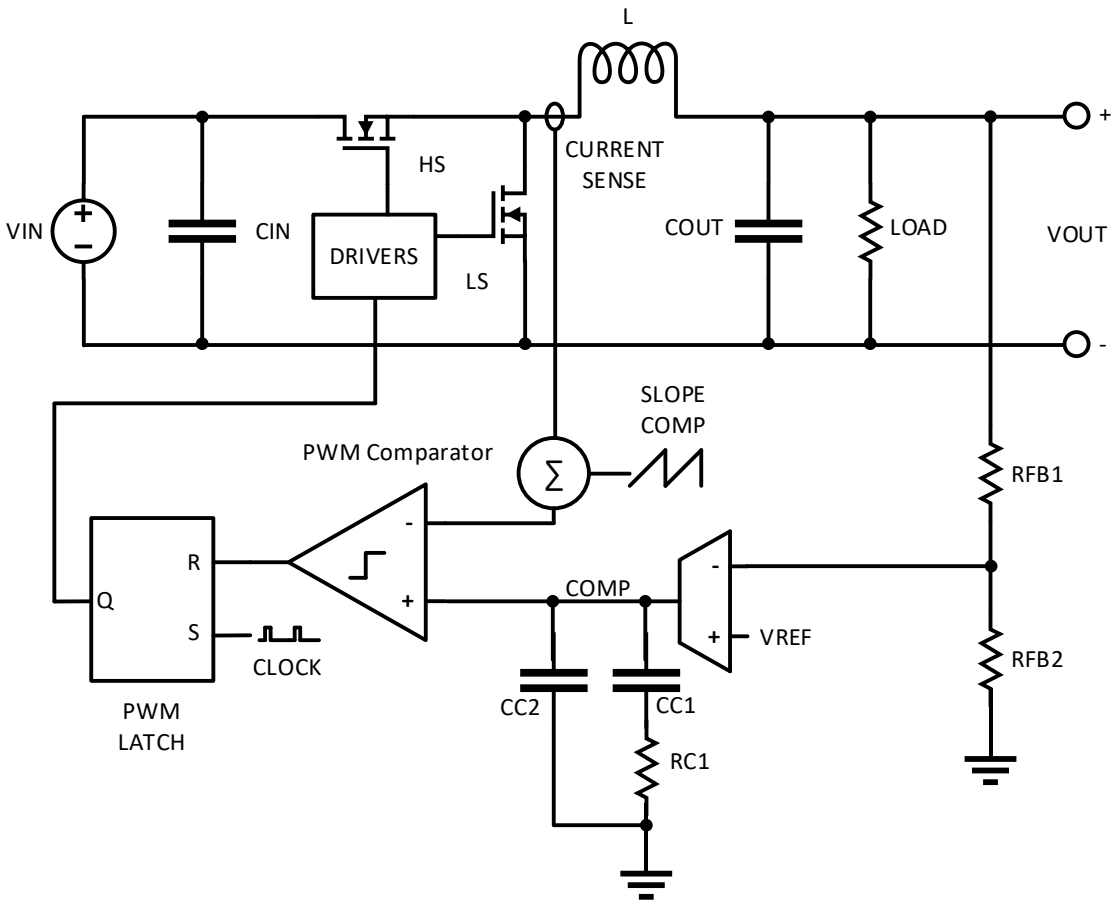
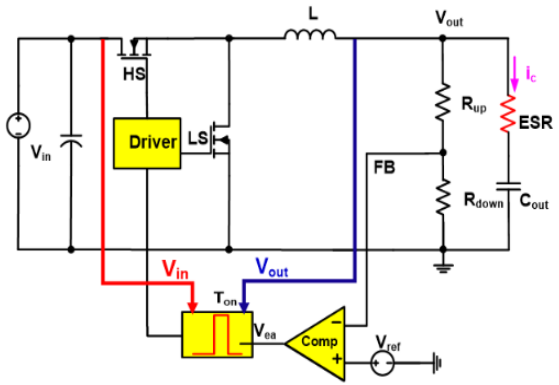
Peak Current Mode Control – Pros and Cons

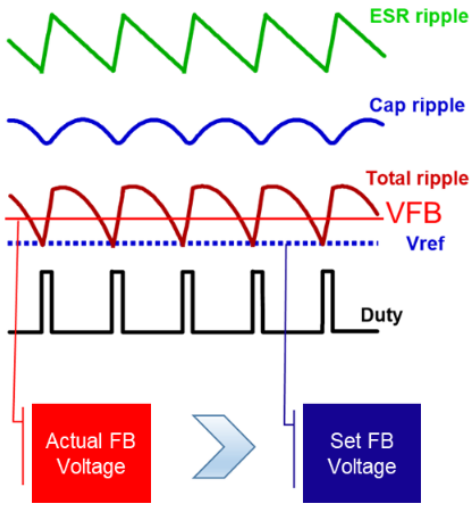


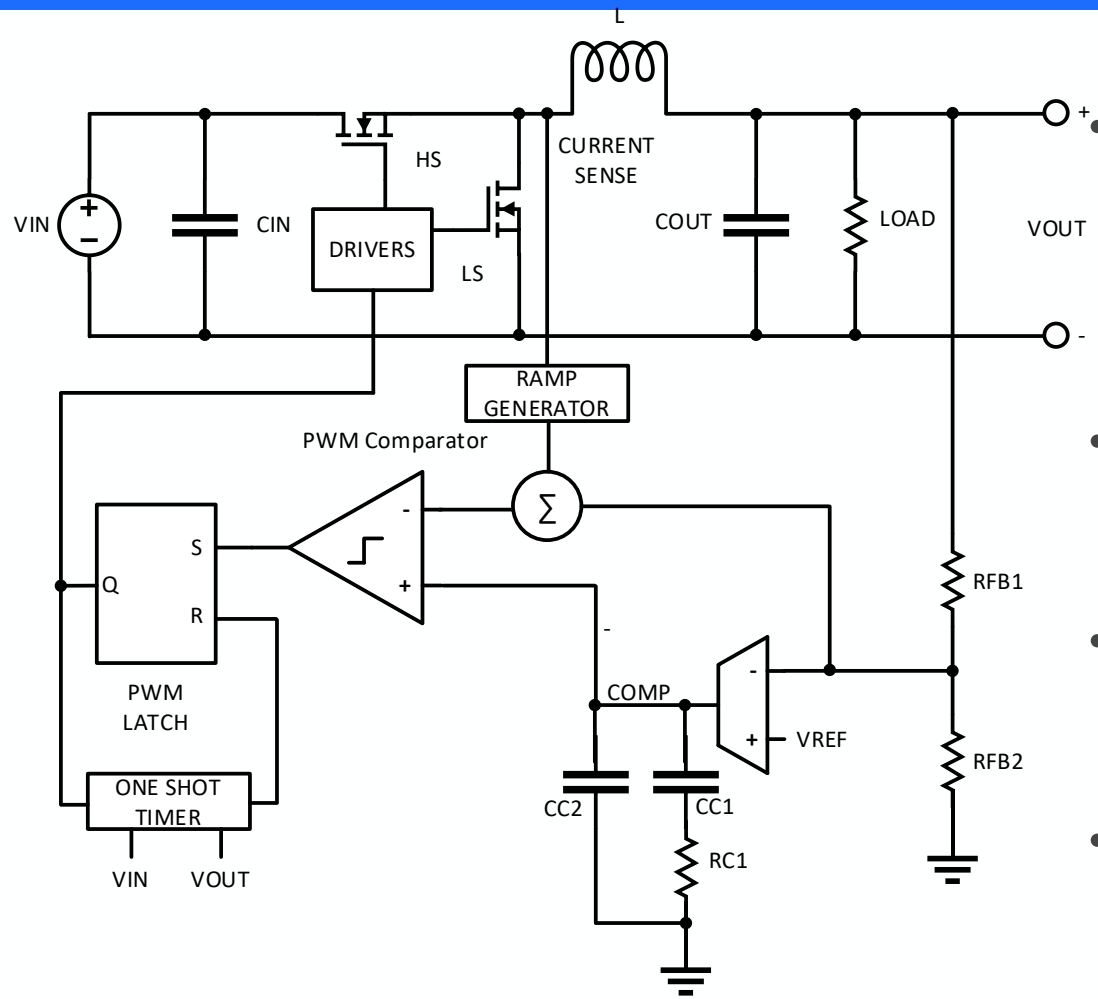
+ Improved compensation with current feedback that acts a lossless resistor damping the output LC filter
+ Good line transient performance
- Okay load transient performance
- Complex compared to voltage mode
- Large minimum on time limits minimum conversion ratio due to “blanking time” for peak current sense

Constant On-time Control - Operation
(w/ Offset Cancellation & Synthetic Ramp)



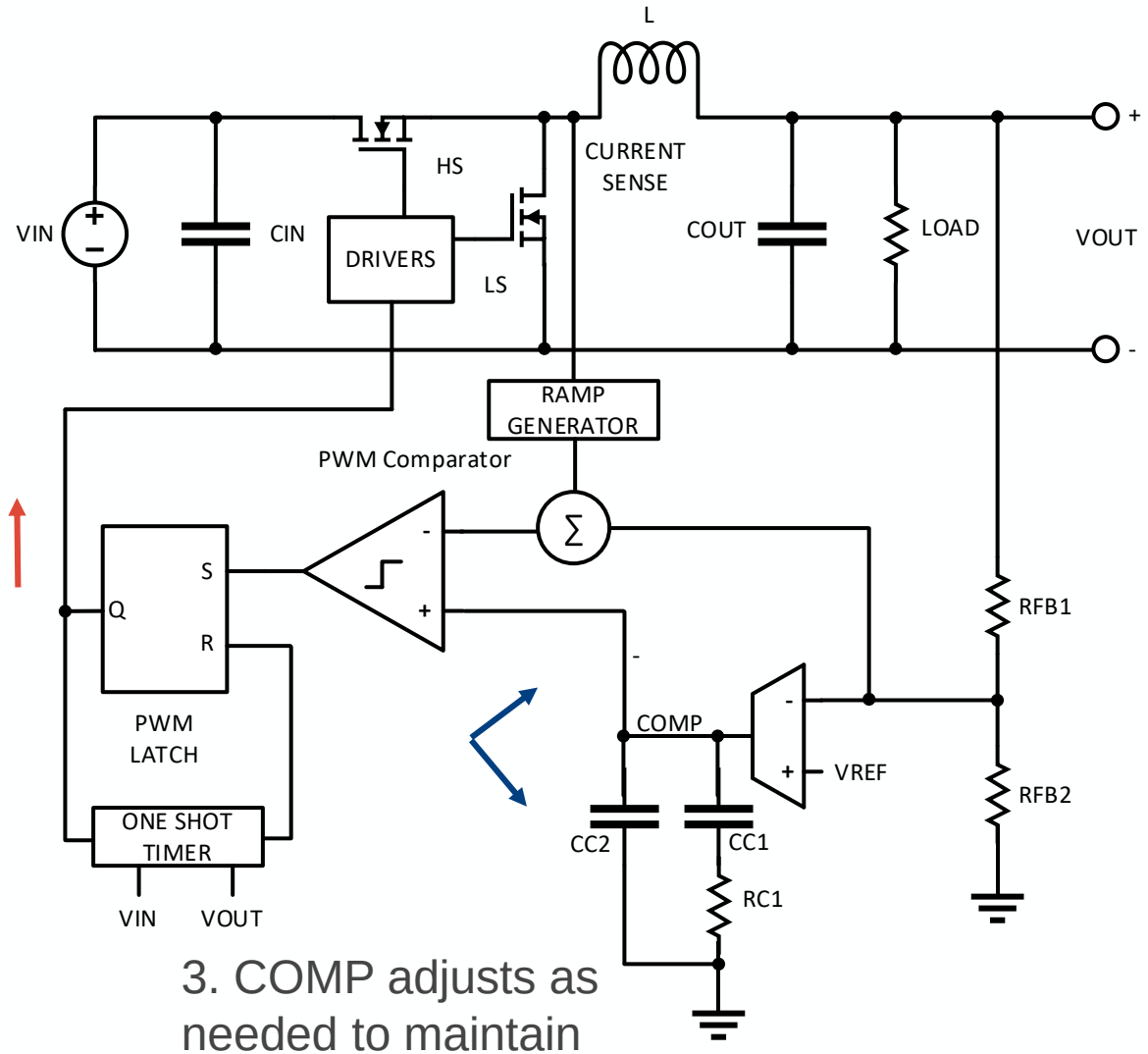
Simple COT





- Output voltage (with synthetic ramp) is fed directly into PWM Comparator and acts as a fast loop response to VOUT changes
- Output voltage compared to VREF to create COMP signal for improved DC regulation
- Synthetic ramp is added to allow operation with low ESR capacitors
- On-time can be generated at any time (after a minimum off-time)

Constant On-time Control – Load Transient Operation
(w/ Offset Cancellation & Synthetic Ramp)



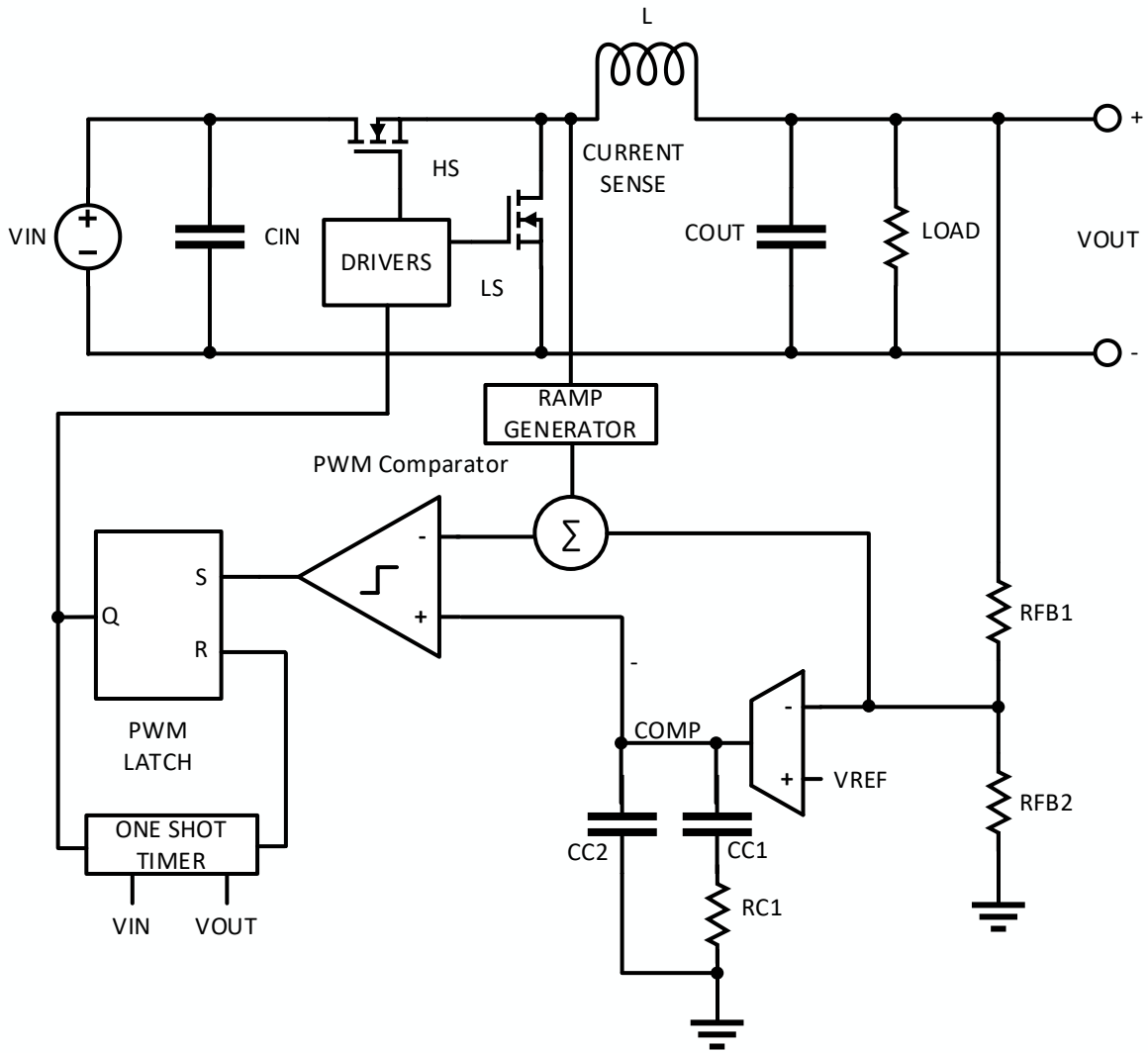
1. Sudden load current increase causes VOUT to drop

2. VOUT dropping directly and immediately causes additional on-time pulses

3. COMP adjusts as needed to maintain DC regulation

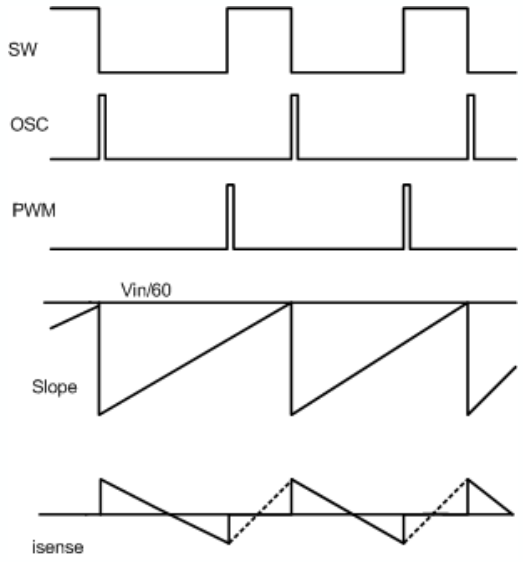
Legend
Fast Change:
Slow change:

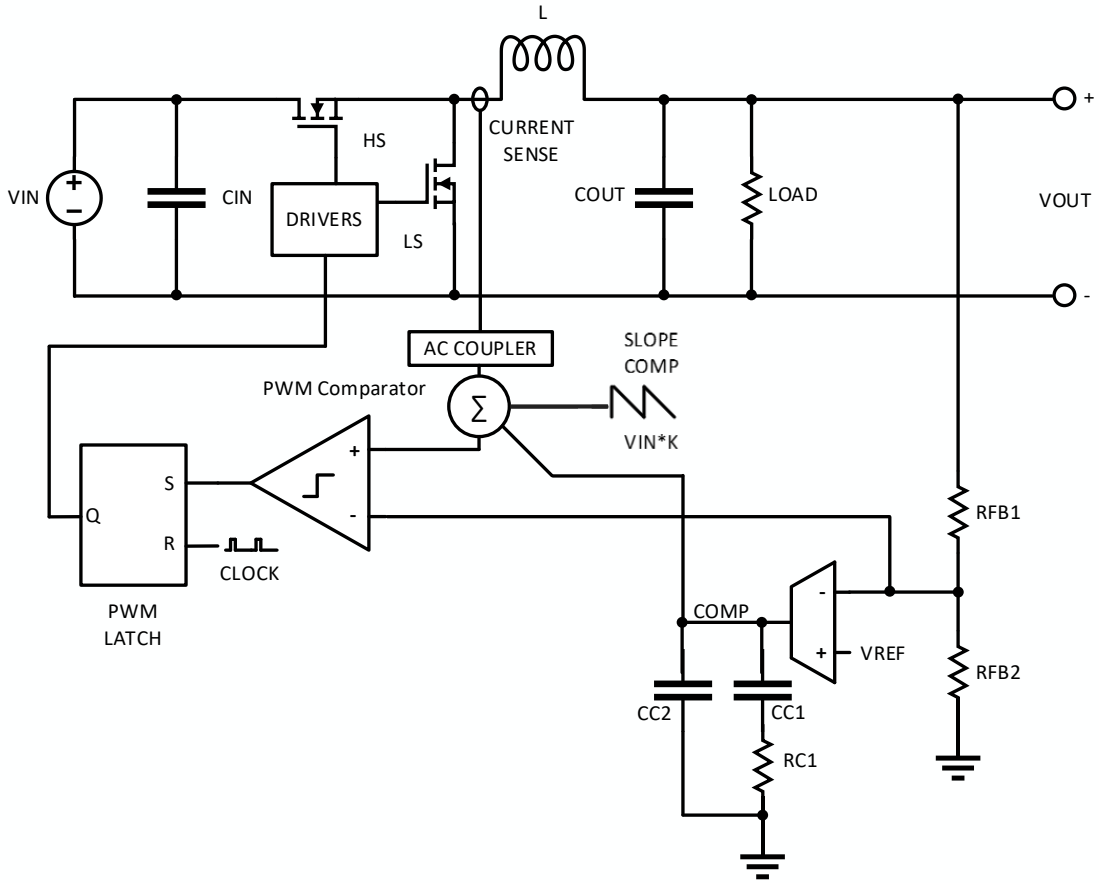
Constant On-time Control – Pros and Cons
(w/ Offset Cancellation & Synthetic Ramp)



+ Great line & load transient response
+ Low cost implementation
- Switching frequency may change, especially during transients, which is unsuitable for EMI in off-battery application
- Synthetic ramp required for low ESR capacitors

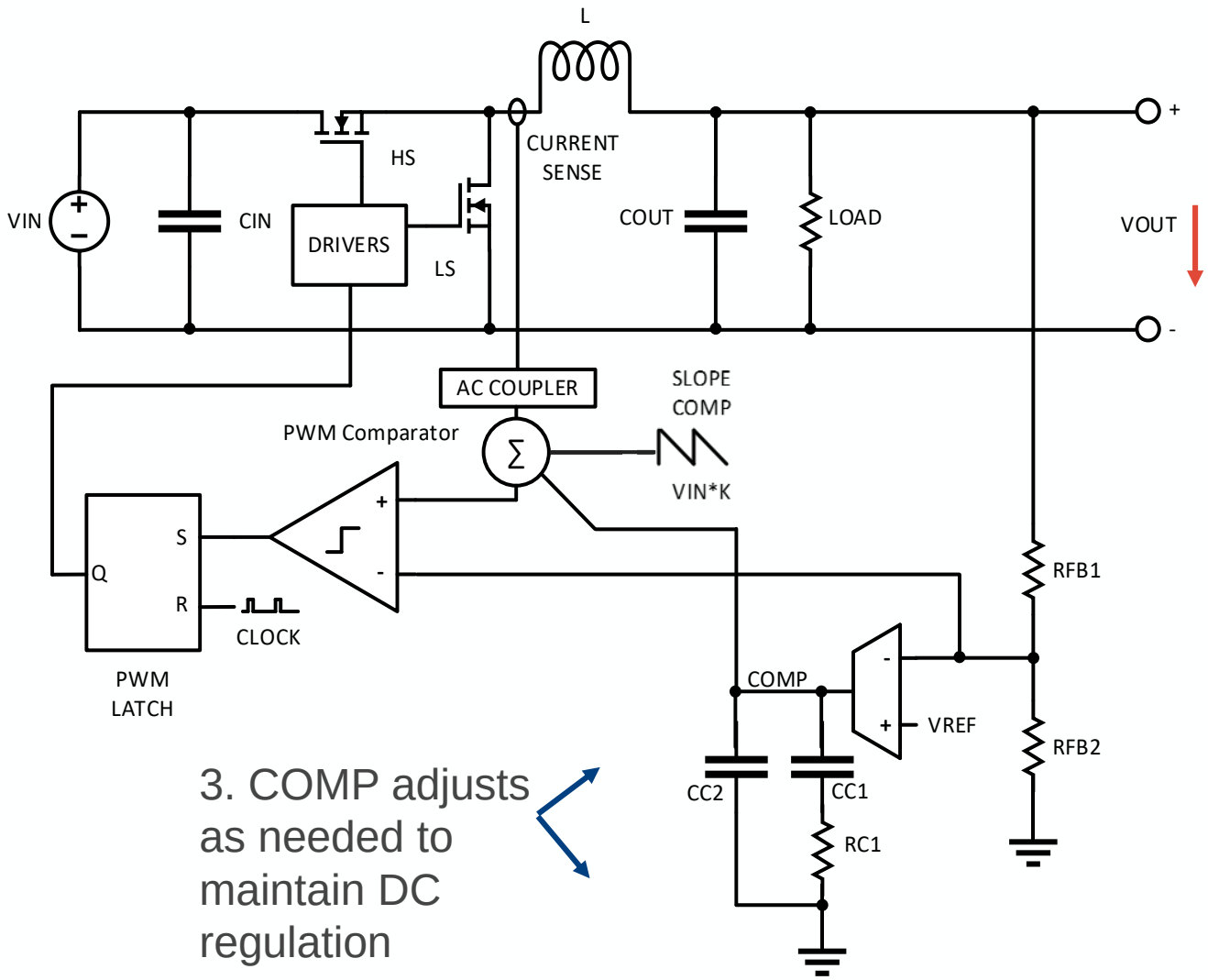
Zero Delay PWM (ZDP) – Operation





- Like COT, output voltage is fed directly into PWM Comparator for a fast loop and compared to VREF to create COMP signal for improved DC regulation
- Like Peak Current Mode, a sensed current signal, with slope compensation, is used. And PWM latch is reset with a fixed frequency clock
- The slope compensation is proportional to VIN and includes offset cancelation to improve the line transient response.
- Valley current mode does not require “blanking time”, allowing for a small minimum on time

Zero Delay PWM (ZDP) – Load Transient Operation



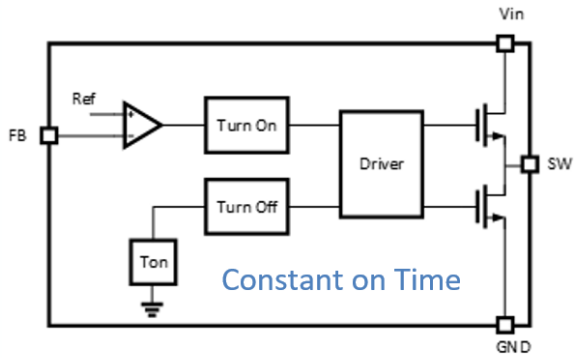
1. Sudden load current increase causes VOUT to drop

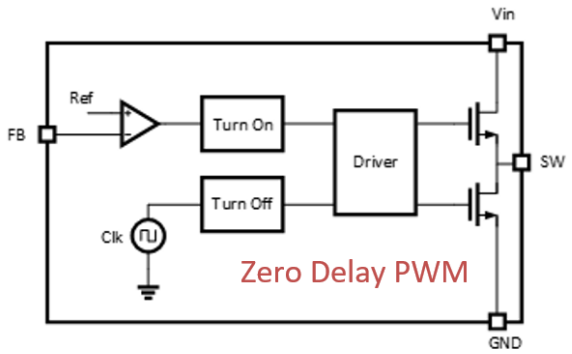
2. VOUT dropping directly and immediately causes duty cycle to increase

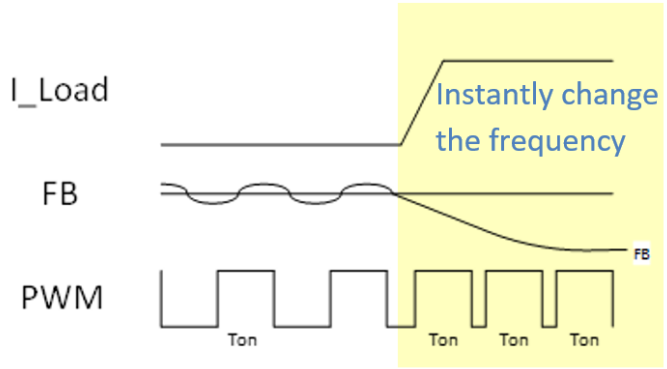
3. COMP adjusts as needed to maintain DC regulation

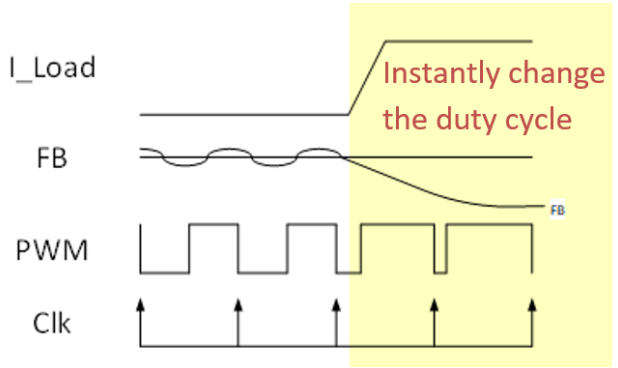
Legend
Fast Change:
Slow change:

ZDP vs COT Comparison





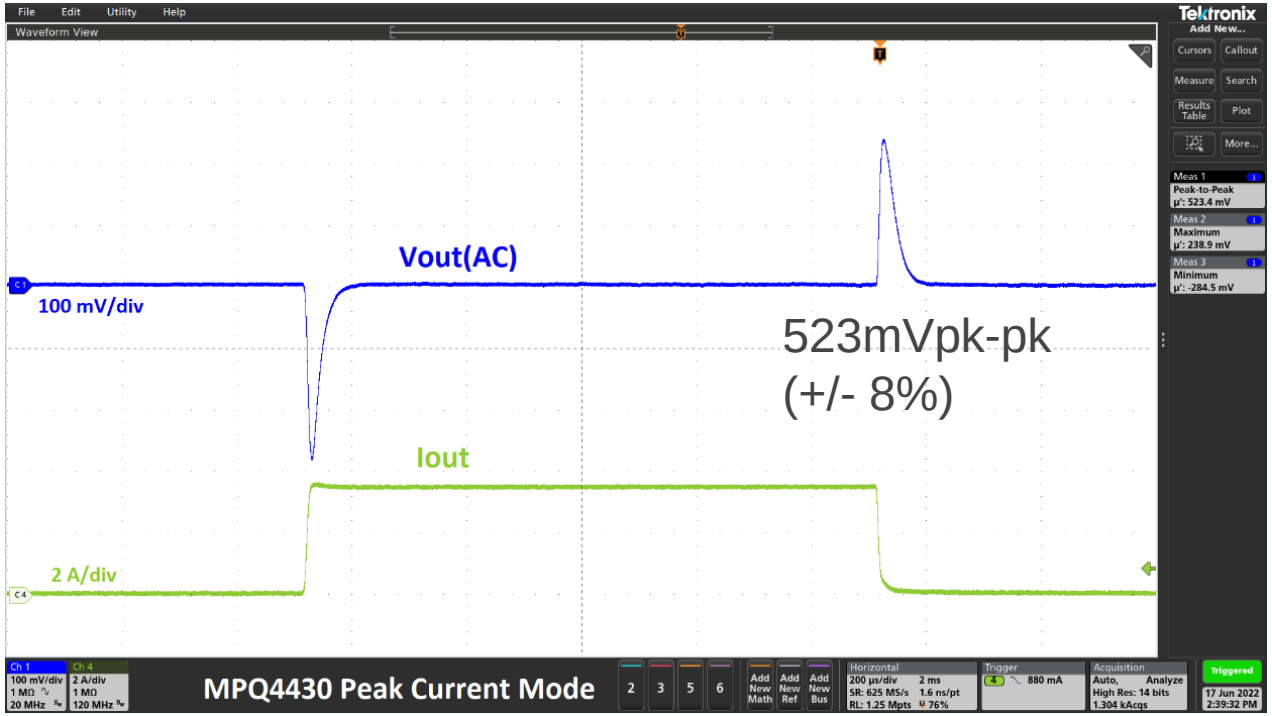




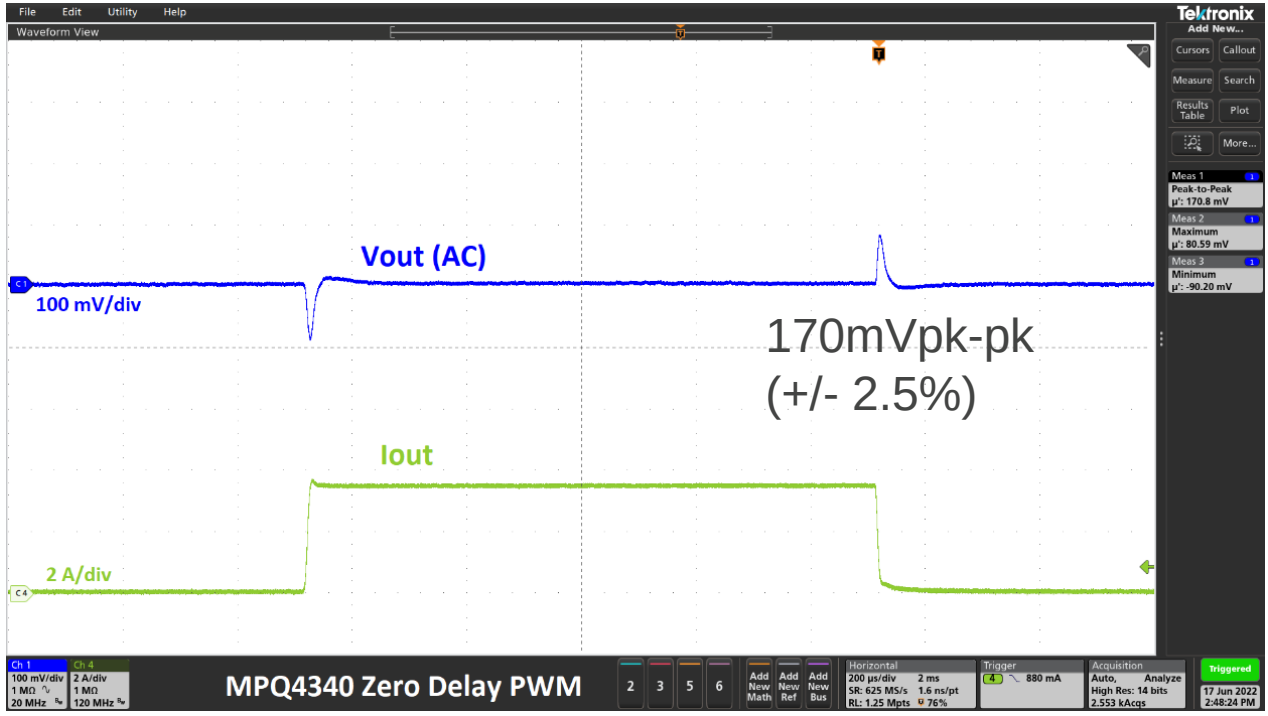
- In COT, SR latch is reset by a one shot timer
- In Zero Delay PWM, SR latch is reset by a clock
- Both topologies bring FB directly to the PWM comparator.

Zero Delay PWM – Load Transient Hardware

Peak Current Mode

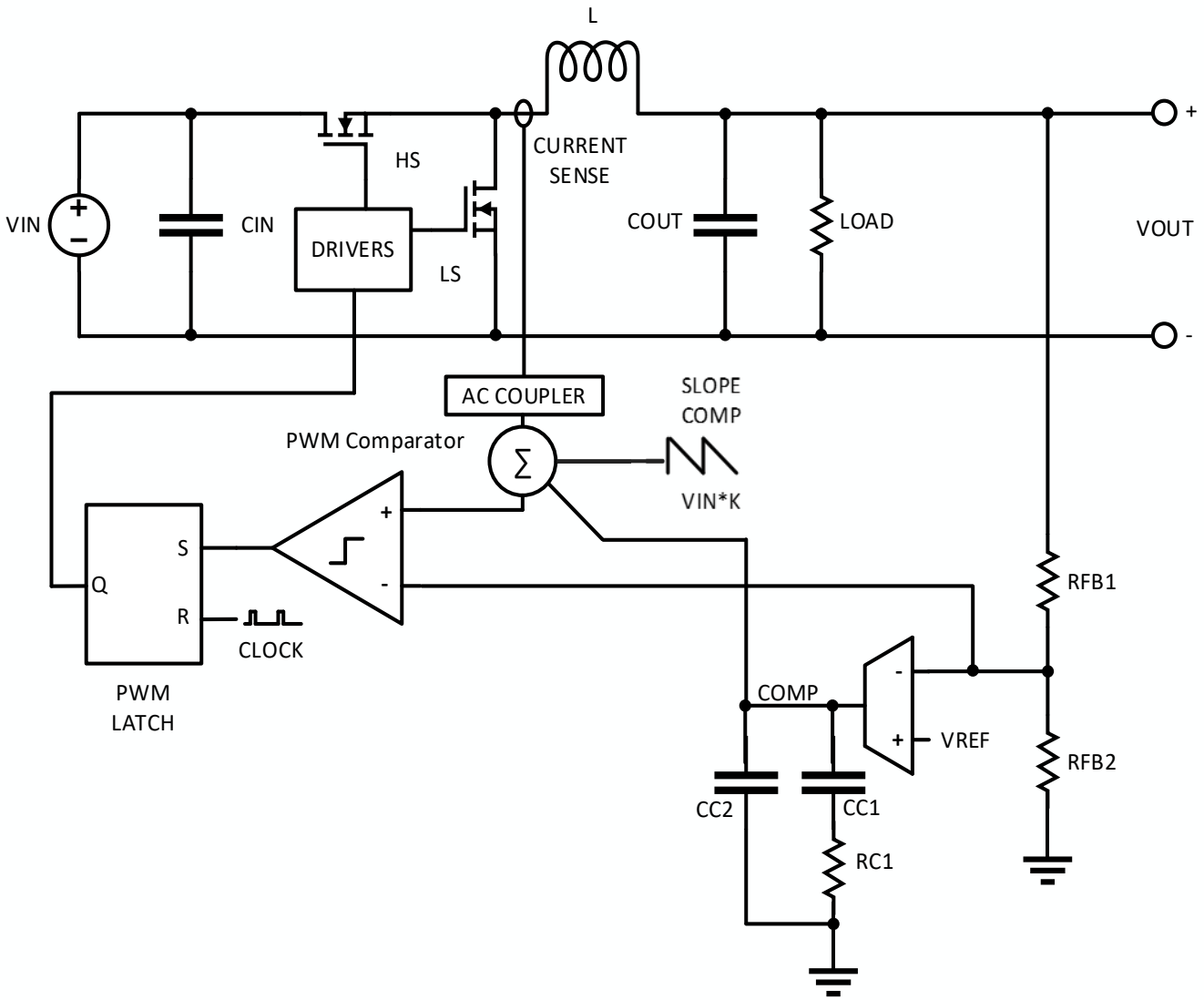


Zero Delay PWM



- 3x faster transient compared to peak current mode with the same components and setup
  - 12V input, 3.3V output, 0A to 3.5A load step
  - 1uH Lout, 2x22uF Cout

Zero Delay PWM – Pros and Cons



+ Type I or Type II compensation is sufficient for stability
+ True fixed frequency operation
+ Can be synchronized without a PLL
+ Line/Load transient performance on par with COT
  - Reduced output capacitance requirement
+ Valley current allows for a very narrow minimum on time
  - Worst case 35ns compared to 60-100ns for peak current mode
- Complexity -> High cost implementation

Thank You