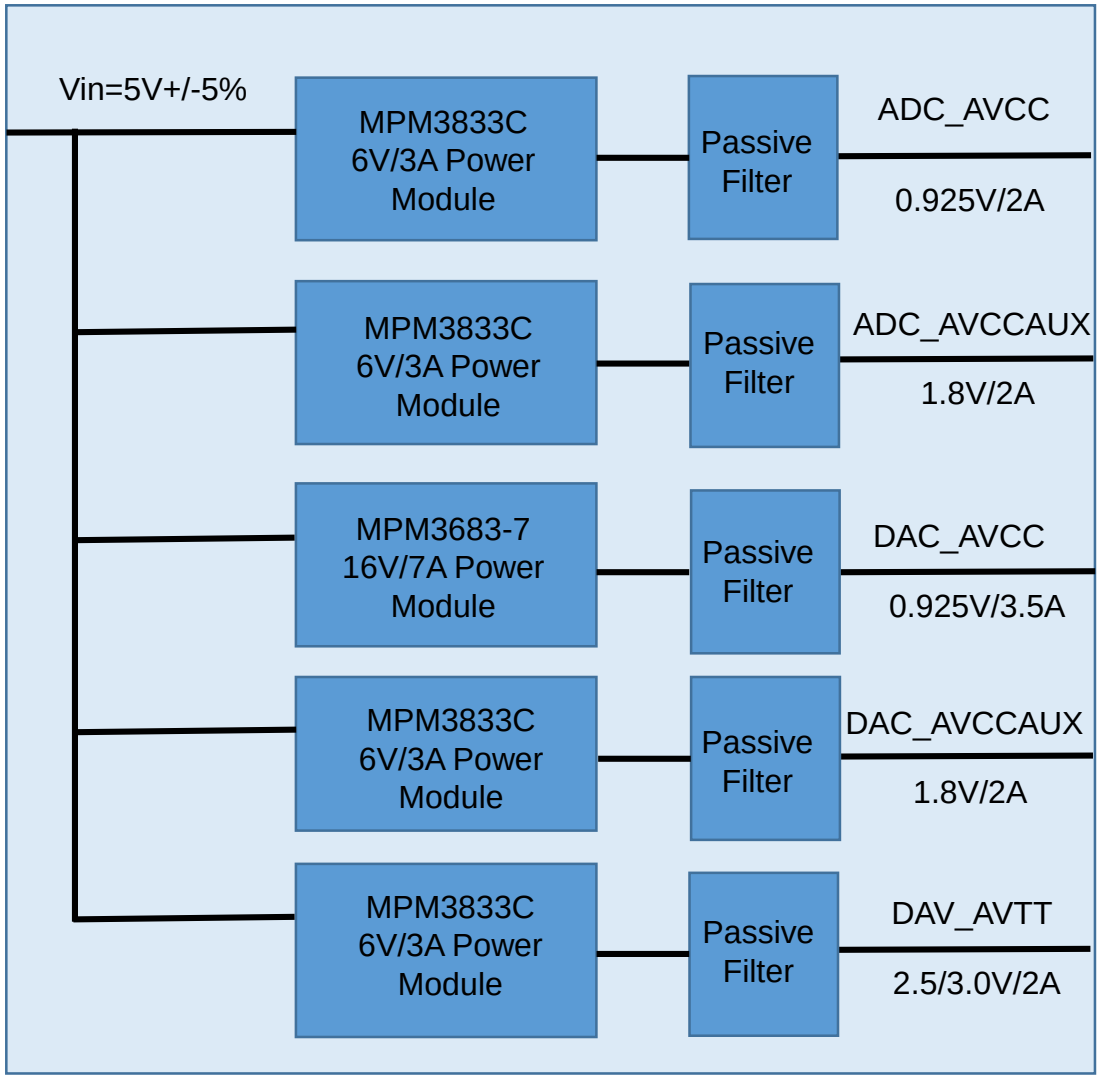
MPS Power Module Solution for Xilinx ZYNQ UltraScale+ RFSoC FPGA Analog Rails

Simple, Easy Solutions™

rev 20170706

Power Tree of MPS Solution – Passive Filter Version



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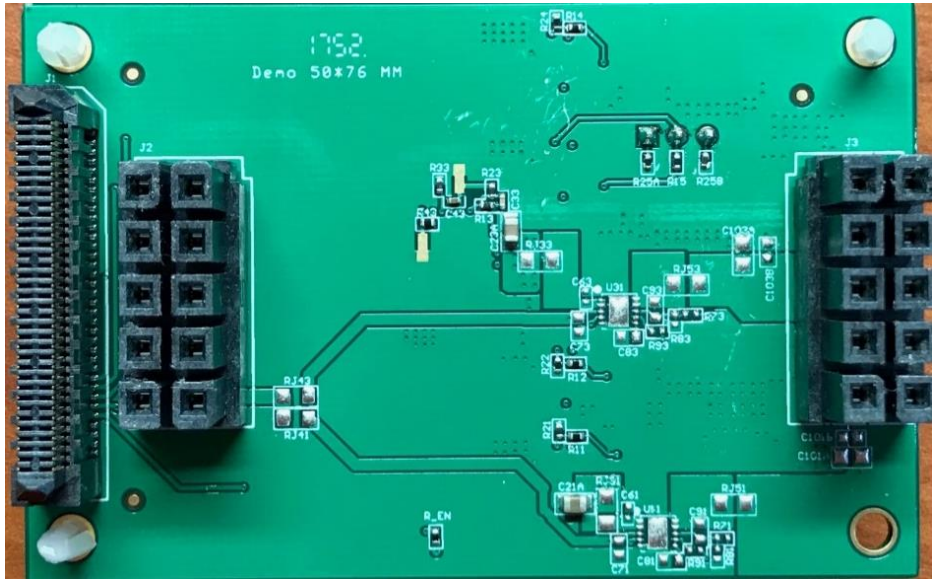
Reference Design Board Pictures

EVREF0102-A Passive filter version



FPGA Series	FPGA P/N	EVB P/N
Zynq Ultrascale+ RFSoC Analog Rails	ZU21DR to ZU29DR	EVREF0102A/B

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Voltage Regulation of EVREF0102-A

Rail Name	MPS P/N	Designator	V_O @ no load (V)	V_O @ full load (V)
ADC_AVCC	MPM3833C	U1	0.927	0.918
ADC_AVCCAUX	MPM3833C	U2	1.795	1.789
DAC_AVCC	MPM3683-7	U3	0.927	0.917
DAC_AVCCAUX	MPM3833C	U4	1.799	1.795
DAC_AVTT	MPM3833C	U5	2.527	2.520

Note: 1% accuracy feedback resistors are used

Output Voltage Ripple of EVREF0102-A

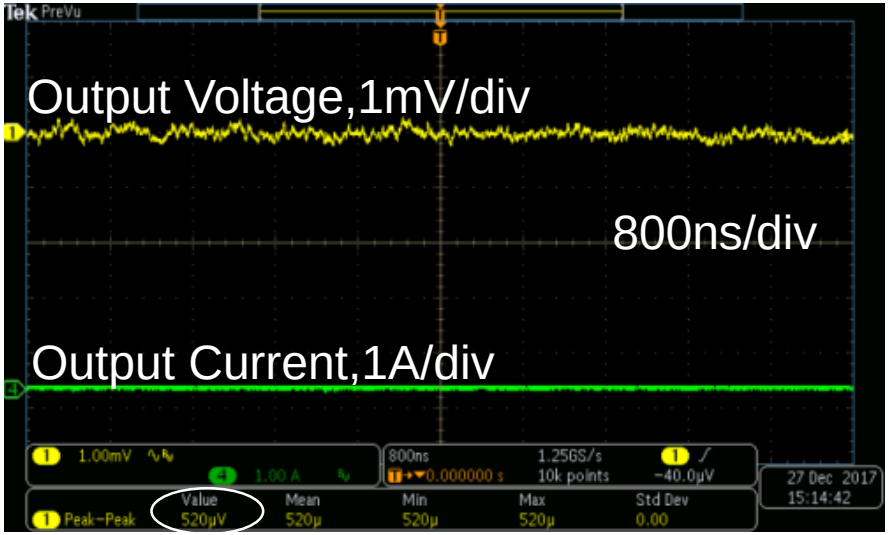
Rail Name	MPS P/N	Designator	$V_{O,P-P}$ @ no load (mV)	$V_{O,P-P}$ @ full load (mV)
ADC_AVCC	MPM3833C	U1	0.52	0.56
ADC_AVCCAUX	MPM3833C	U2	1.04	0.88
DAC_AVCC	MPM3683-7	U3	0.88	0.84
DAC_AVCCAUX	MPM3833C	U4	0.84	0.72
DAC_AVTT	MPM3833C	U5	2.08	1.68

Note: 20 MHz bandwidth is selected for ripple measurements.

ADC_AVCC Voltage Ripple

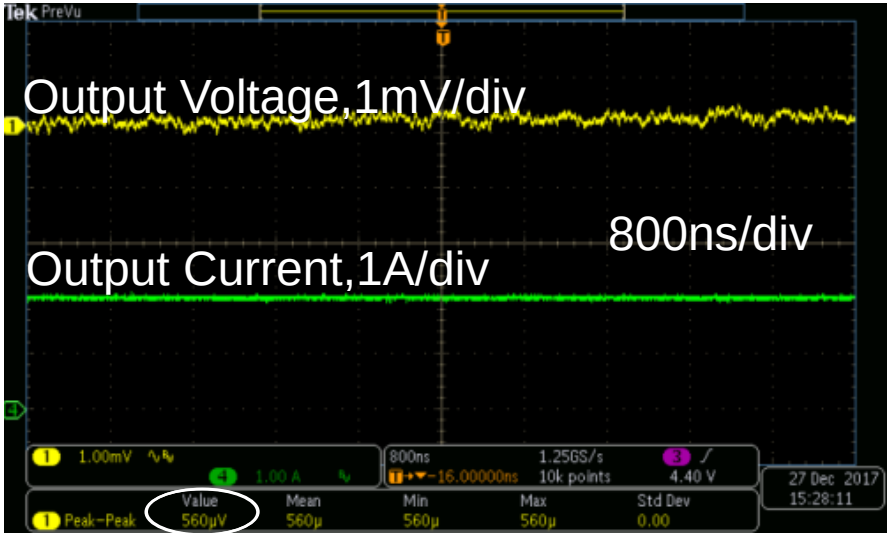
Vo=0.925V,I_o=0A

$V_{o,P-P}$=0.52mV



Vo=0.925V,I_o=2A

$V_{o,P-P}$=0.56mV



MPM3833C

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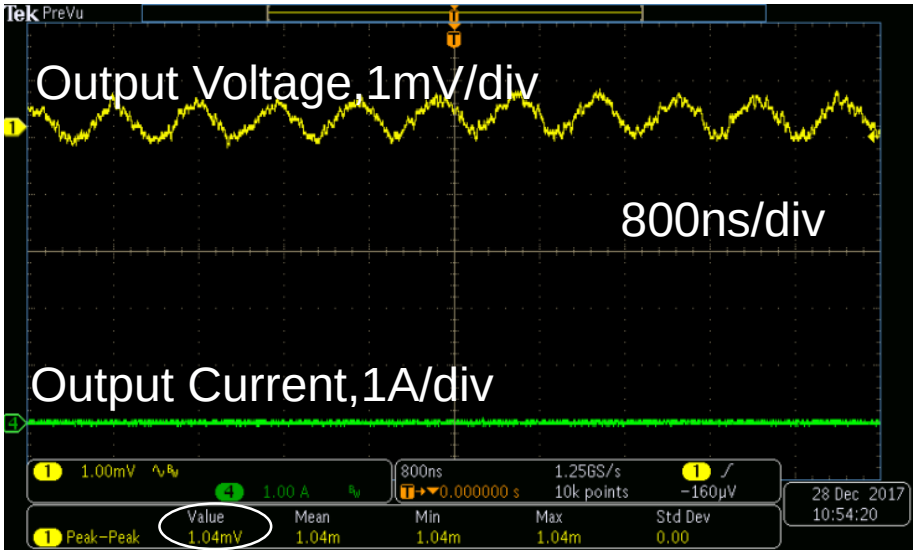
ADC_AVCCAUX Voltage Ripple

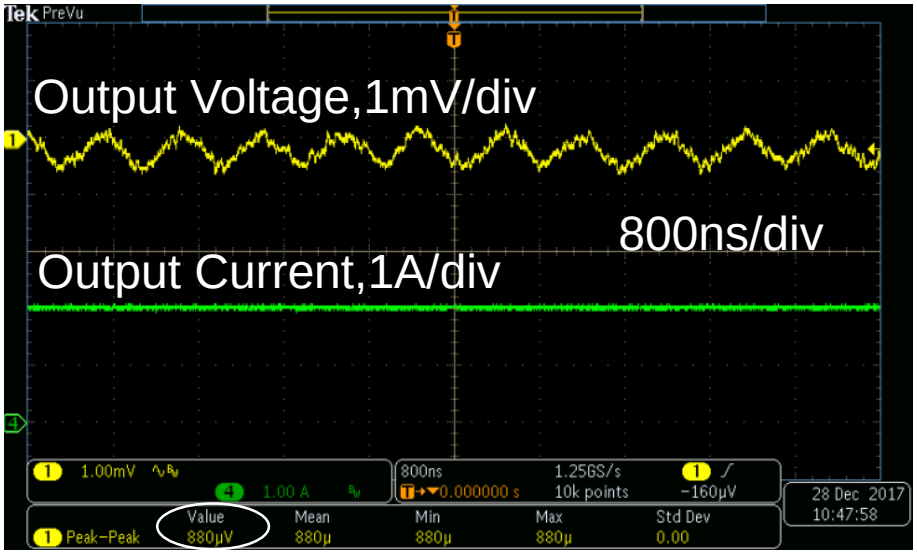
Vo=1.8V,I_o=0A

$V_{o,P-P}$=1.04mV



Vo=1.8V,I_o=2A

$V_{o,P-P}$=0.88mV



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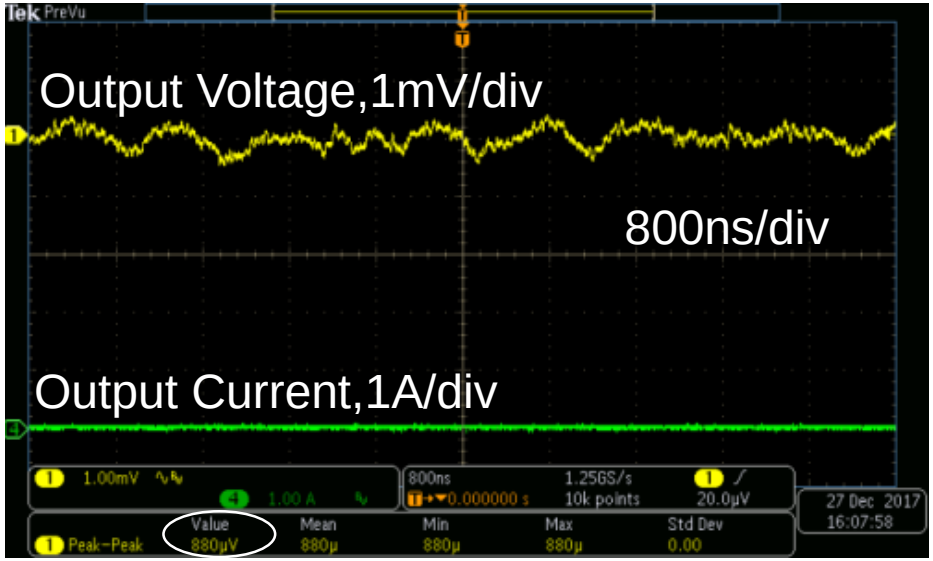
DAC_AVCC Voltage Ripple

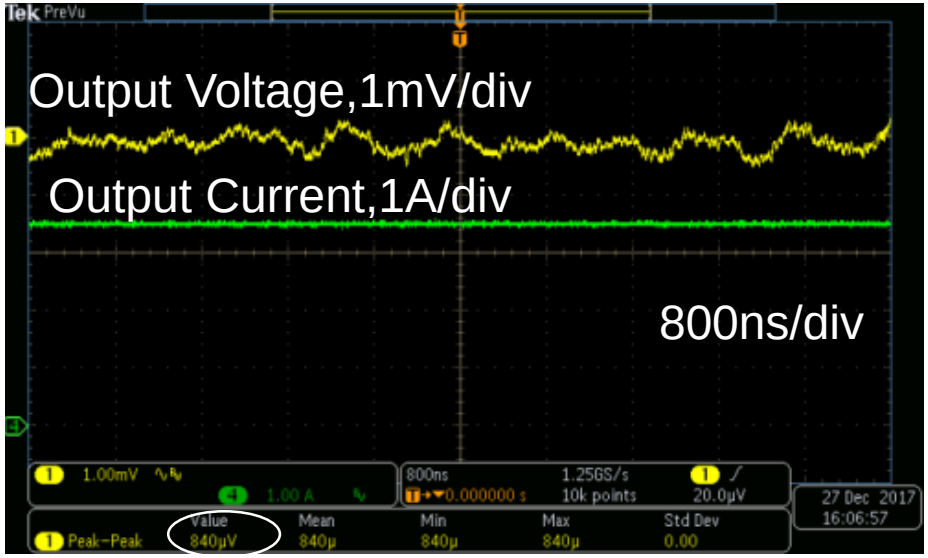
Vo=0.925V,I_o=0A

$V_{o,P-P}$=0.88mV



Vo=0.925V,I_o=3.5A

$V_{o,P-P}$=0.84mV



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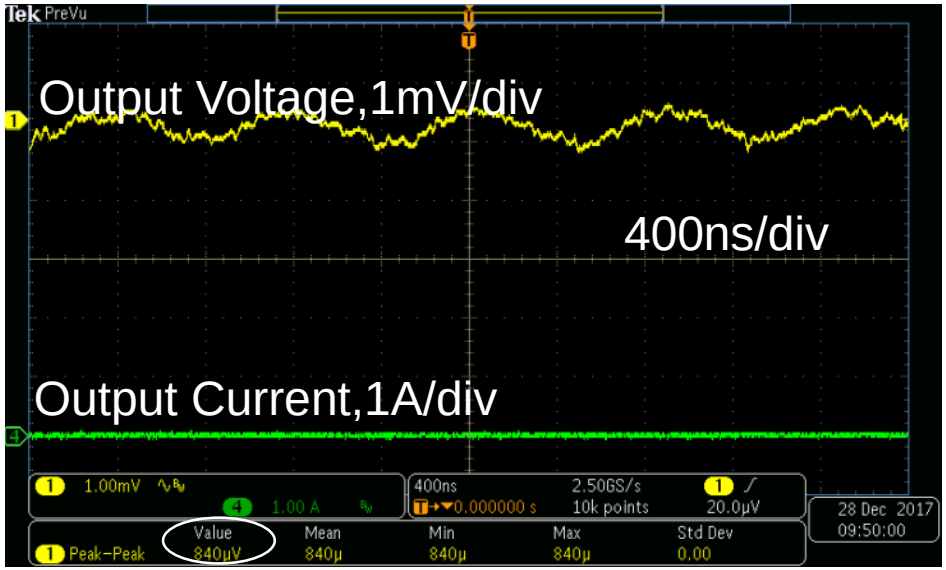
DAC_AVCCAUX Voltage Ripple

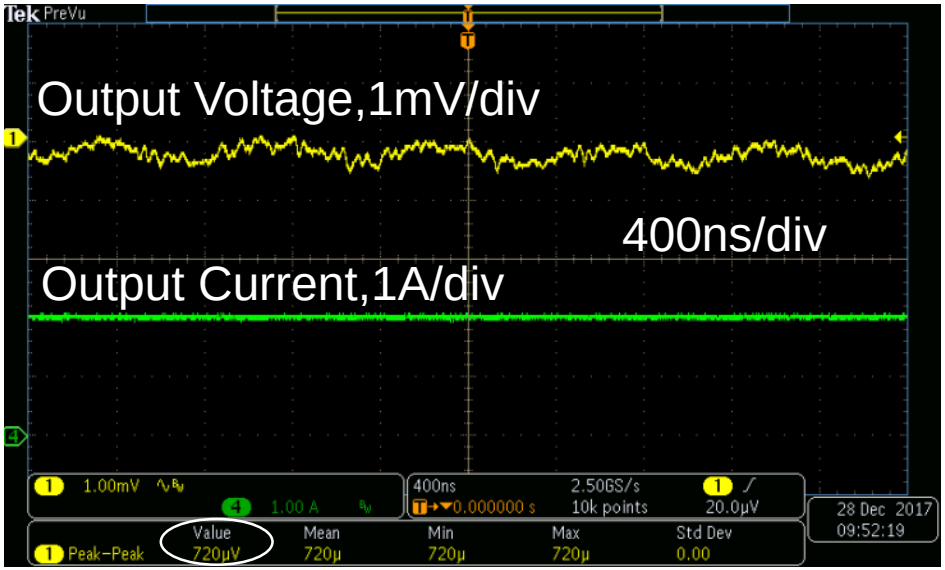
Vo=1.8V,I_o=0A

$V_{o,P-P}$=0.84mV



Vo=1.8V,I_o=2A

$V_{o,P-P}$=0.72mV



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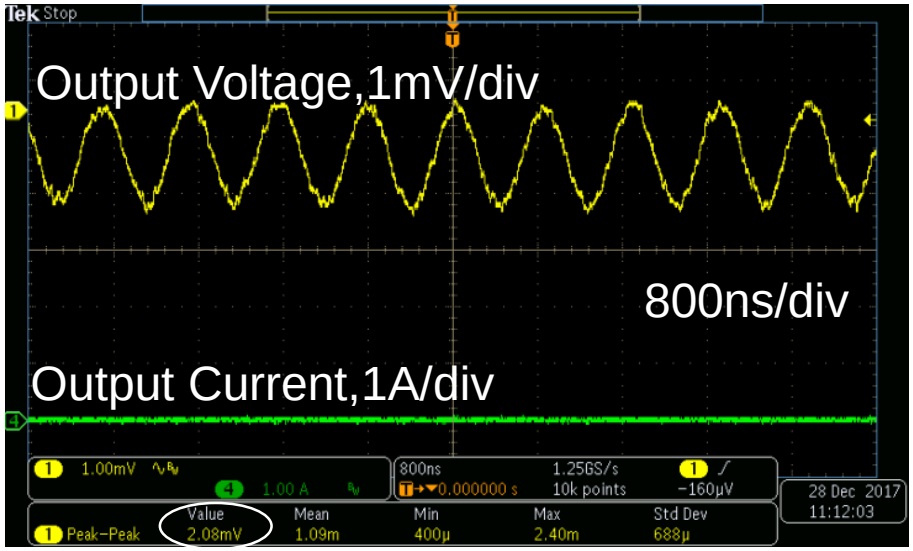
DAC_AVTT Voltage Ripple

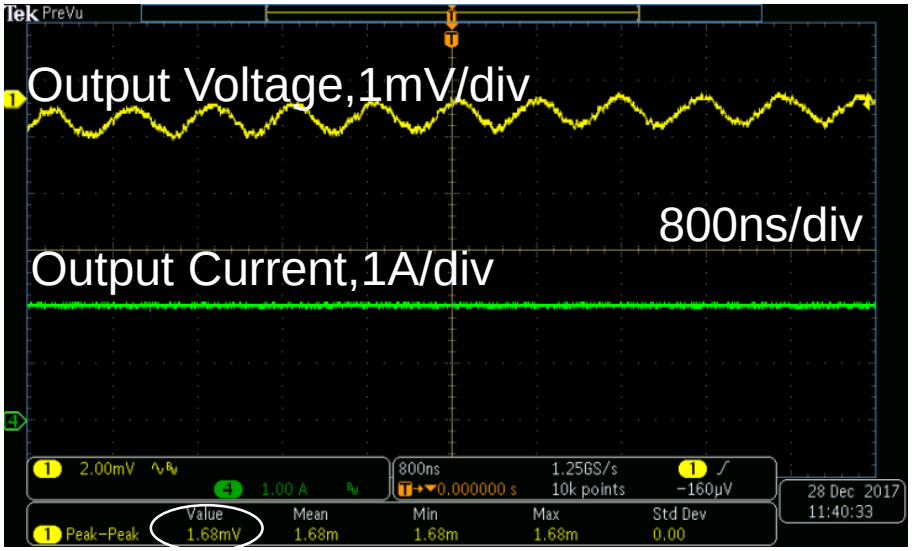
Vo=2.5V,I_o=0A

$V_{o,P-P}$=2.08mV



Vo=2.5V,I_o=2A

$V_{o,P-P}$=1.68mV



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