EVRXLV2-00A Test Report

EVB – Xilinx Versal AI Edge and Prime Series Gen 2

May 2026

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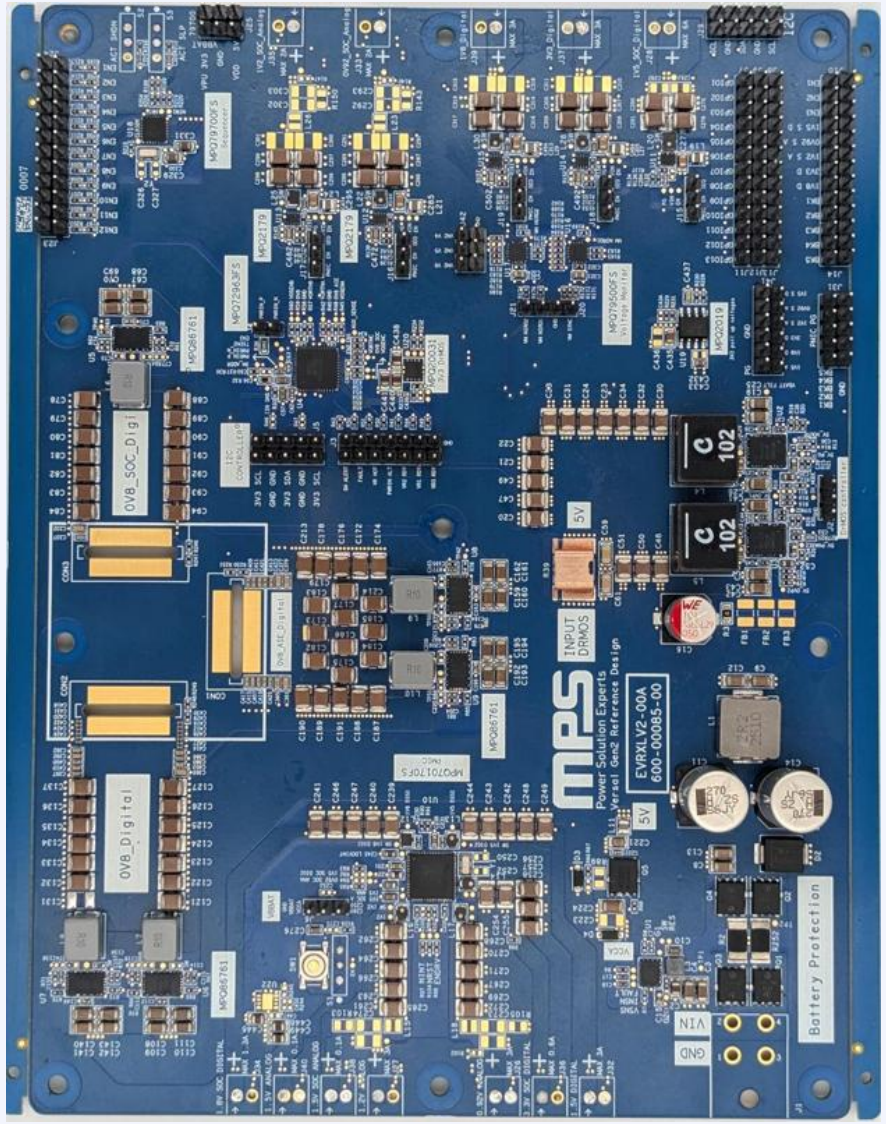
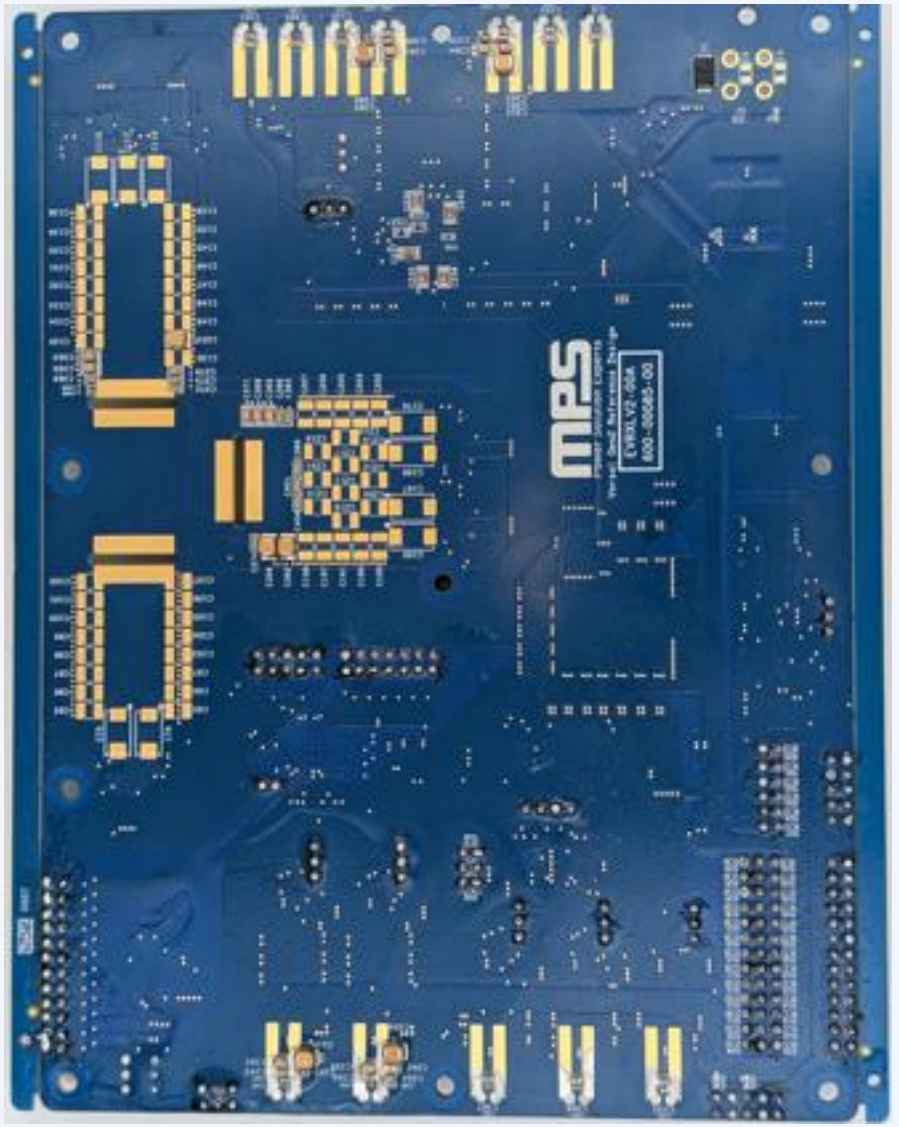
EVRXLV2-00A Board

Top side



Bottom side



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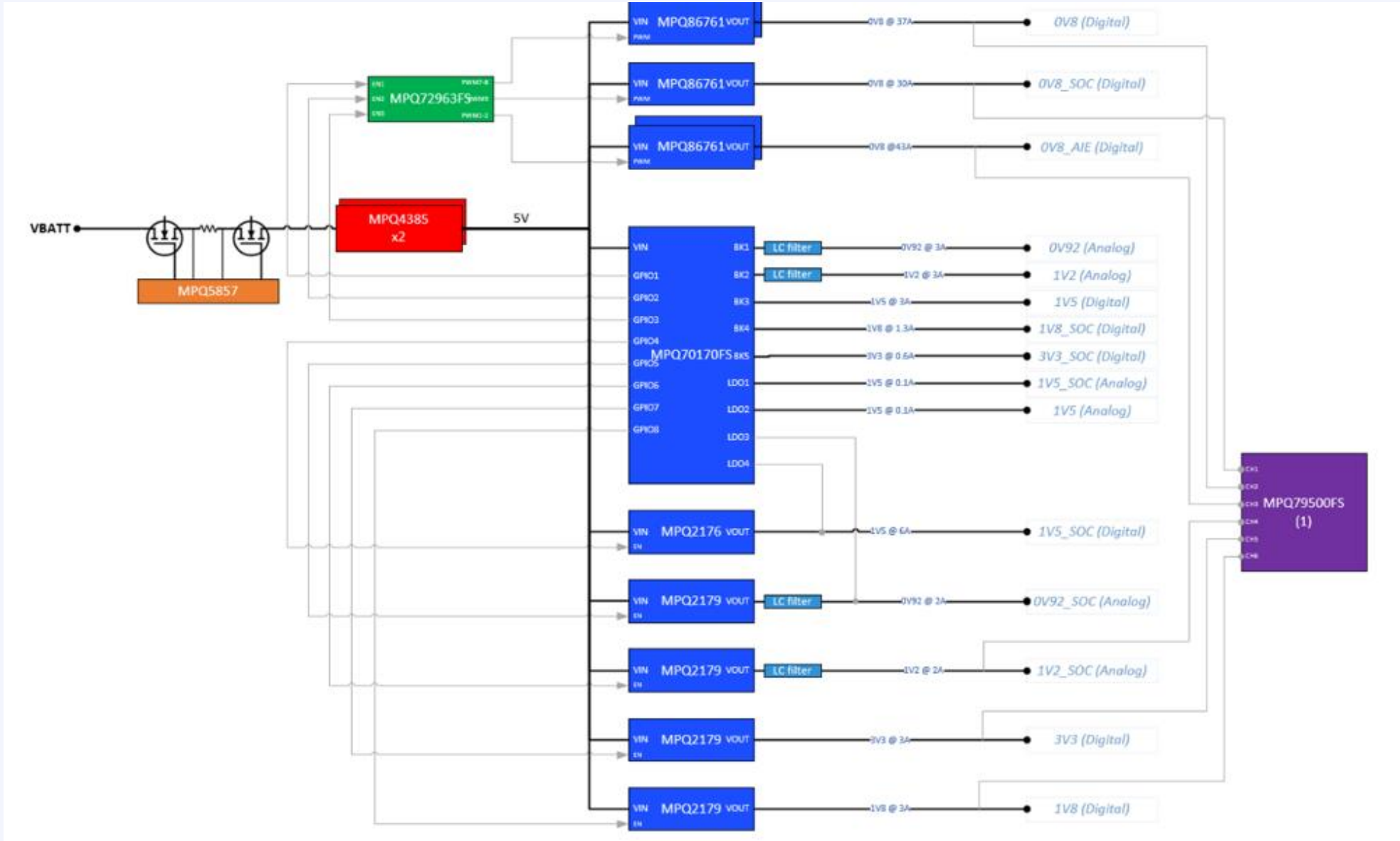
Block Diagram (SoC Mode)



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Test Specs (AI Edge Gen2 SoC Mode)

Sequence	Rail Group	Combined Rails	Nom Voltage (V)	DC Tolerance	AC Transient Margin	Step Load (%)	Current (A)
1.2	0V8_SOC (Digital)	VCC_MIPI, VCC_LPD, VCC_FPD, VCC_USB2, VCC_PAUX, VCC_USB3, VCC_SOC, VCC_IO	0.8	±1%	±2%	33	30
1.3	1V5_SOC (Digital)	VCCAUX_SMON, VCCAUX_LPD, VCCAUX, VCCAUX_PLL	1.5	±1%	±2%	100	6
1.4	0V92_SOC (Analog)	VGTYP_MMI_AVCC**	0.92	±1%	±2%	70	2
1.5	1V5_SOC (Analog)	VGTYP_MMI_AVCCAUX**	1.5	±1%	±2%	70	0.1
1.6	1V2_SOC (Analog)	VGTYP_MMI_AVTT**	1.2	±1%	±2%	70	2
1.1	1V8_SOC (Digital)	VCCIO_MIPI, VCCO_PSIO, VCCIO_PAUX, VCCREG_USB2, VCCIO_USB3	1.8	±1%	±2%	100	1.3
1.1	3V3_SOC (Digital)	VCCO_PSIO, VCCIO_USB2	3.3	±1%	+2% - 4%	100	0.6
2.2	0V8 (Digital)	VCC_RAM, VCCINT*	0.8	±1%	±17mV	33	37
2.1	1V5 (Digital)	VCCO_HDIO	1.5	±1%	±2%	100	3
2.3	0V92 (Analog)	VGTYP_AVCC**	0.92	±1%	±2%	70	3
2.4	1V5 (Analog)	VGTYP_AVCCAUX**	1.5	±1%	±2%	70	0.1
2.5	1V2 (Analog)	VGTYP_AVTT**	1.2	±1%	±2%	70	3
2.1	1V8 (Digital)	VCCO_HDIO	1.8	±1%	±2%	100	3
2.1	3V3 (Digital)	VCCO_HDIO	3.3	±1%	+2% - 4%	100	3
3.1	0V8_AIE (Digital)	VCC_AIE*	0.8	±1%	±17mV	33	43

* slew rate of 200A/us for VCCINT and VCC_AIE. All others 10A/us

** AC noise limit <10mVpp

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Test Specs (Prime Gen2 SoC Mode)

Sequence	Rail Group	Combined Rails	Nom Voltage (V)	DC Tolerance	AC Transient Margin	Step Load (%)	Current (A)
1.2	0V8_SOC (Digital)	VCC_MIPI, VCC_LPD, VCC_FPD, VCC_USB2, VCC_PAUX, VCC_USB3, VCC_SOC, VCC_IO	0.8	±1%	±2%	33	23
1.3	1V5_SOC (Digital)	VCCAUX_SMON, VCCAUX_LPD, VCCAUX, VCCAUX_PLL	1.5	±1%	±2%	100	6
1.4	0V92_SOC (Analog)	VGTYP_MMI_AVCC**	0.92	±1%	±2%	70	2
1.5	1V5_SOC (Analog)	VGTYP_MMI_AVCCAUX**	1.5	±1%	±2%	70	0.1
1.6	1V2_SOC (Analog)	VGTYP_MMI_AVTT**	1.2	±1%	±2%	70	2
1.1	1V8_SOC (Digital)	VCCIO_MIPI, VCCO_PSIO, VCCIO_PAUX, VCCREG_USB2, VCCIO_USB3	1.8	±1%	±2%	100	1.3
1.1	3V3_SOC (Digital)	VCCO_PSIO, VCCIO_USB2	3.3	±1%	+2% - 4%	100	0.6
2.2	0V8 (Digital)	VCC_RAM, VCCINT*	0.8	±1%	±17mV	33	37
2.1	1V5 (Digital)	VCCO_HDIO	1.5	±1%	±2%	100	3
2.3	0V92 (Analog)	VGTYP_AVCC**	0.92	±1%	±2%	70	3
2.4	1V5 (Analog)	VGTYP_AVCCAUX**	1.5	±1%	±2%	70	0.1
2.5	1V2 (Analog)	VGTYP_AVTT**	1.2	±1%	±2%	70	3
2.1	1V8 (Digital)	VCCO_HDIO	1.8	±1%	±2%	100	3
2.1	3V3 (Digital)	VCCO_HDIO	3.3	±1%	+2% - 4%	100	3

* slew rate of 200A/us for VCCINT and VCC_AIE. All others 10A/us

** AC noise limit <10mVpp

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Ripple and Transients

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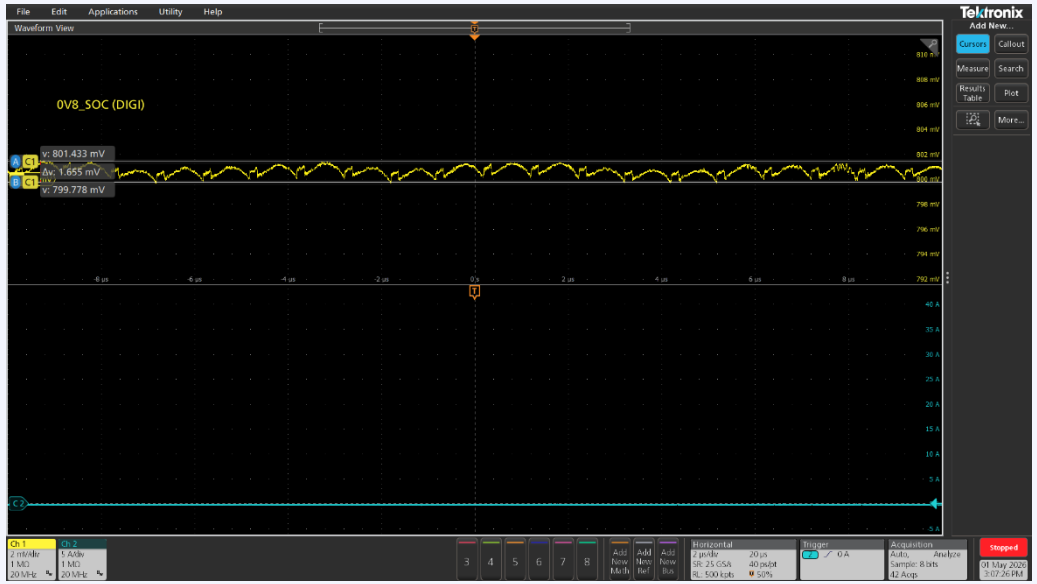
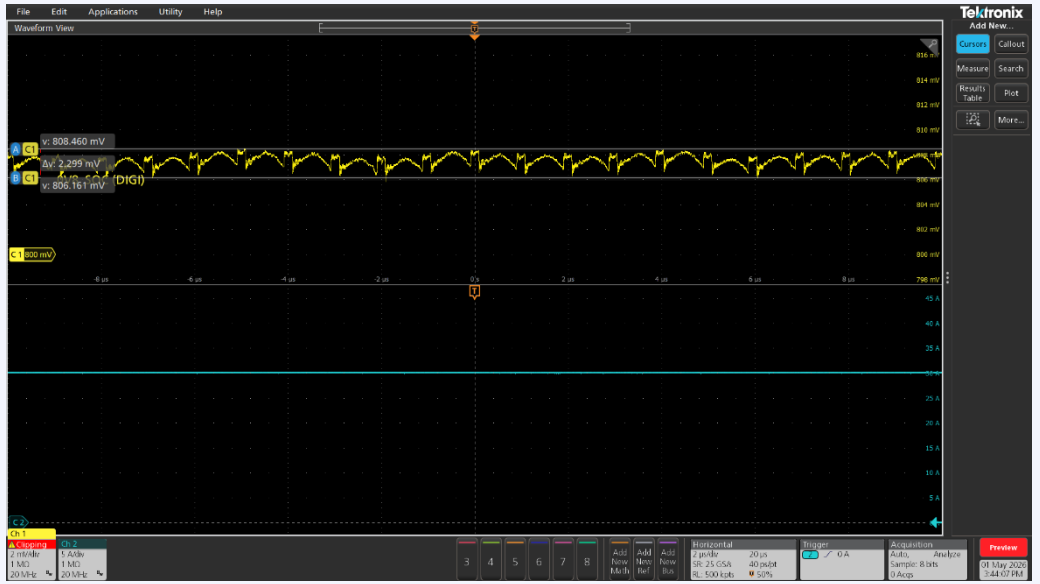
0V8_SOC (Digital) Ripple 0.8Vout

0A



30A



- Steady state ripple 1.66mVp-p at 0A
- Steady state ripple 2.3mVp-p at 30A

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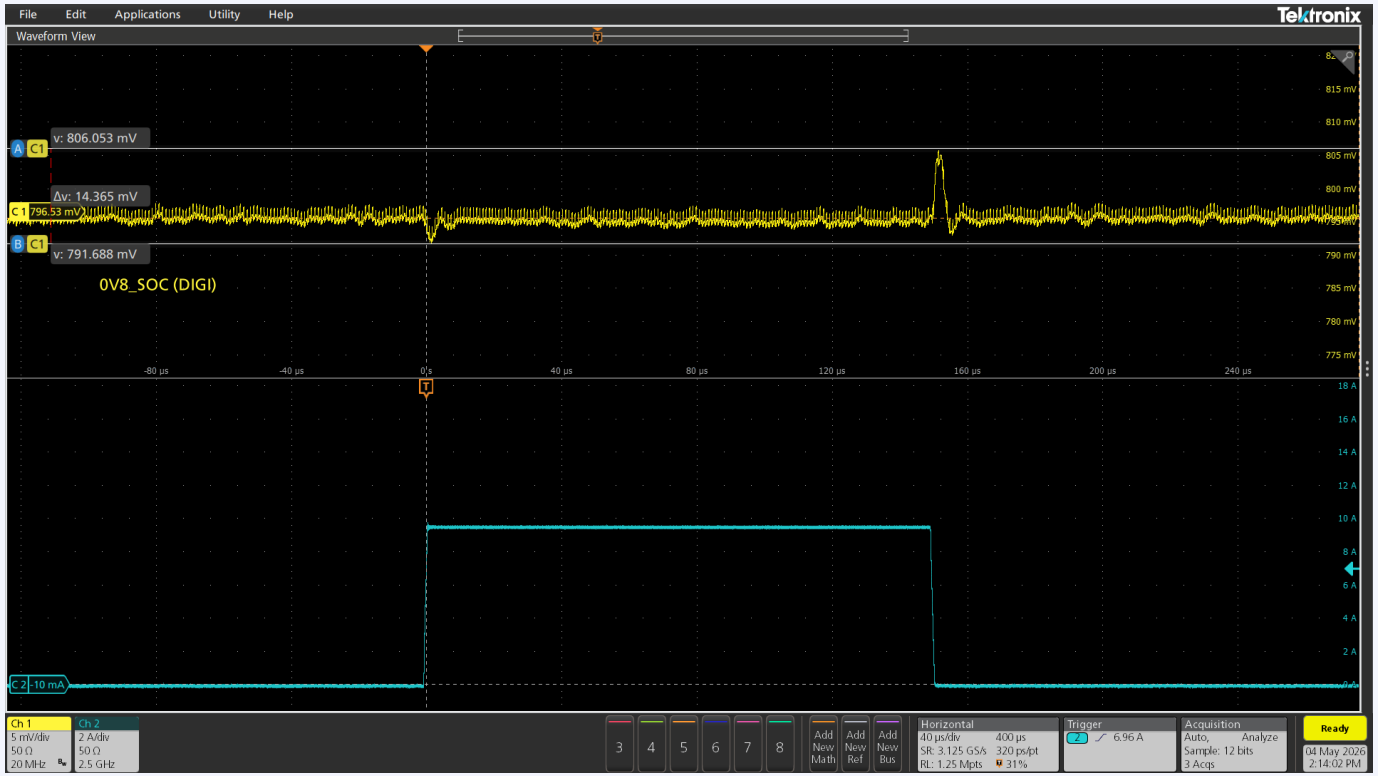
0V8_SOC (Digital) Transient – 0.8Vout

0A → 10A → 0A

10A/us



- Vout ripple -0.608% (-4.842mV) to +1.2% (9.523mV) with load transient

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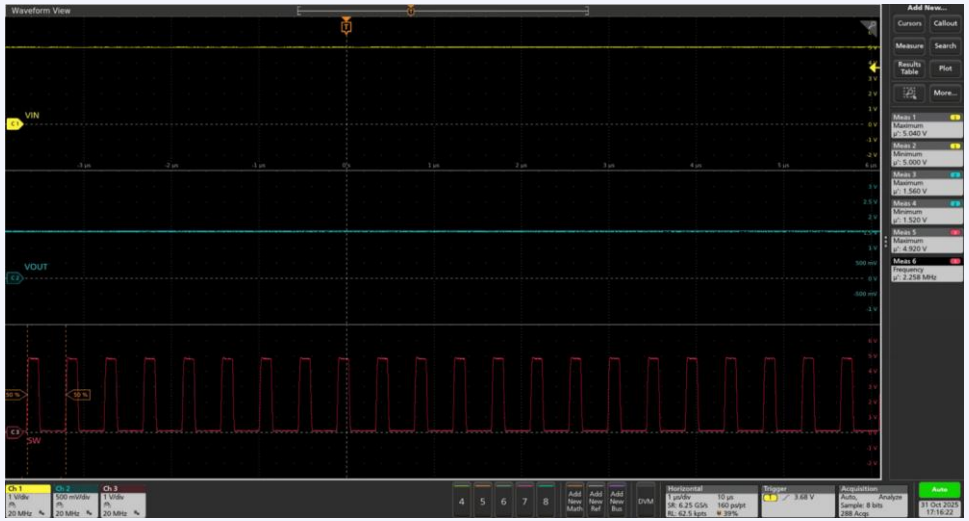
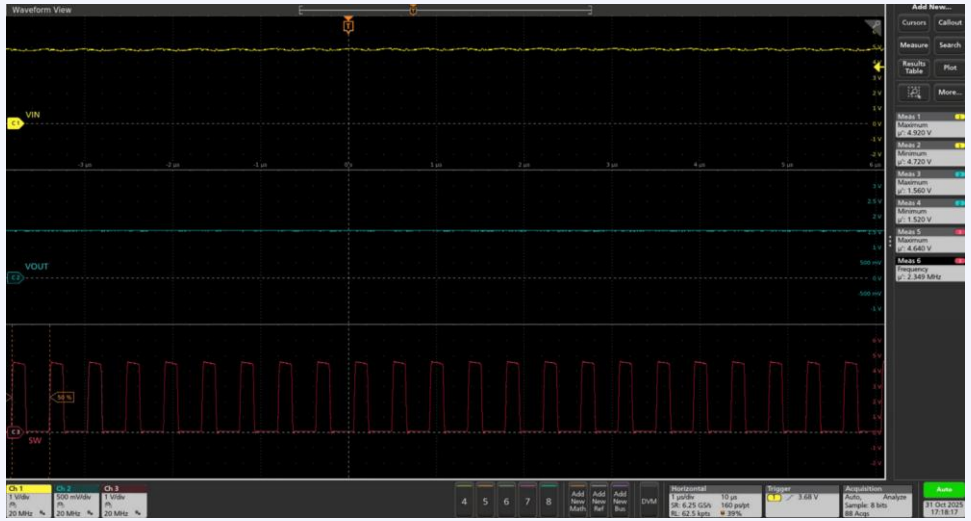
1V5_SOC (Digital) Ripple 1.5Vout

0A



6A



- Steady state ripple 6mVp-p

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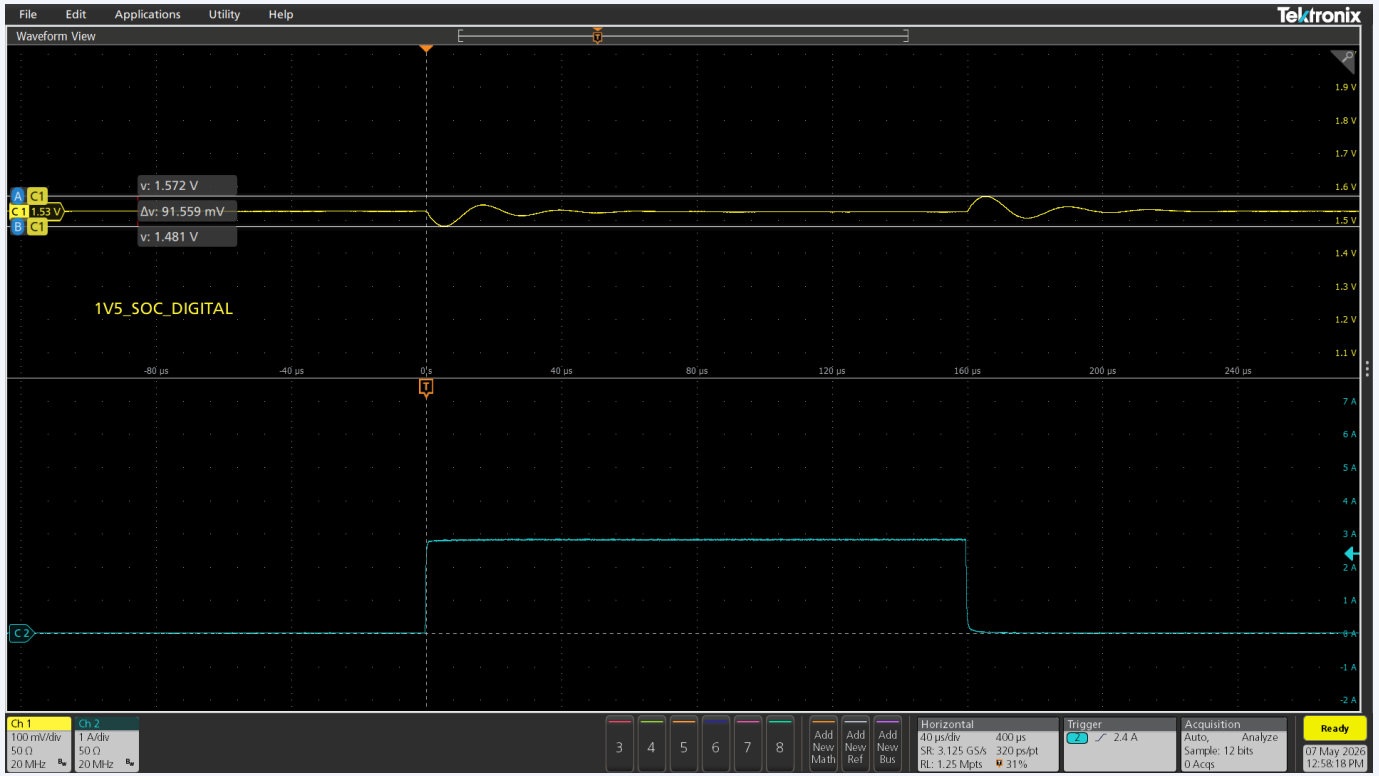
1V5_SOC (Digital) Transient 1.5Vout

0A → 3A → 0A



- Vout ripple -3.2% (-49mV) to +2.7% (42mV) with load transient

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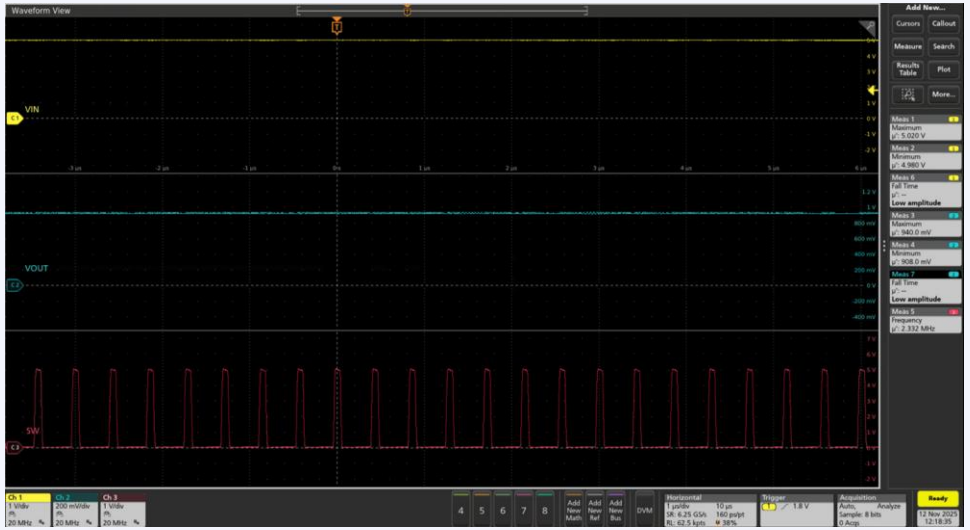
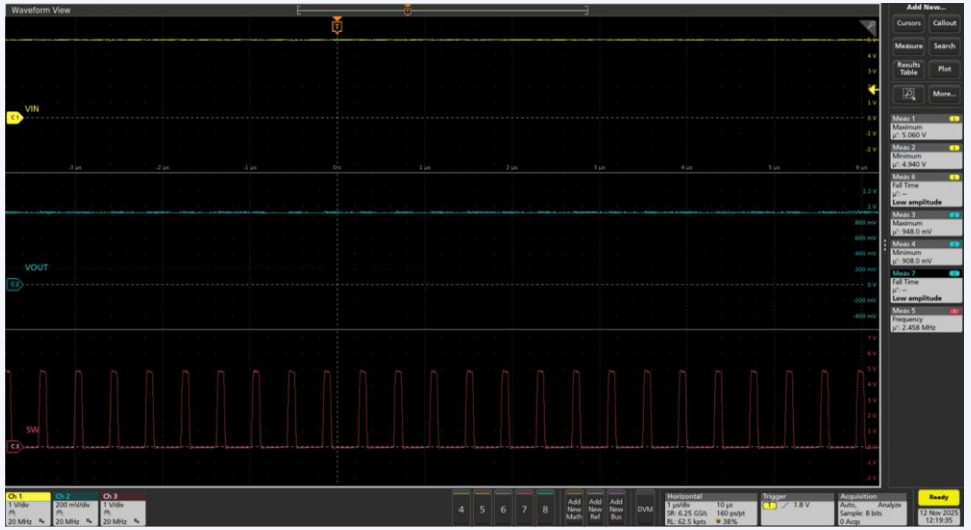
0V92_SOC (Analog) Ripple 0.92Vout

0A



2A



- Steady state ripple 6mVp-p

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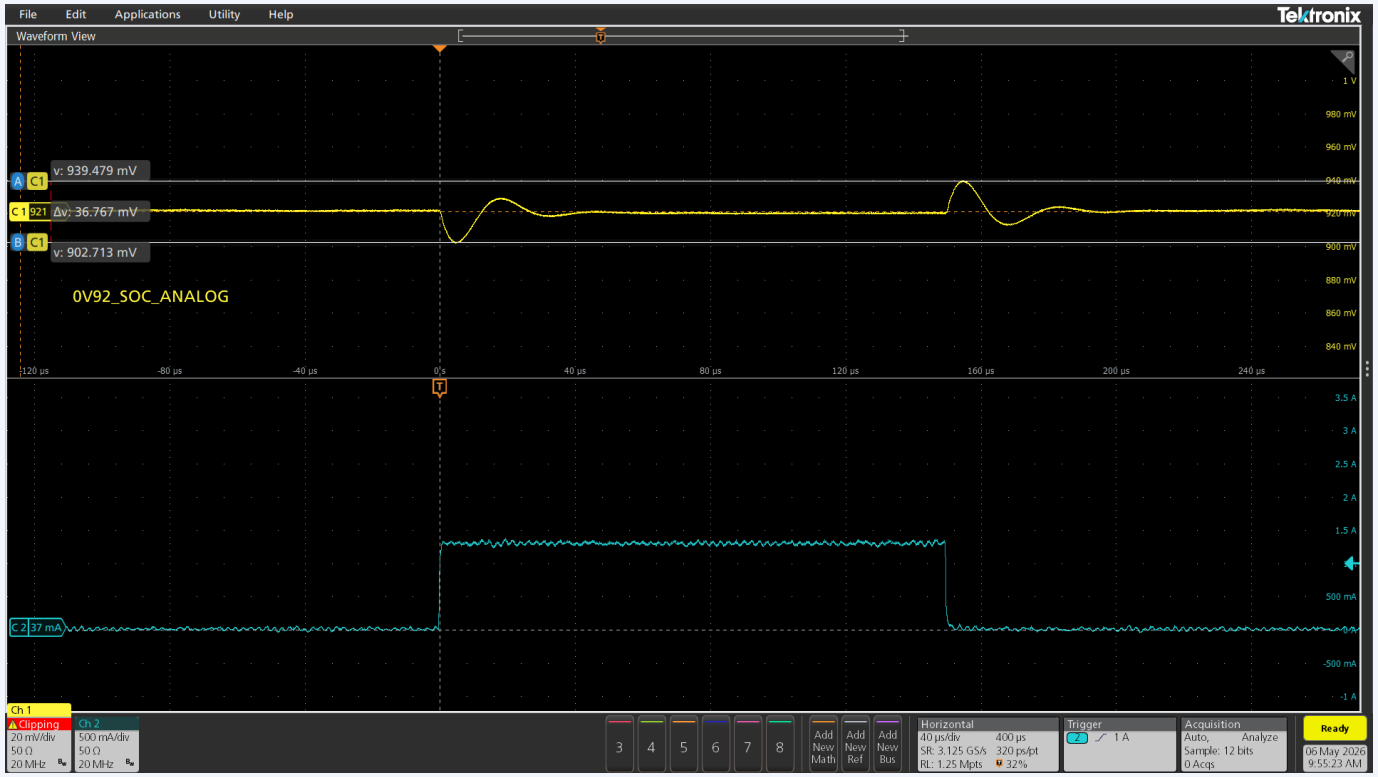
0V92_SOC (Analog) Transient 0.92Vout

0A → 1.4A → 0A



- Vout ripple -1.99% (-18.3mV) to +2.01% (18.48mV) with load transient

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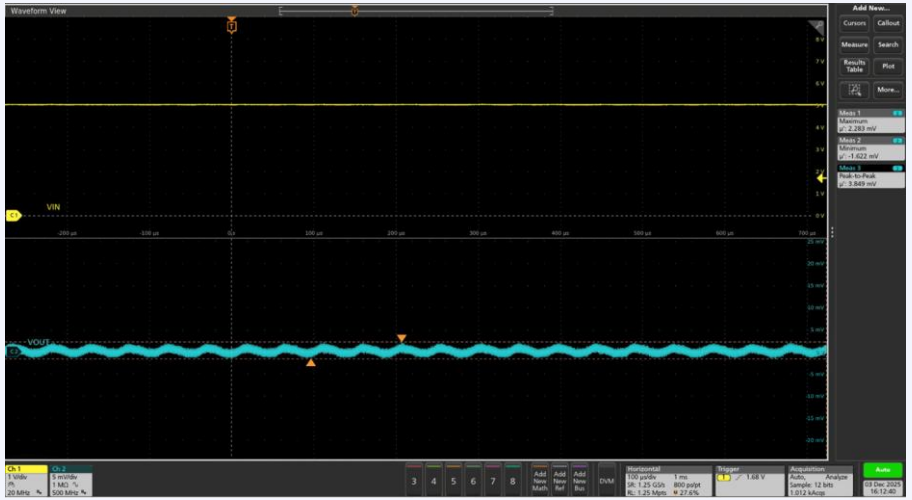
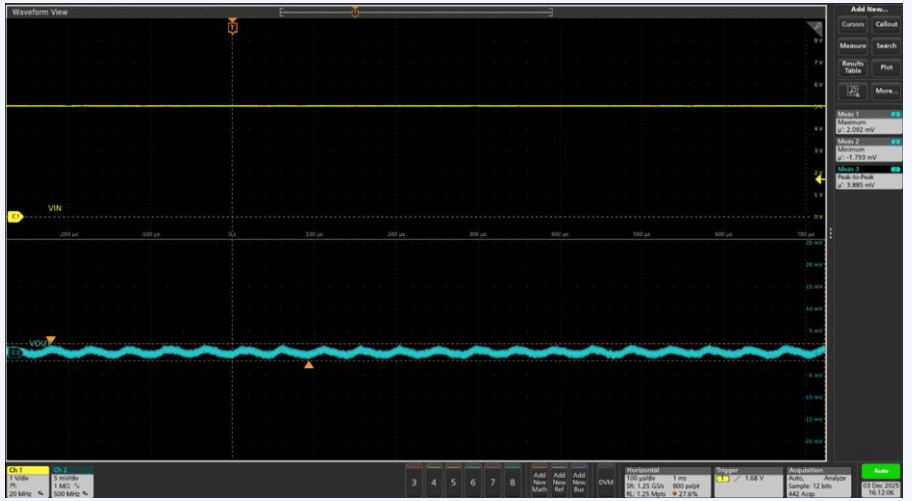
1V5_SOC (Analog) Ripple 1.5Vout

0A



100mA



- Steady state ripple 3.88mVp-p

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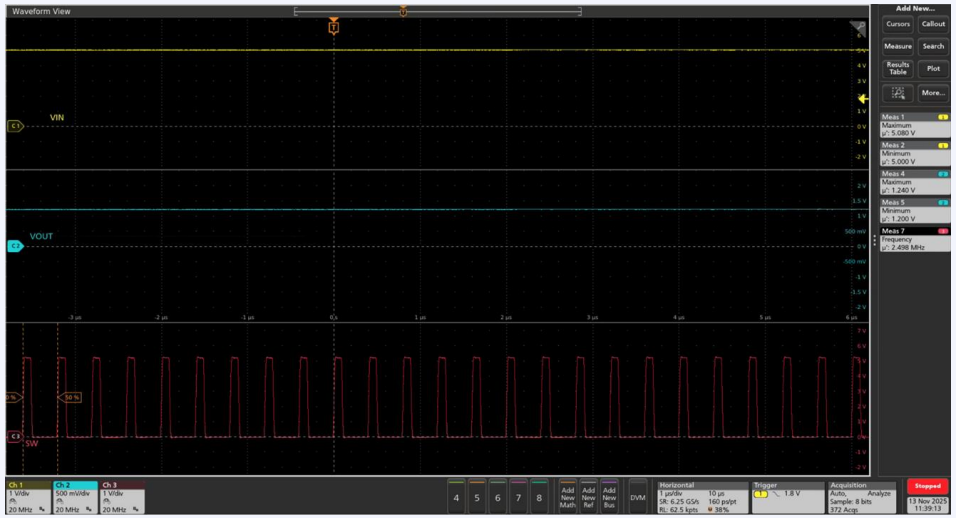
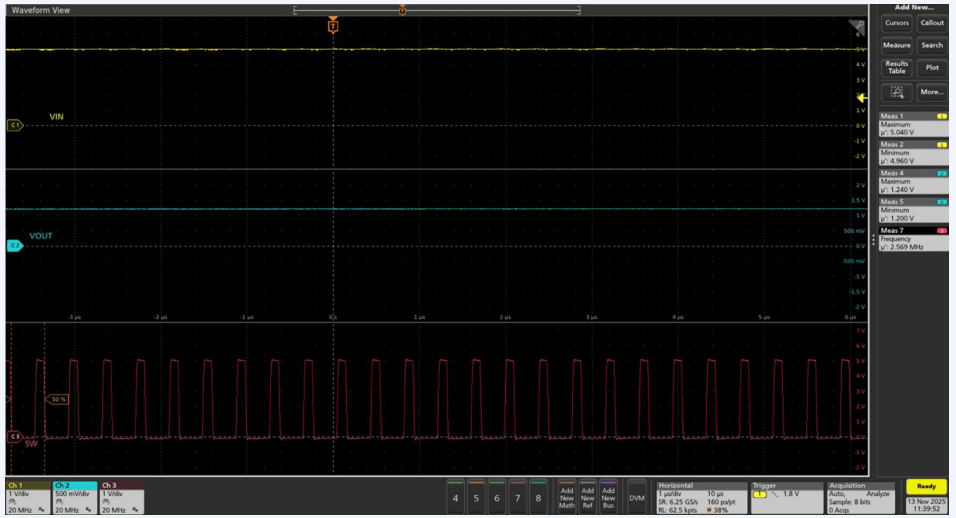
1V2_SOC (Analog) Ripple 1.2Vout

0A



2A



- Steady state ripple 8mVp-p

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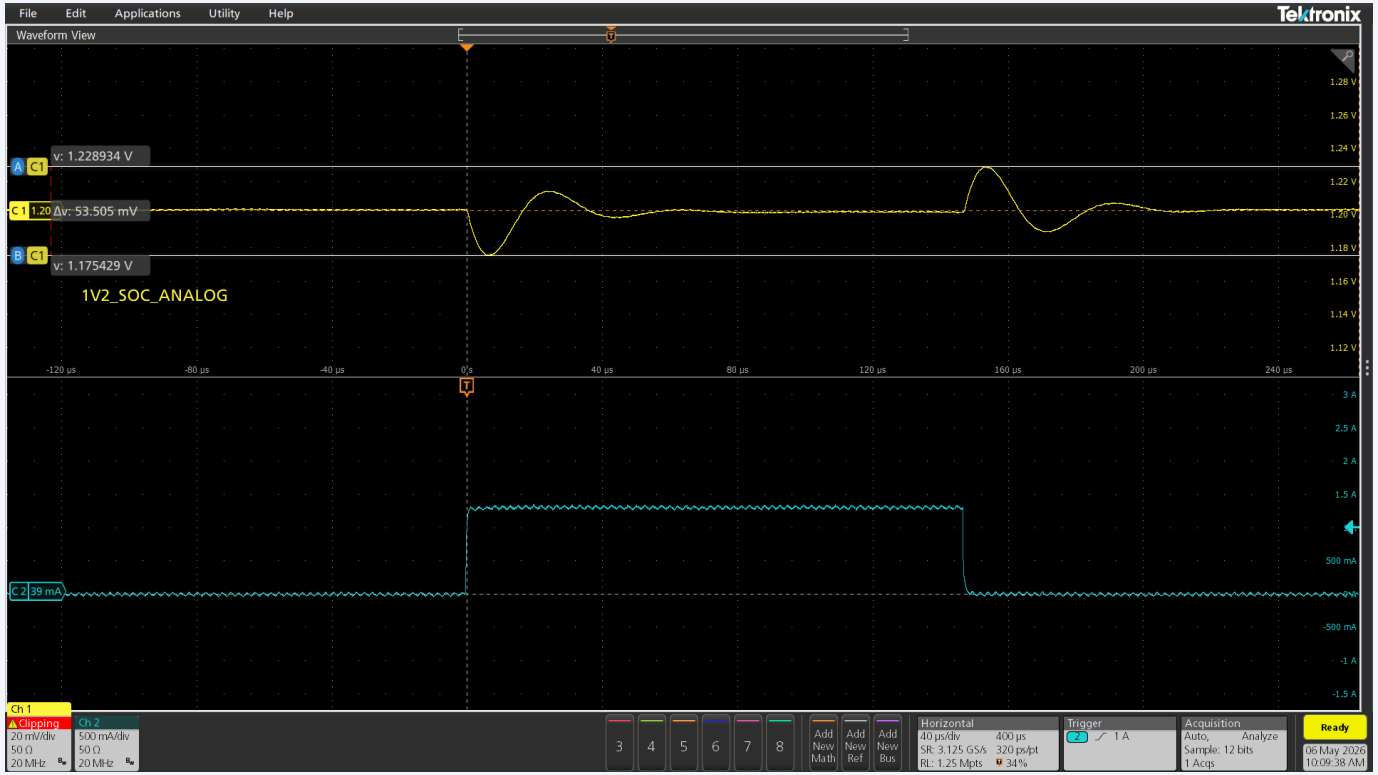
1V2_SOC (Analog) Transient 1.2Vout

0A → 1.4A → 0A



- Vout ripple -2.05% (-24.5mV) to +2.4% (28.9mV) with load transient

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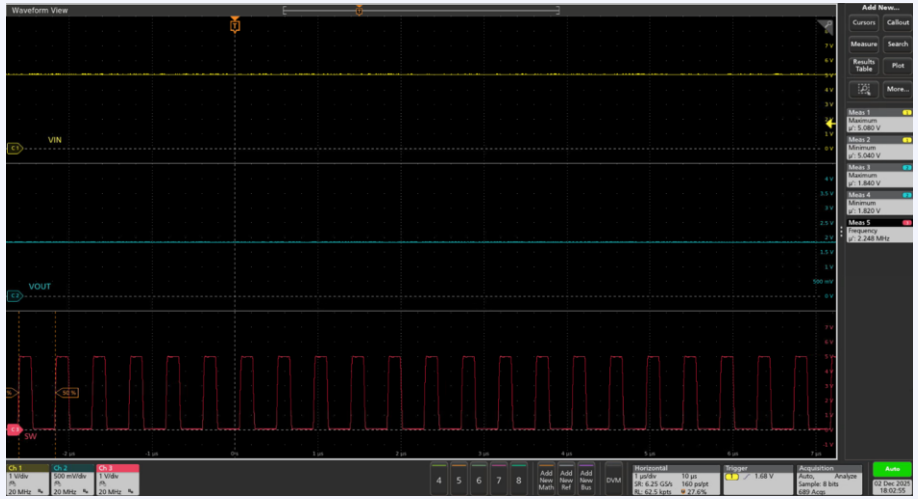
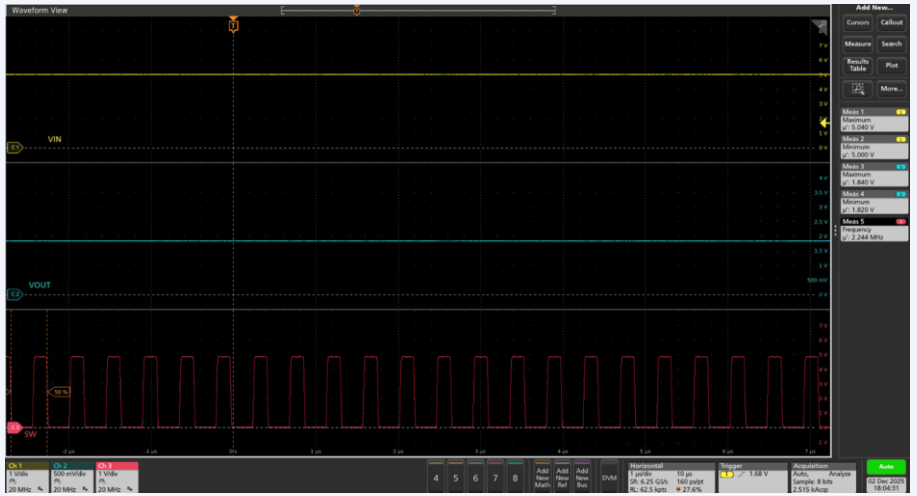
1V8_SOC (Digital) Ripple 1.8Vout

0A



1.3A



- Steady state ripple 5.8mVp-p

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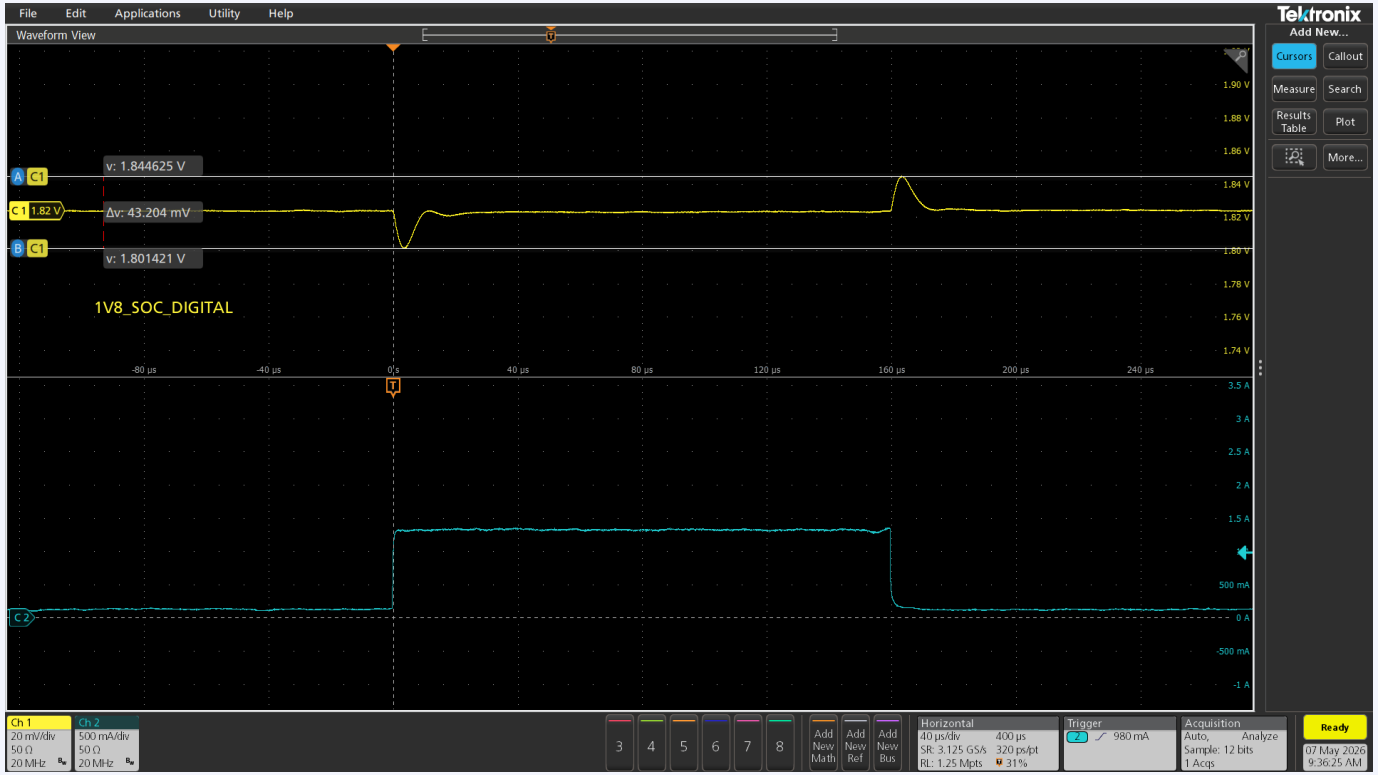
1V8_SOC (Digital) Transient 1.8Vout

0A → 1.3A → 0A



- Vout ripple -1.02% (-18.58mV) to +1.35% (24.63mV) with load transient

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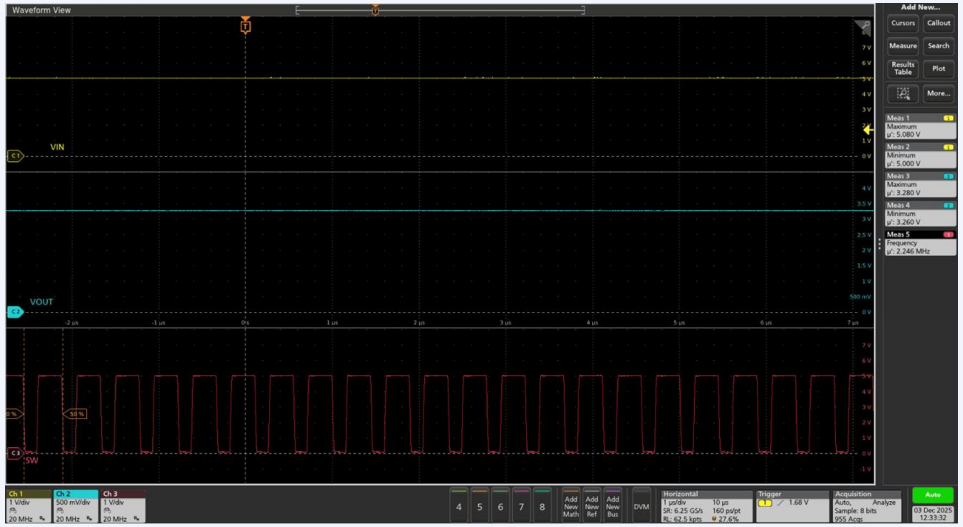
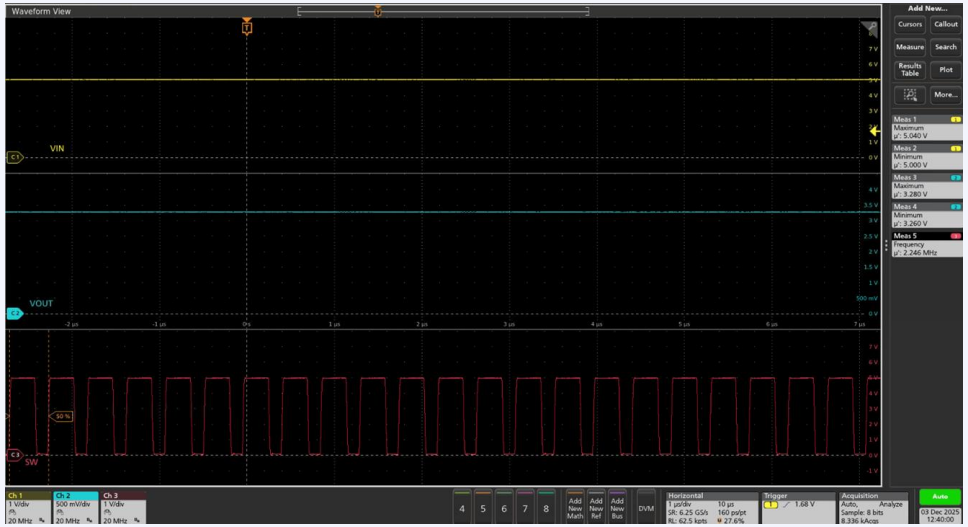
3V3_SOC (Digital) Ripple 3.3Vout

0A



600mA



- Steady state ripple 5.2mVp-p

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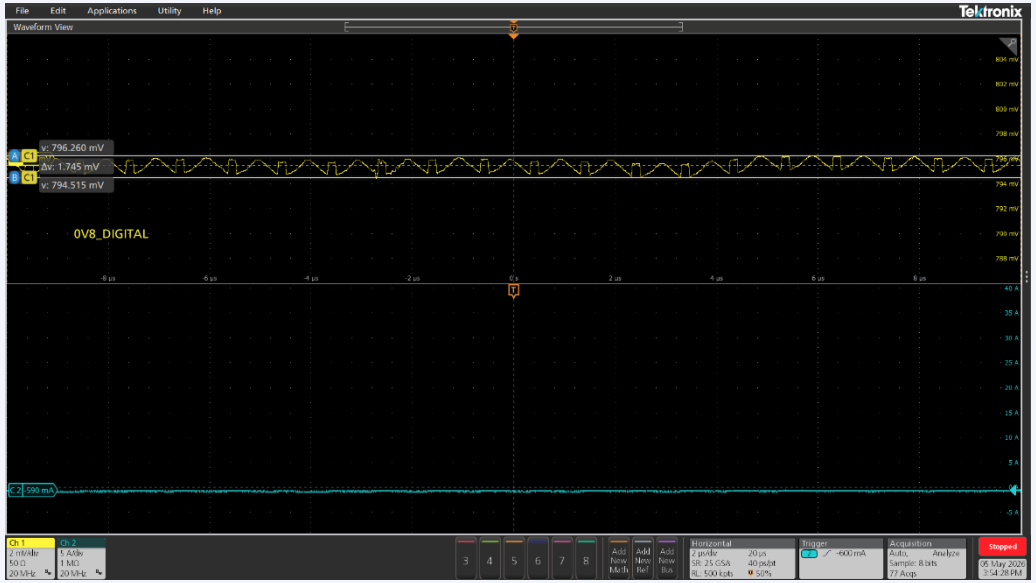
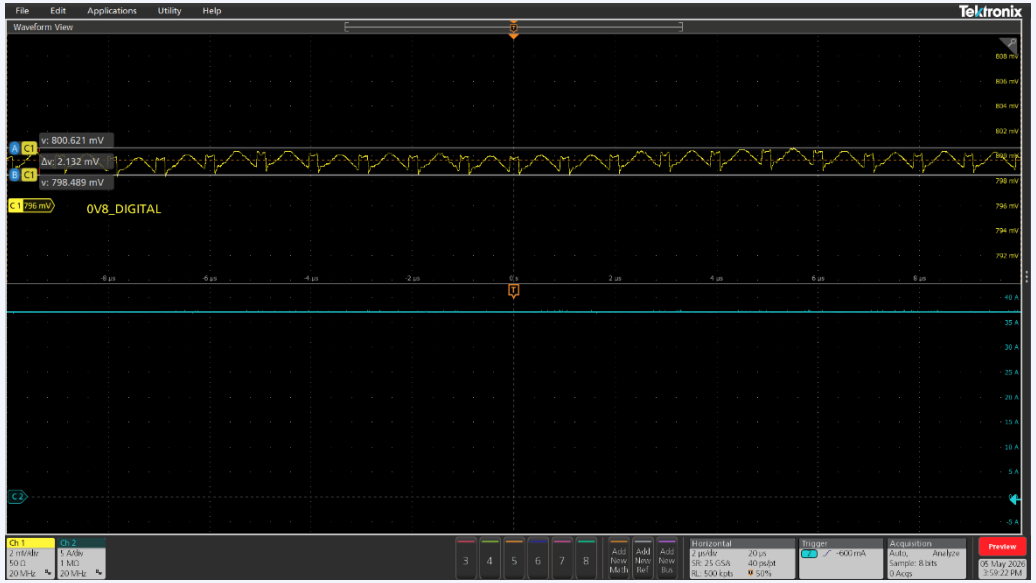
0V8 (Digital) Ripple – 0.8Vout

0A



37A



- Steady state ripple 1.745mVp-p at 0A
- Steady state ripple 2.132mVp-p at 37A

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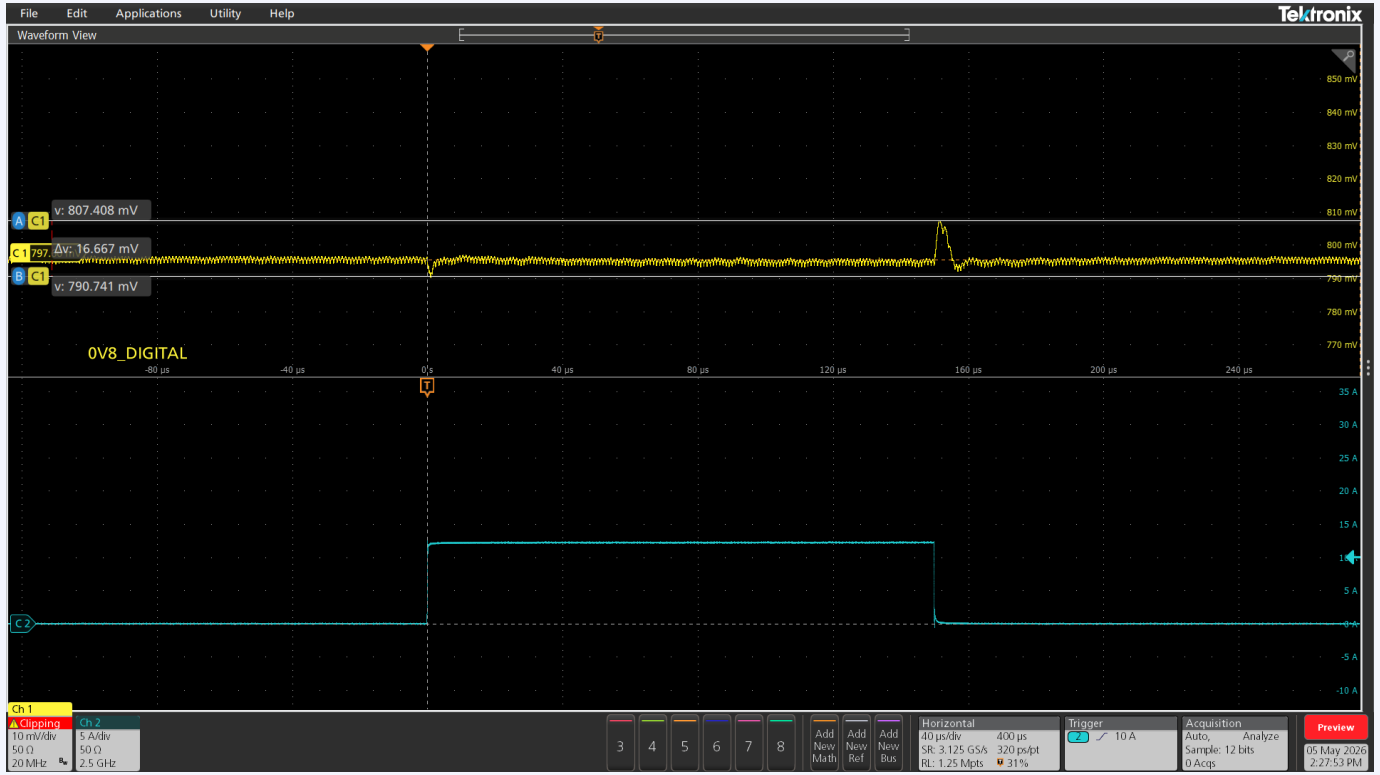
0V8 (Digital) Transient – 0.8Vout

0A → 12A → 0A



- Vout ripple -0.86% (-6.86mV) to +1.23% (9.81mV) with load transient

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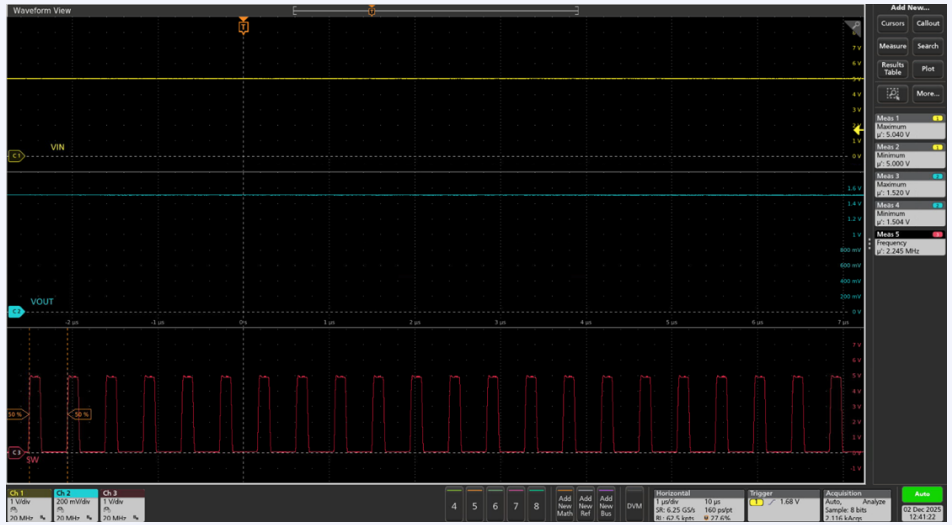
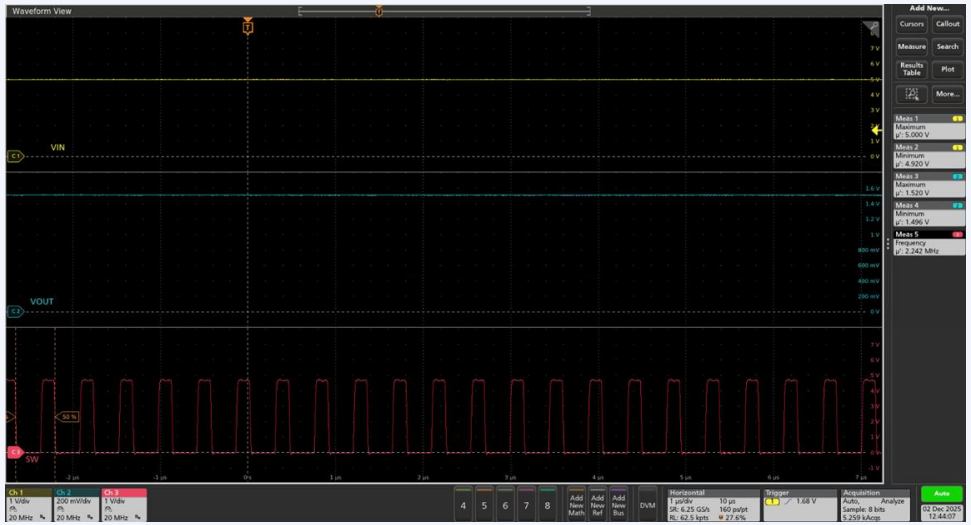
1V5 (Digital) Ripple – 1.5Vout

0A



3A



- Steady state ripple 6mVp-p

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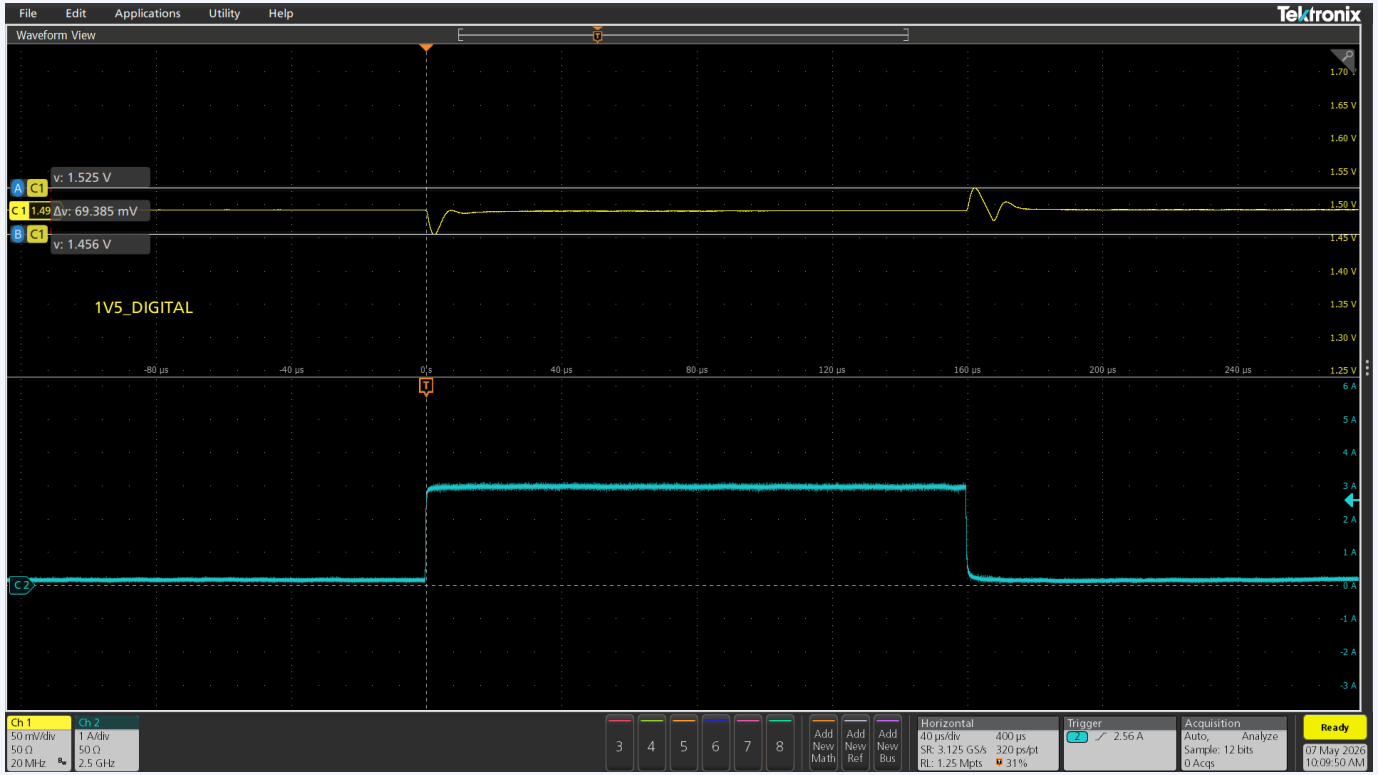
1V5 (Digital) Transient – 1.5Vout

0A → 3A → 0A



- Vout ripple -2.28% (-34mV) to +2.35% (35mV) with load transient

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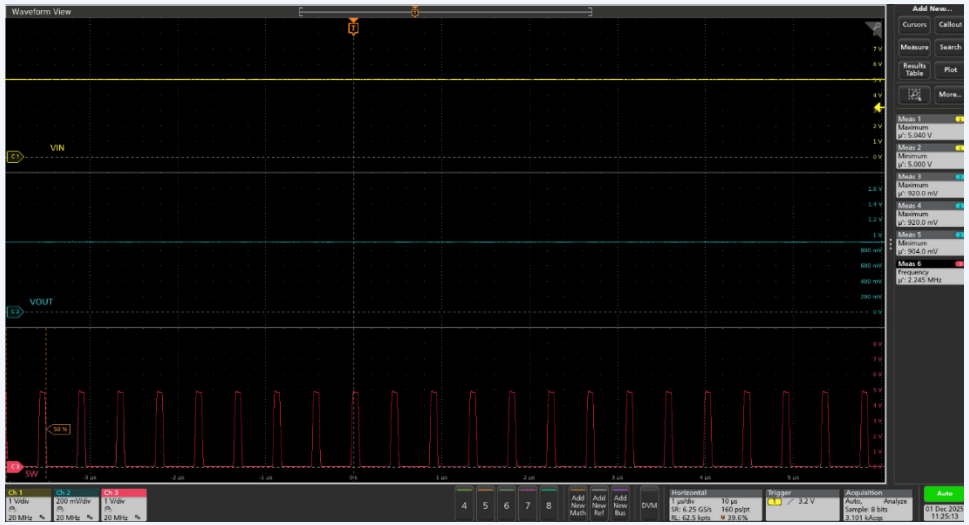
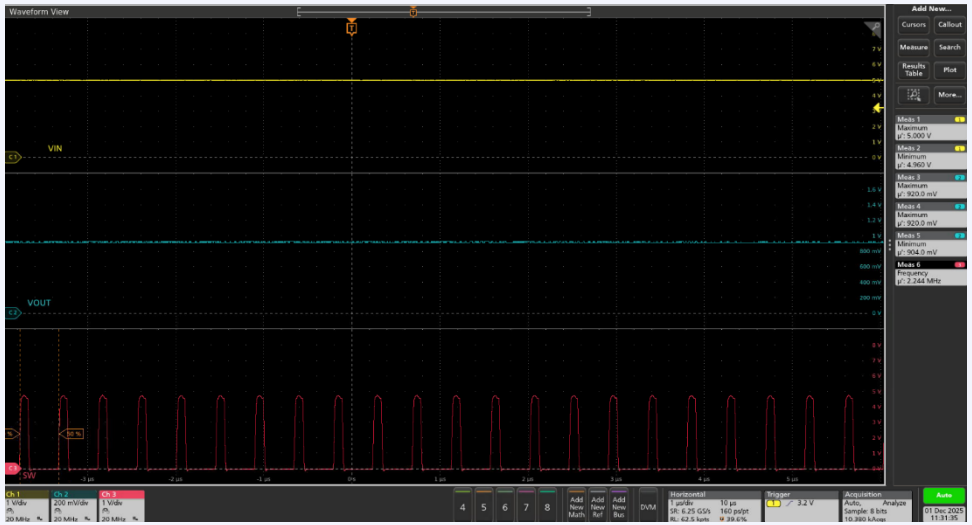
0V92 (Analog) Ripple – 0.92Vout

0A



3A



- Steady state ripple 6mVp-p

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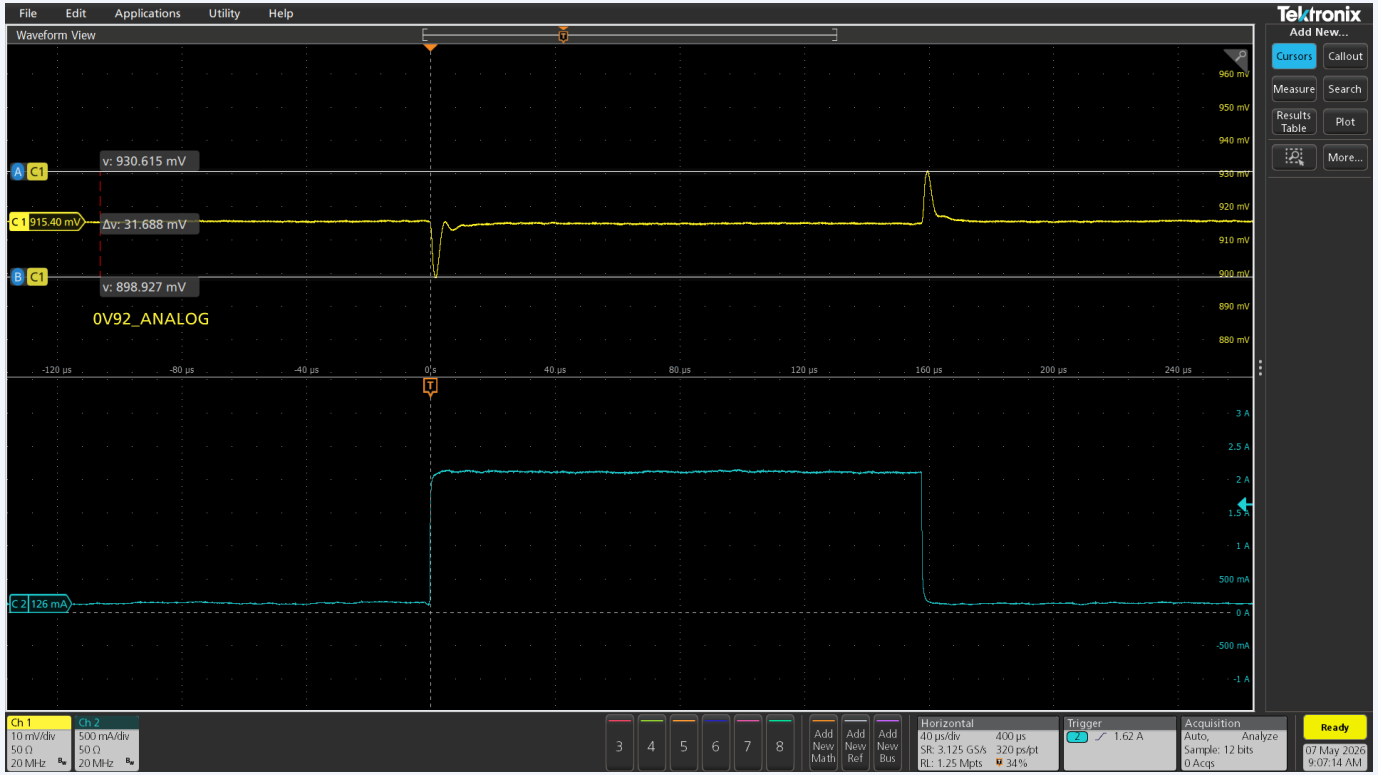
0V92 (Analog) Transient – 0.92Vout

0A → 2.1A → 0A



- Vout ripple -1.79% (-16.47mV) to +1.66% (15.215mV) with load transient

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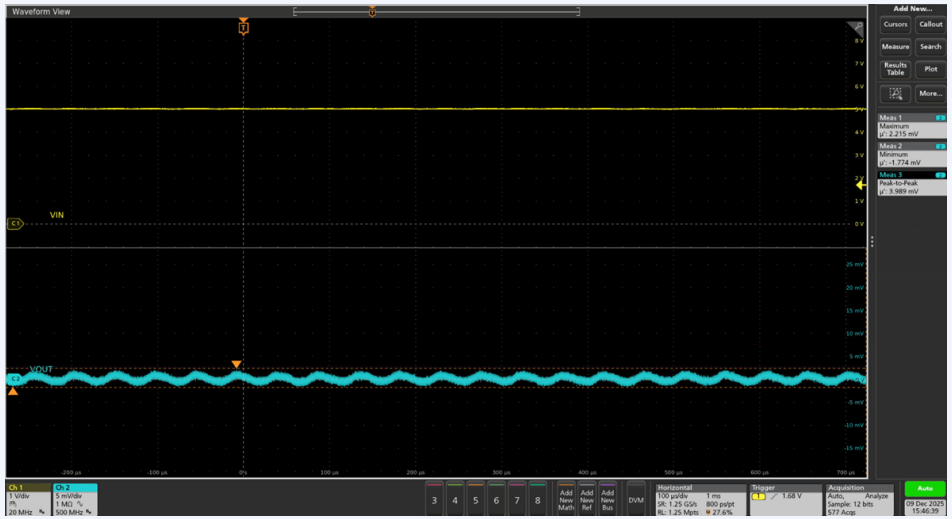
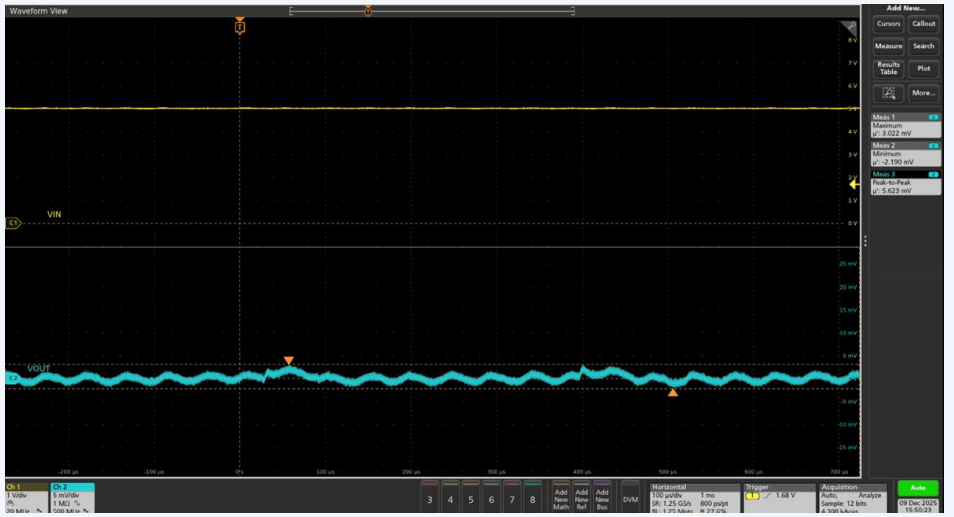
1V5 (Analog) Ripple – 1.5Vout

0A



100mA



- Steady state ripple 5mVp-p

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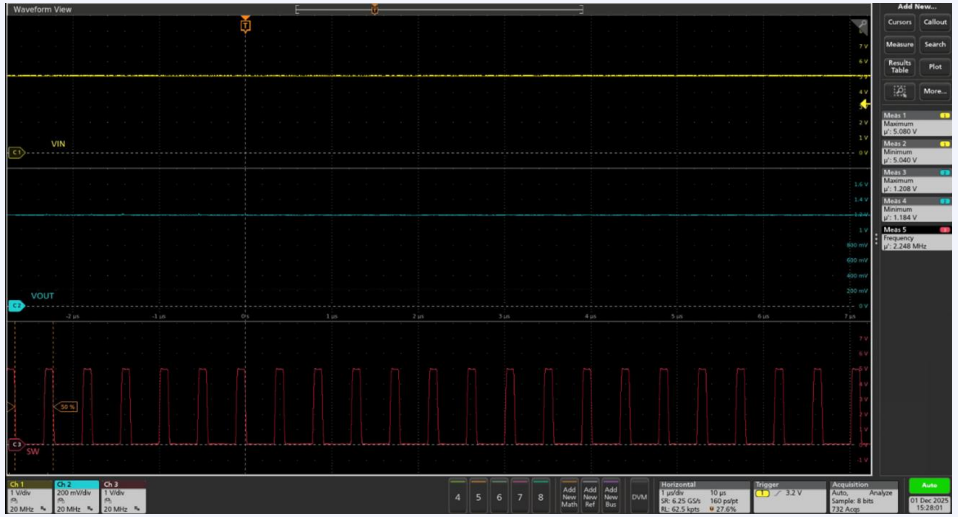
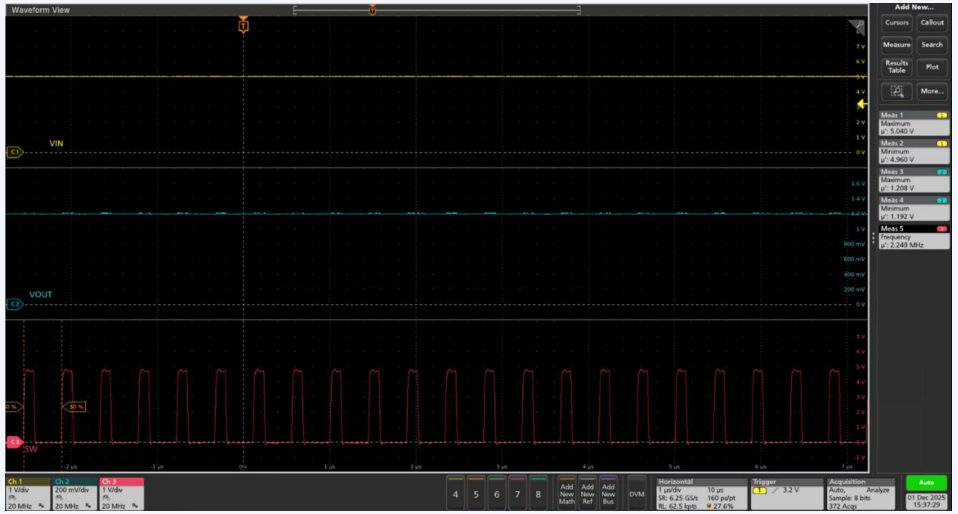
1V2 (Analog) Ripple – 1.2Vout

0A



3A



- Steady state ripple 8mVp-p

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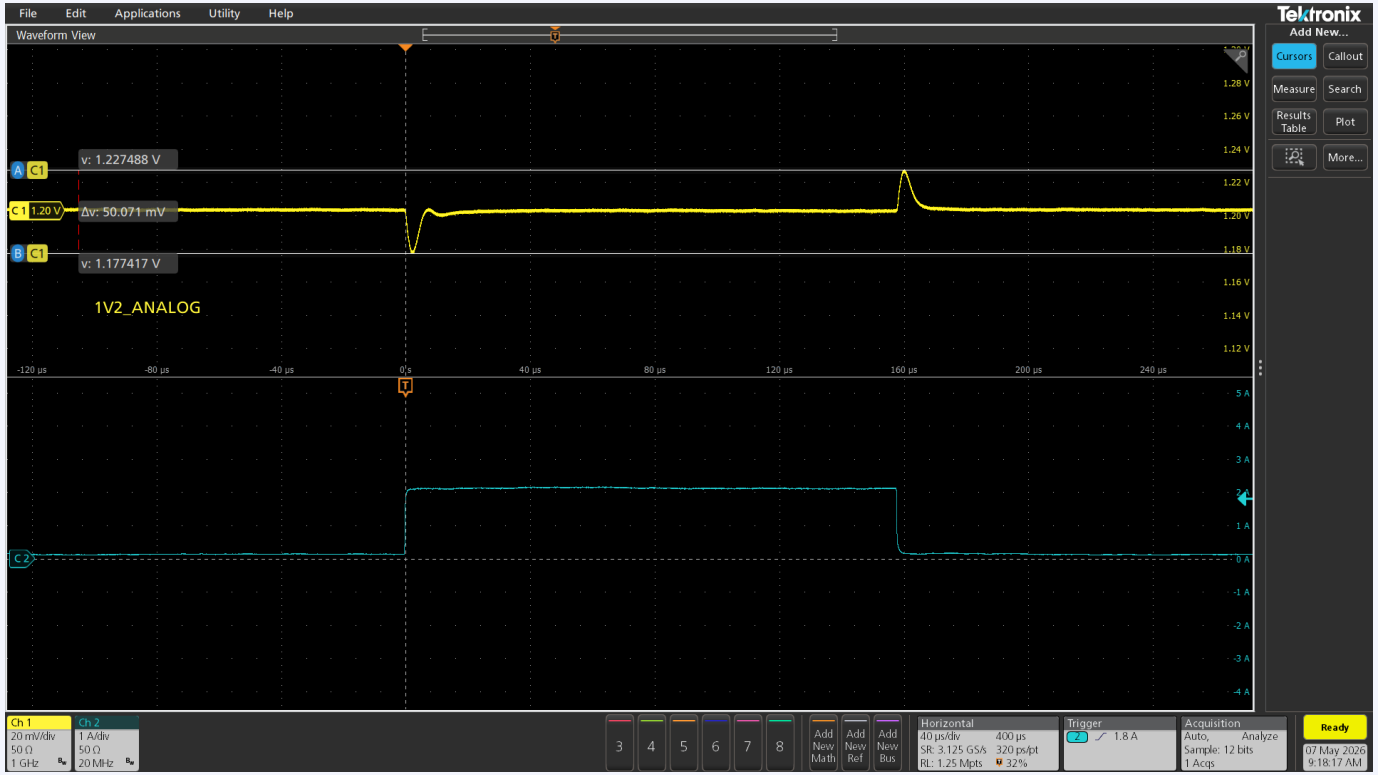
1V2 (Analog) Transient – 1.2Vout

0A → 2.1A → 0A



- Vout ripple -1.88% (-22.6mV) to +2.29% (27.5mV) with load transient

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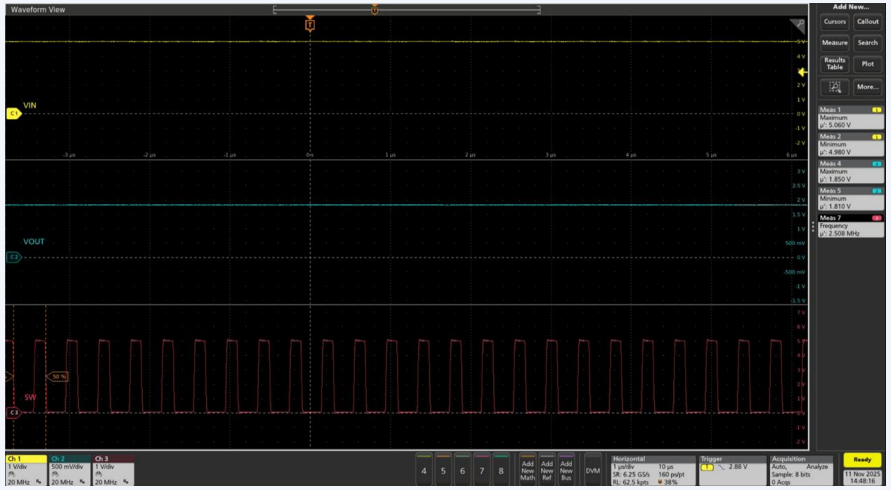
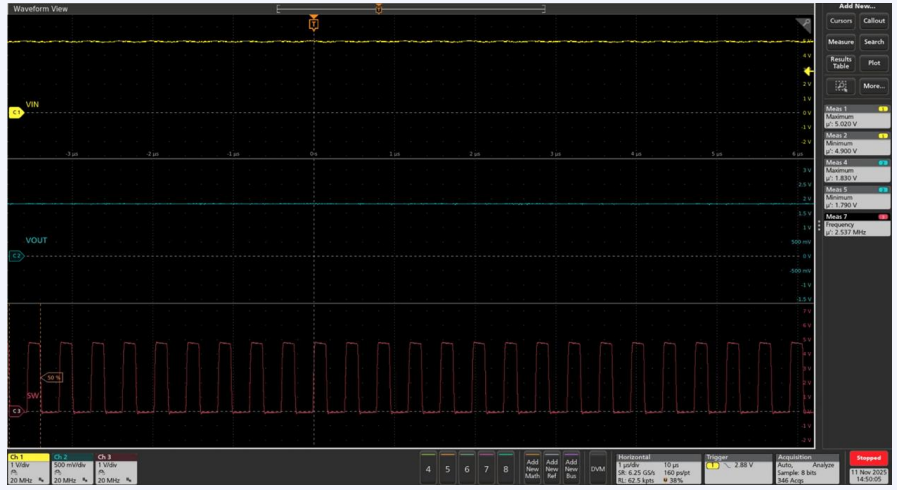
1V8 (Digital) Ripple – 1.8Vout

0A



3A



- Steady state ripple 6mVp-p

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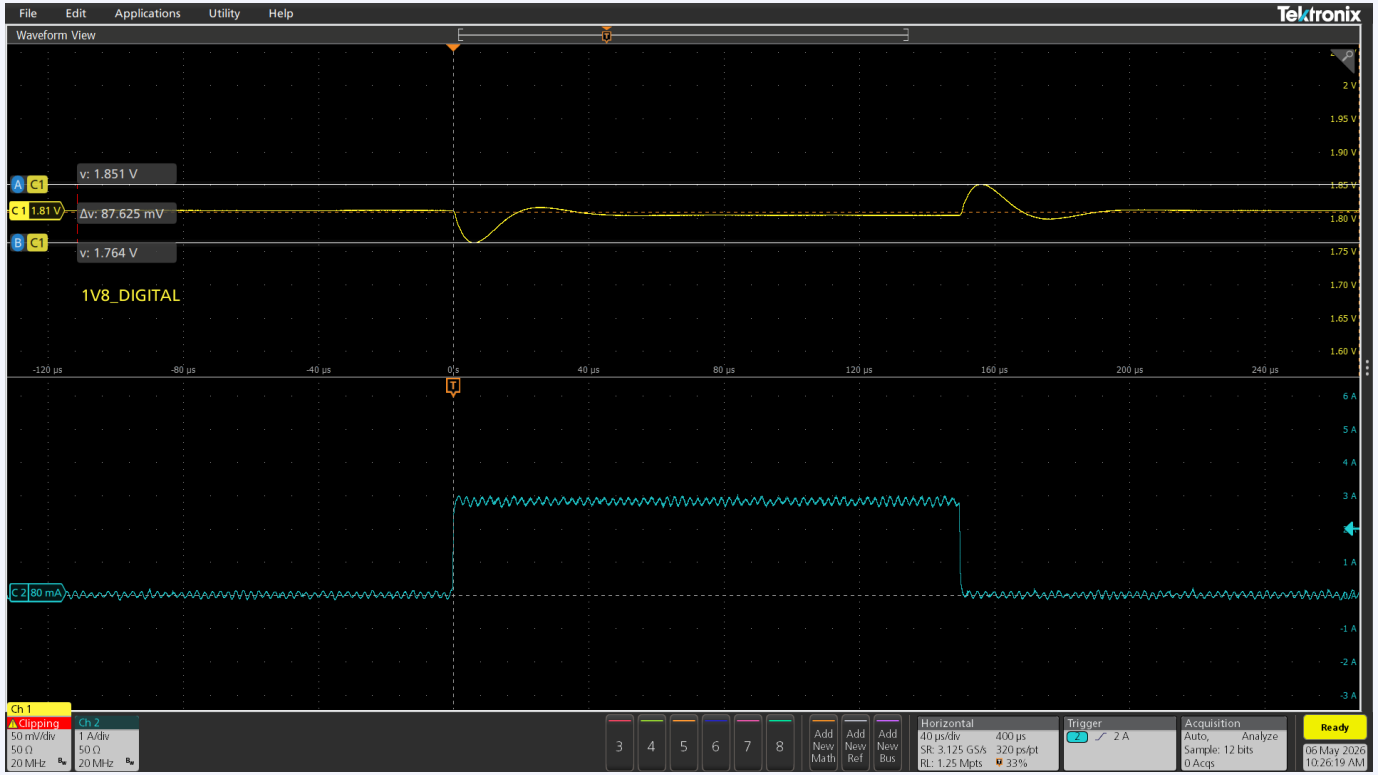
1V8 (Digital) Transient – 1.8Vout

0A → 3A → 0A



- Vout ripple -2.54% (-46mV) to +2.27% (41mV) with load transient

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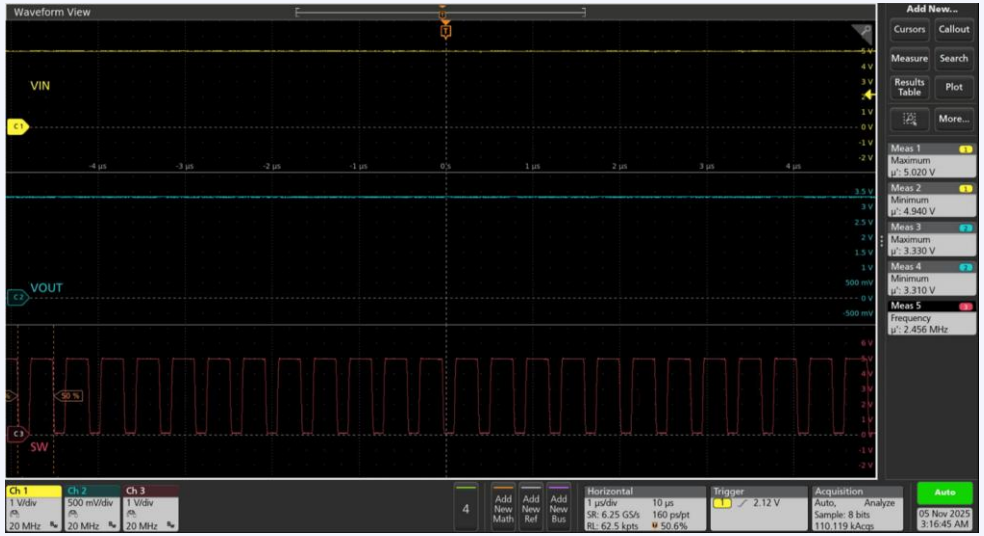
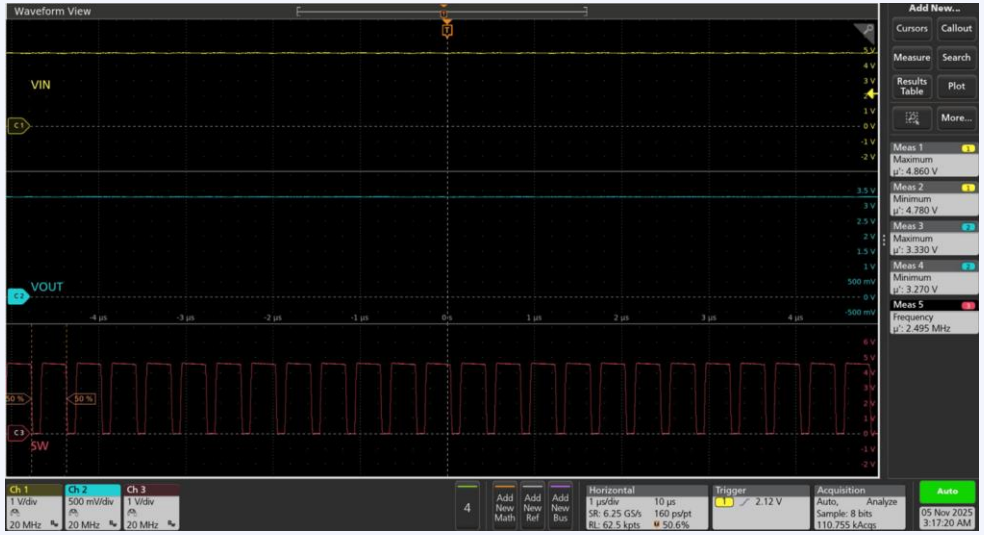
3V3 (Digital) Ripple – 3.3Vout

0A



3A



- Steady state ripple 5.2mVp-p

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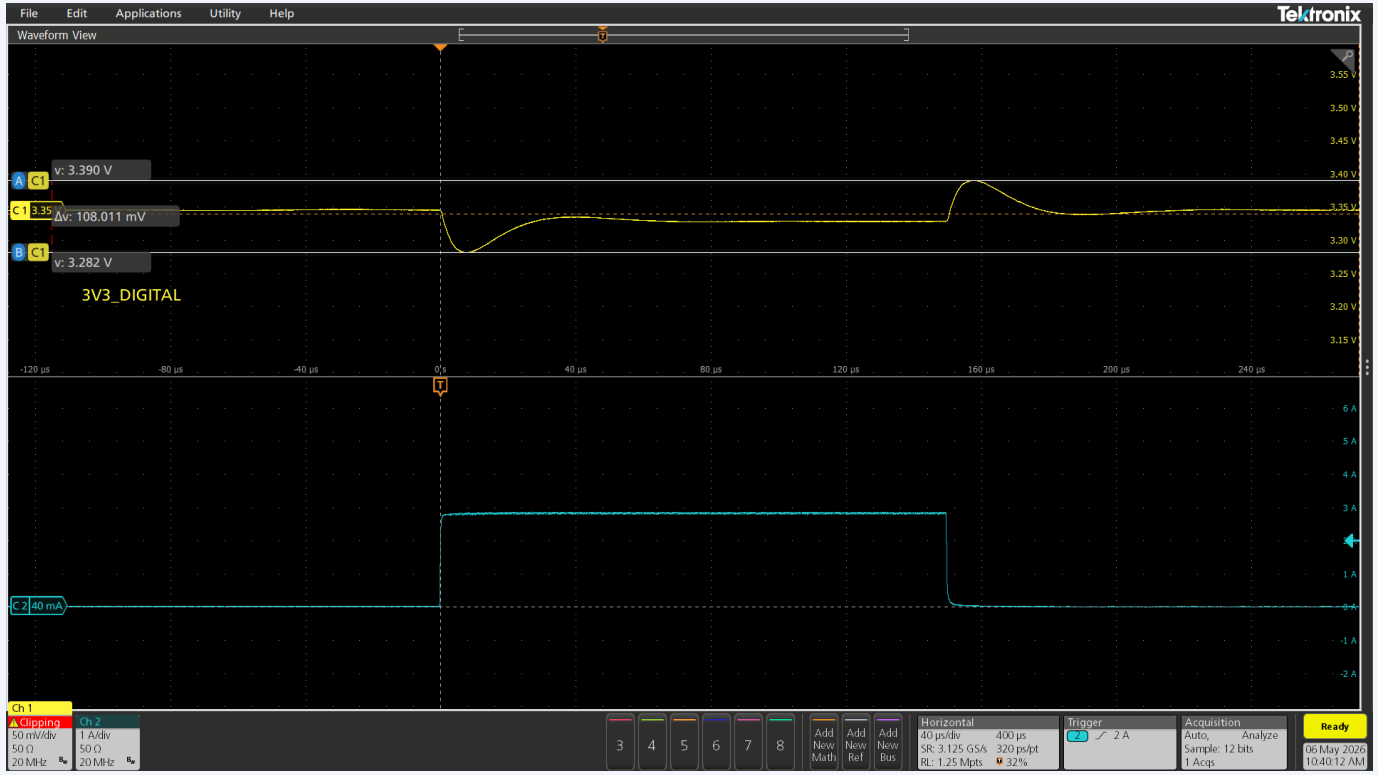
3V3 (Digital) Transient – 3.3Vout

0A → 3A → 0A



- Vout ripple -2.03% (-68mV) to +1.19% (40mV) with load transient

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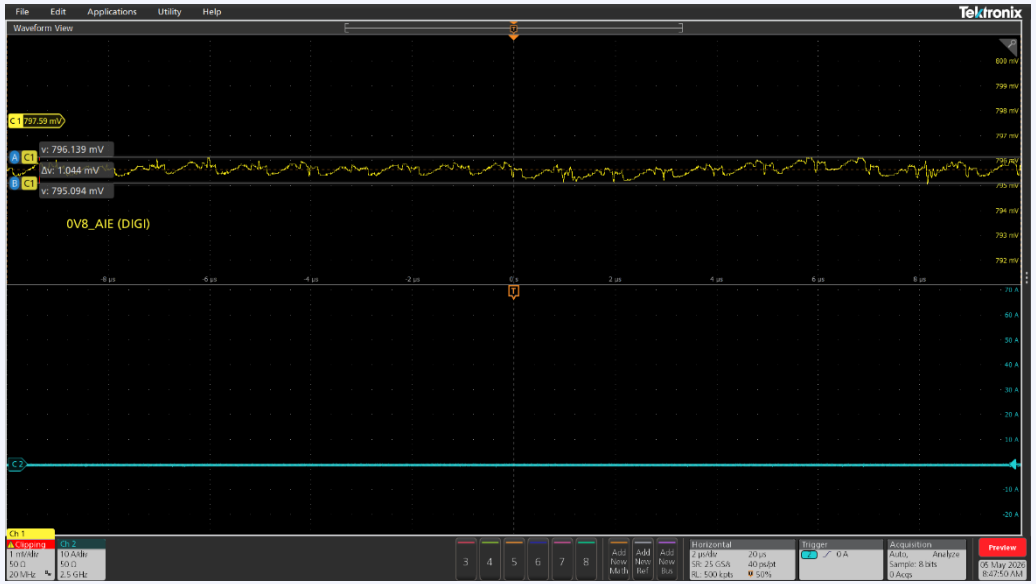
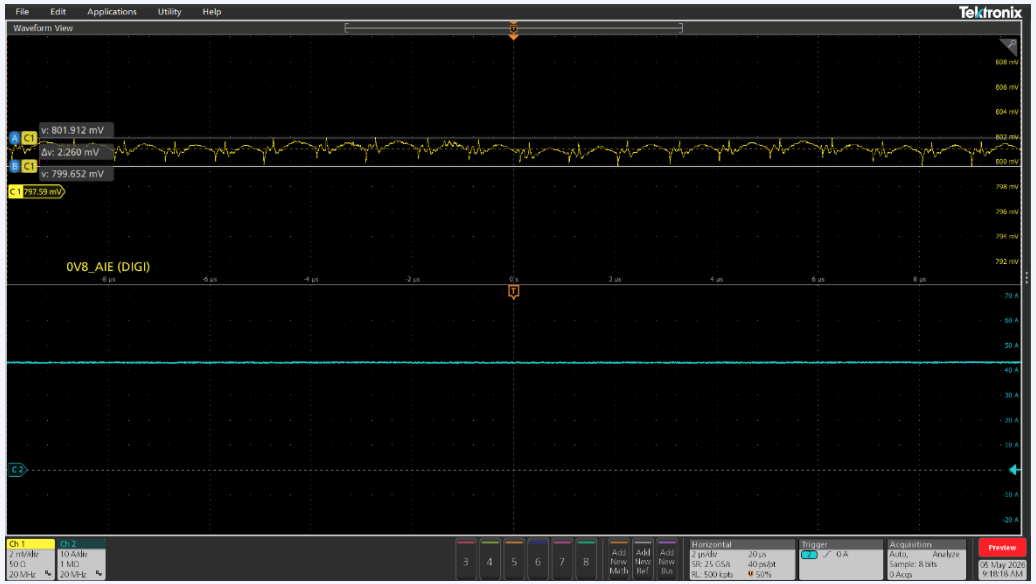
0V8_AIE (Digital) Ripple – 0.8Vout

0A



43A



- Steady state ripple 1.04mVp-p at 0A
- Steady state ripple 2.26mVp-p at 43A

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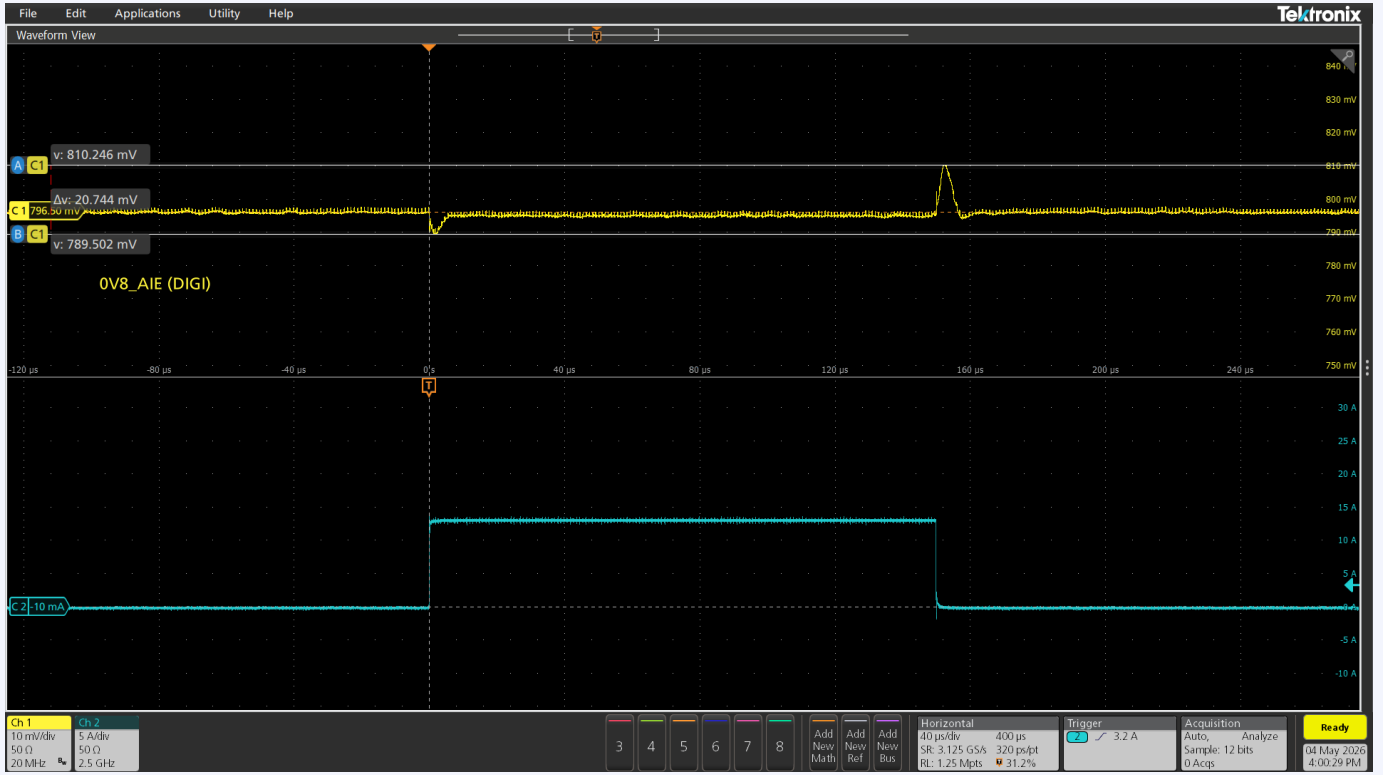
0V8_AIE (Digital) Transient – 0.8Vout

0A → 14A → 0A



- Vout ripple -0.87% (6.998mV) to +1.73% (13.746mV) with load transient

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Power On/Off Sequence

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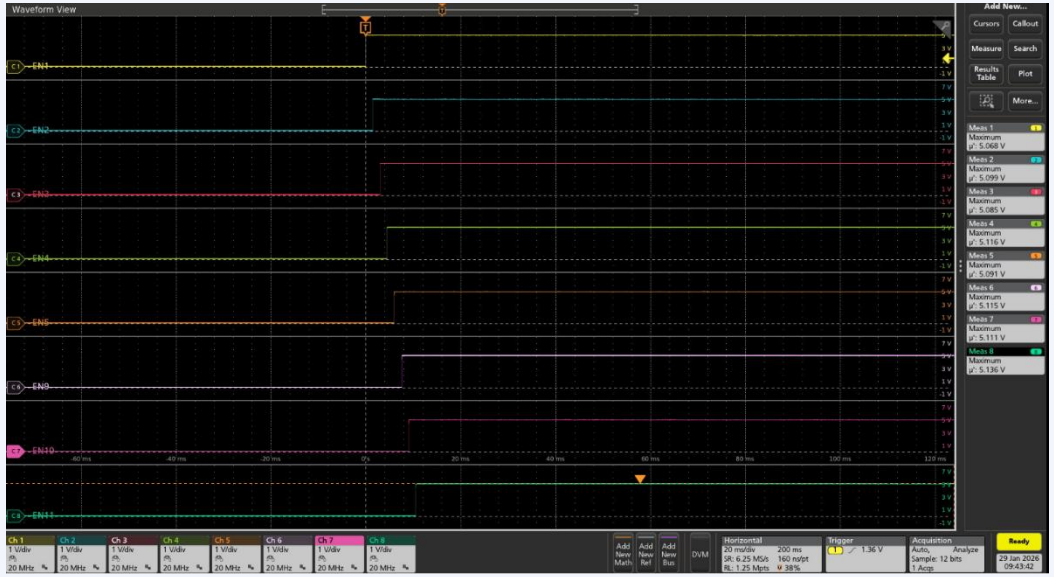
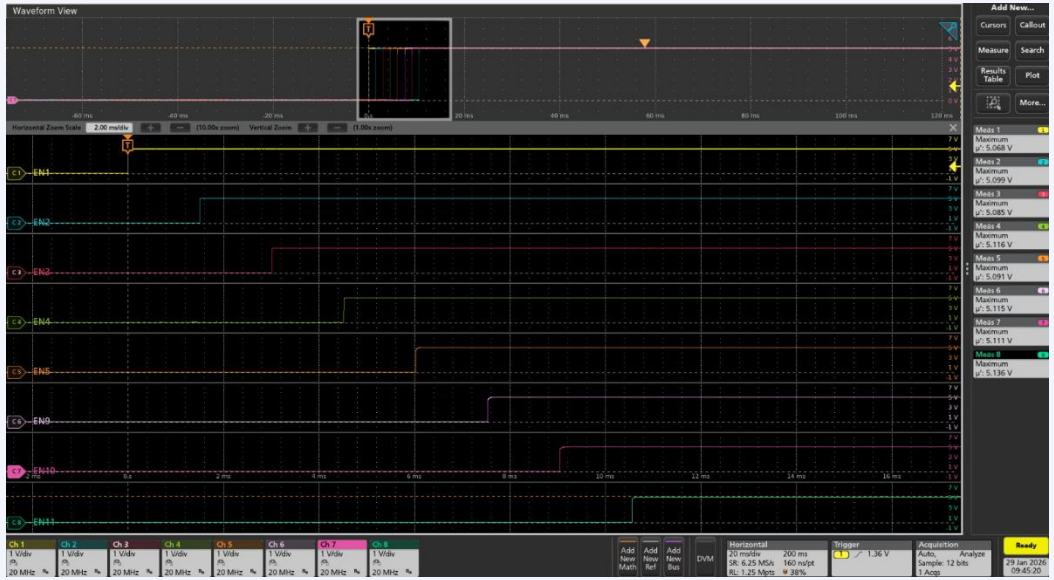
Power ON sequence





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Power OFF sequence

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