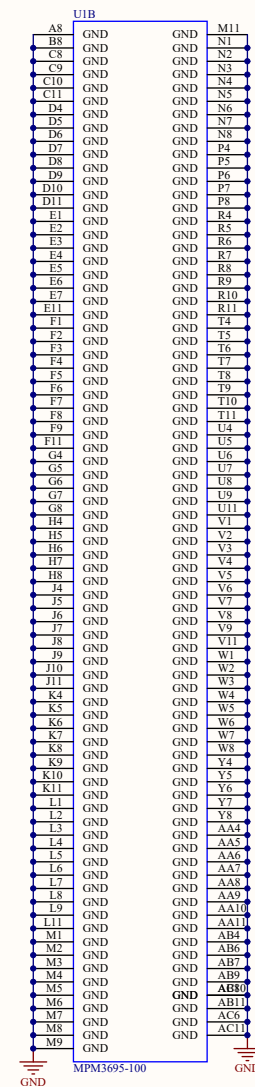
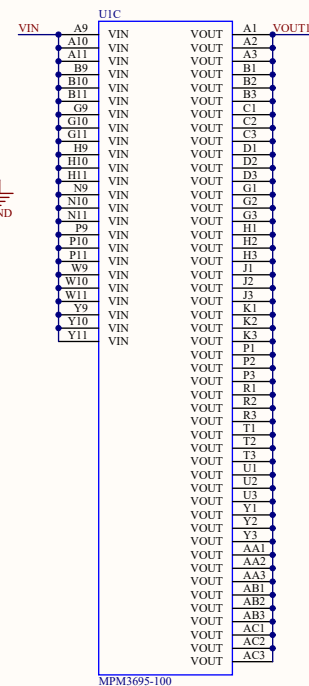
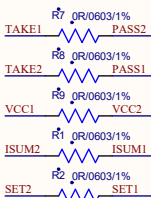
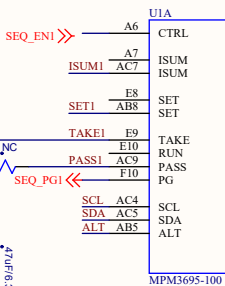



Rail1: 0.7-0.88V@100-200A

Default output: 0.8V@200A

U1: MASTER
U2: SLAVE

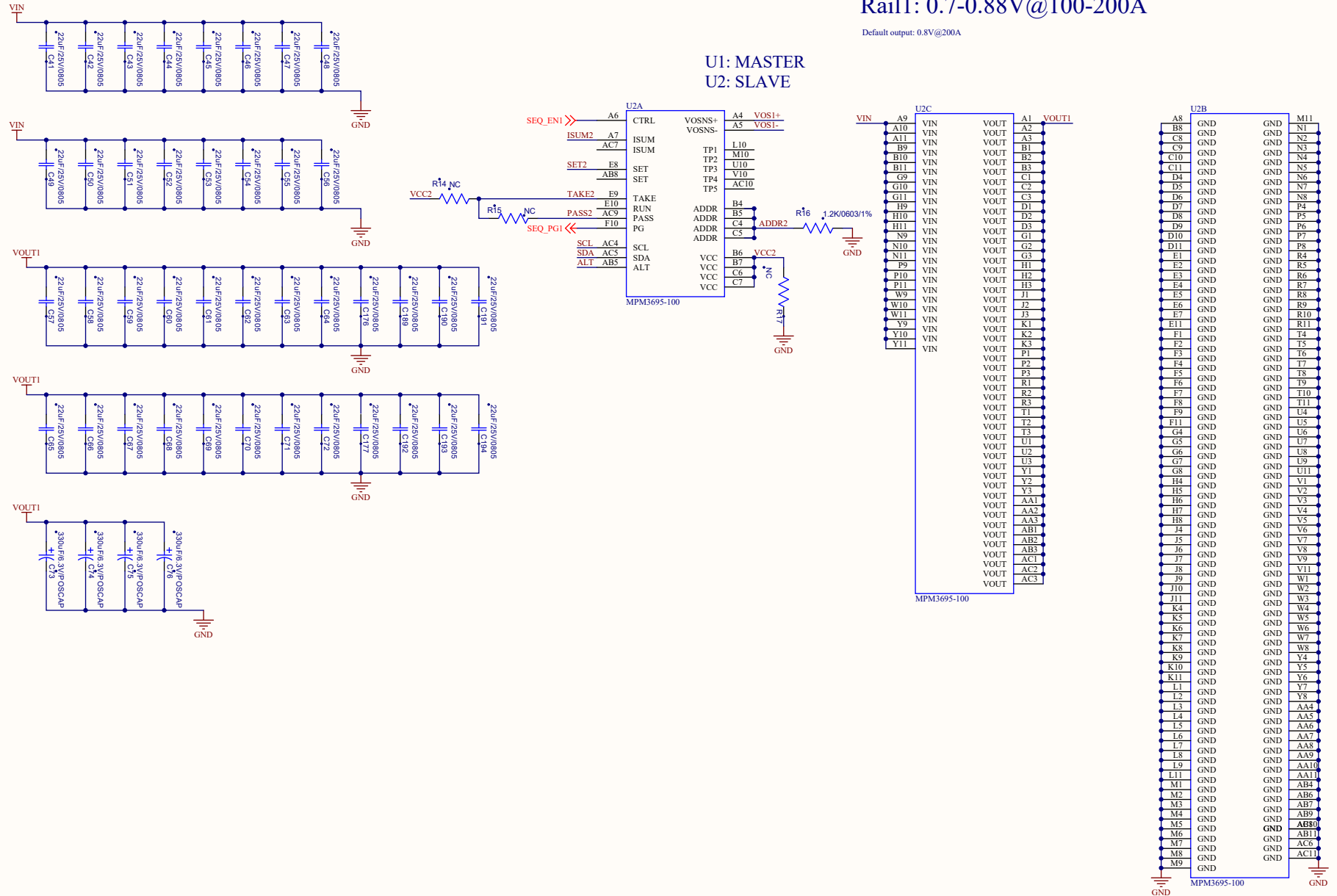


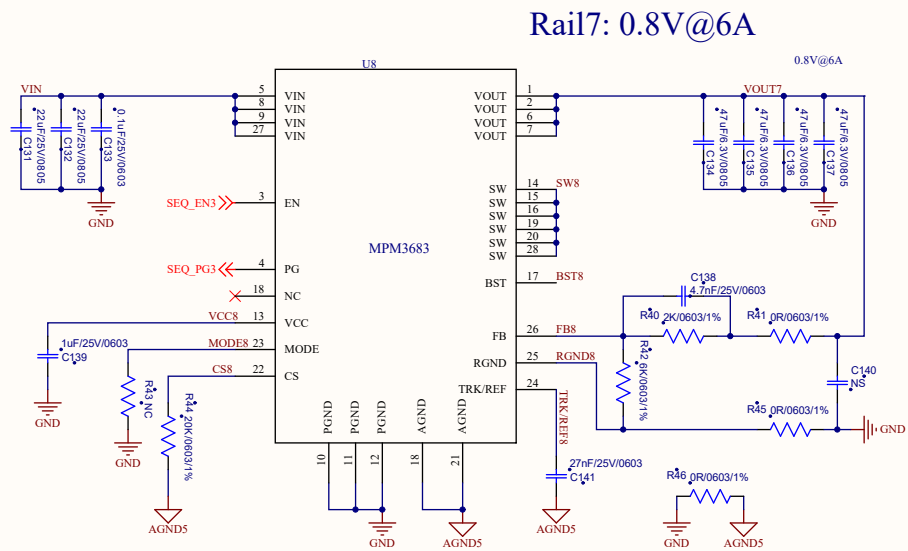
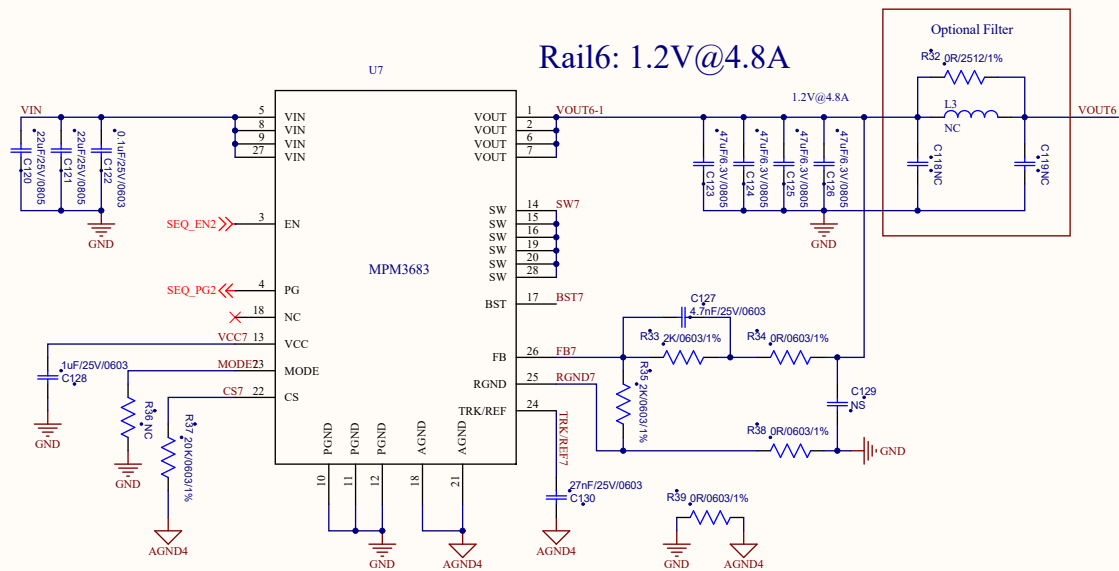
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Size: A3	Engineer: Ryan Zhang	Revision: R1.0	
Date: 9/1/2020	Drawer: Ryan Zhang	Sheet: 2 of 7	
File: \\cd-rw\home\Groups\AE\Product\EVXLVA_02\02_Rail1_1.SchDoc			

Rail1: 0.7-0.88V@100-200A

Default output: 0.8V@200A

U1: MASTER
U2: SLAVE



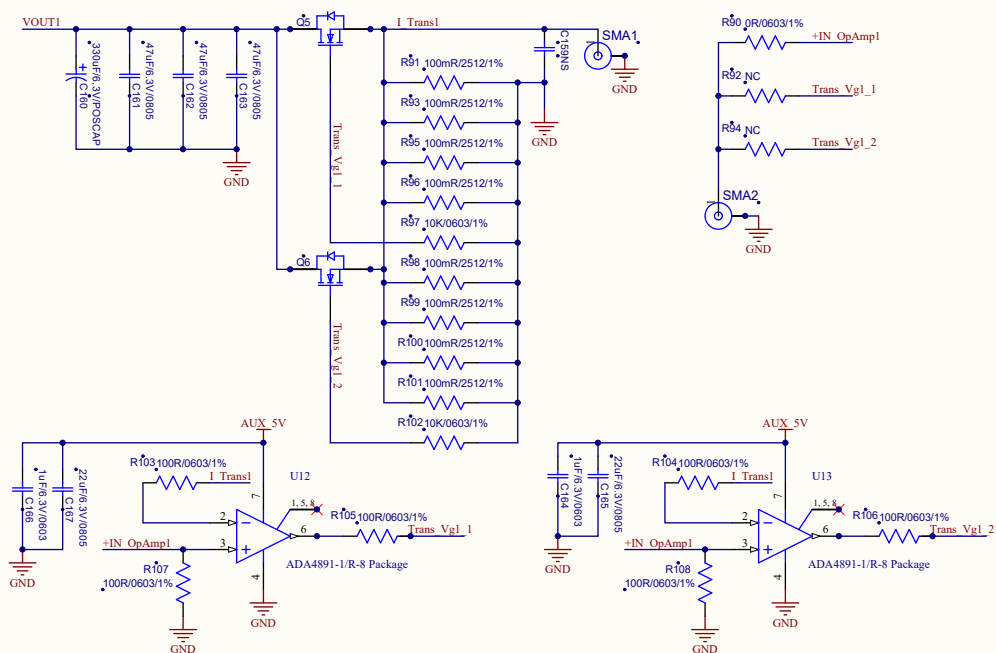


Title:	Versal_Reference_Design_High_Current		
Size:	A3	Engineer: Ryan Zhang	Revision: R1.0
Date:	9/1/2020	Drawer: Ryan Zhang	Sheet: 5 of 7
File:	\\cd-rw-home\Groups\AE\Product\EXL\VA_02\05_Rail6-7_SchDoc		



Transient Circuit for Rail1

For test only



Transient Circuit for Rail2,3,4,5,6,7 For test only

