

Introduction

Due to their versatility, ease of design, and low cost, flyback converters have become one of the most widely used topologies in power electronics. Its structure derives from one of the three basic topologies — specifically, buck-boost topology. However, unlike buck-boost converters, flyback topologies allow the voltage output to be electrically isolated from the input power supply. This feature is vital for industrial and consumer applications.

Among the different control methods used to stabilize power converters, the most widely used control method is peak current mode, which continuously senses the primary current to provide important protection for the power supply. Additionally, to obtain a higher design performance, it is common to regulate the converter with the output that has the highest load using a technique called cross-regulation.

This article aims to show readers, engineers, and students how to correctly design the control loop that stabilizes the flyback converter in order to provide optimal functionality. This process includes minimizing the stationary error, increasing/decreasing the bandwidth as required, and increasing the phase/gain margin as much as possible.

Closed-Loop Flyback Converter Block Diagram

Before making the necessary calculations for the controller to stabilize the peak current control mode flyback, it is important to understand the components of the entire closed-loop system: the converter averaged model and the control loop (see Figure 1).

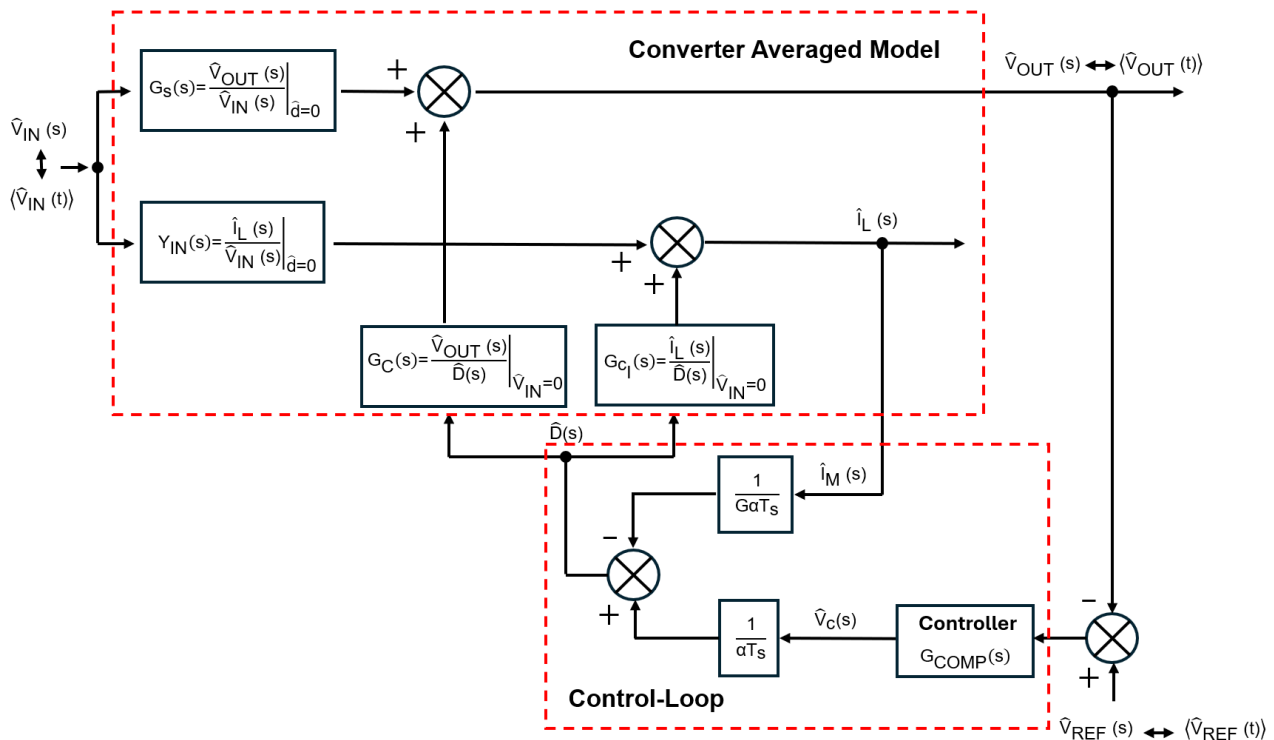


Figure 1: Closed-Loop System Block Diagram

The design engineer's main interest is to study the behavior of the converter under load changes. Considering a fixed input voltage (V_{IN}), the open-loop transfer function can be modeled under small perturbations produced in the duty cycle to study the power supply's dynamic response.

The summarized open-loop system can be modeled with Equation (1):

$$T_{V0}(s) = \left. \frac{V_{OUT}(s)}{V_C(s)} \right|_{V_{IN}=0} = \frac{G \times G_C(s)}{G_{CI}(s) + G \alpha T_s} \tag{1}$$

Where G is the current-sense gain transformed to voltage, $G_C(s)$ and $G_{CI}(s)$ are the transfer functions of the flyback converter in terms of output voltage and magnetizing current response (respectively) under small perturbations in the duty cycle, and $G \alpha T_s$ is the modelling of the ramp compensation to avoid the double-pole oscillation at half of the switching frequency.

Flyback Converter Control Design and Component Selection

There are many decisions and tradeoffs involved in designing the flyback converter’s control loop. The following sections of the article will explain the design process step by step.

Figure 2 shows the design flow.

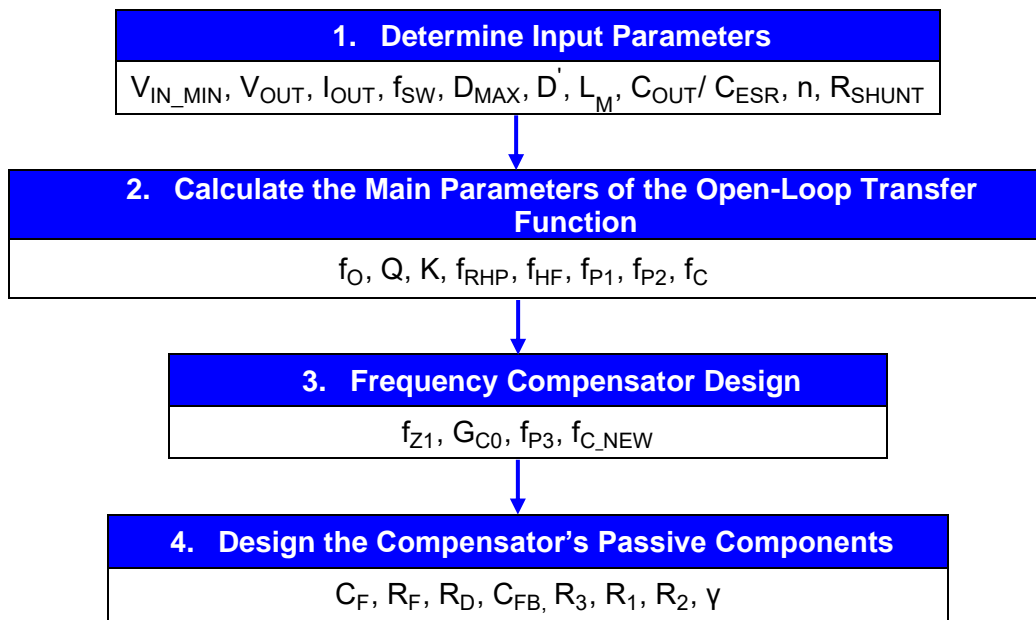


Figure 2: Control Loop Design Flowchart

Control Loop Design Process and Calculations

Step 1: Design Inputs

Once the converter’s main parameters have been designed according to the relevant specifications, it is time to define the parameters as inputs for the control loop design. These parameters include the input and output voltages (V_{IN} and V_{OUT} , respectively), operation mode, switching frequency (f_{SW}), duty cycle, magnetizing inductance (L_M), turns ratio ($N_P:N_S$), shunt resistor (R_{SHUNT}), and output capacitance (C_{OUT}). Table 1 shows a summary of the design inputs for the circuit discussed in this article.

Table 1: Summary of Design Inputs

Design Input	Value
Minimum input voltage (V _{IN_MIN})	85V _{AC}
Output voltage (V _{OUT})	12V
Output current (I _{OUT})	3.33A
Operation mode	CCM at V _{IN_MIN}
Switching frequency (f _{sw})	65kHz
Maximum duty cycle (D _{MAX})	46%
Secondary duty cycle (D')	54%
Magnetizing inductance (L _M)	610μH
Output capacitance/ESR (C _{OUT} /C _{ESR})	950μF/15mΩ
Turns ratio N _S :N _P (n)	1/6
Shunt resistor (R _{SHUNT})	0.4Ω

To design a flyback converter compensator, it is necessary to first obtain all main components that make the converter. For this article, MPS's [HF500-40](#) flyback regulator will be used to demonstrate that designing a compensator using optocoupler feedback is not a complex process. This device is a fixed-frequency, current-mode regulator with built-in slope compensation. Because the converter works in continuous conduction mode (CCM) at low line input, a double-pole oscillation at half of the switching frequency is produced; built-in slope compensation dampens this oscillation, making its effect almost null.

Step 2: Calculate the Parameters of the Open-Loop Transfer Function

It is vital to calculate the parameters of the open-loop transfer function and calculate the values for all of the compensator's parameters that can optimize the converter at the dynamic behavior level.

The open-loop transfer function of the peak current control flyback converter (also including the compensation ramp factor) can be estimated with Equation (2):

$$\frac{\hat{V}_{OUT}(s)}{\hat{V}_C(s)} \Big|_{\hat{V}_{IN}=0} = \frac{2xGxV_{IN}xD'R}{\frac{D'xV_{OUT}xT_sxR}{n^2xL_M} + 2xn xV_{IN}x(1+D')} \times \frac{\left(1 - \frac{L_MxDn^2}{D'xR}xs\right)x(1+C_{OUT}xR_{ESR}xs)}{\left(\frac{RxV_{OUT}xD'T_sxC_{OUT}}{n^2xL_M}xs^2 + \frac{V_{OUT}xD'T_s+2xnxC_{OUT}xRxV_{IN}xs+1}{\frac{D'xV_{OUT}xT_sxR}{n^2xL_M} + 2xn xV_{IN}x(1+D')}}\right)} \quad (2)$$

Where D' is defined by the percentage of time that the secondary diode (or synchronous FET) is active during a switching cycle.

The basic canonical model can be defined with Equation (3):

$$\frac{\hat{V}_{OUT}(s)}{\hat{V}_C(s)} \Big|_{\hat{V}_{IN}=0} = G_{C0} \times \frac{\left(1 - \frac{s}{\omega_{RHP}}\right)x\left(1 + \frac{s}{\omega_{HF}}\right)}{\left(\left(\frac{s}{\omega_o}\right)^2 + \frac{s}{\omega_o xQ} + 1\right)} \quad (3)$$

Note that the equivalent series resistance (ESR) effect on the output capacitors has been included in the transfer function, as it is the most significant parasitic effect.

By using Equation (2) and Equation (3), it is possible to calculate the vital parameters.

The resonant frequency (f_0) can be calculated with Equation (4):

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi} \times \sqrt{\frac{D^3 \times V_{OUT} \times T_s \times R}{n^2 \times L_M} + 2 \times n \times V_{IN} \times (1+D)}{\frac{R \times V_{OUT} \times D \times T_s \times C_{OUT}}{}} \quad (4)$$

After inputting the relevant values, f_0 can be calculated with Equation (5):

$$f_0 = \frac{1}{2\pi} \times \sqrt{\frac{\frac{(0.54)^3 \times 12 \times \frac{12}{3.33}}{n^2 \times L_M} + 2 \times \frac{1}{6} \times 85 \times \sqrt{2} \times (1+0.46)}{\frac{12}{3.33} \times 12 \times (0.54) \times \frac{1}{65 \times 10^3} \times 950 \times 10^{-6}}} = 2.191 \text{kHz} \quad (5)$$

The right-half-plane zero (f_{RHP}) can be estimated with Equation (6):

$$f_{RHP} = \frac{D^2 \times R}{2 \times \pi \times n^2 \times L_M \times D} = \frac{(0.54)^2 \times \frac{12}{3.33}}{2 \times \pi \times (\frac{1}{6})^2 \times 610 \times 10^{-6} \times 0.46} = 21.46 \text{kHz} \quad (6)$$

The q-factor (Q) can be calculated with Equation (7):

$$Q = \frac{\sqrt{\frac{D^3 \times V_{OUT} \times T_s \times R}{n^2 \times L_M} + 2 \times n \times V_{IN} \times (1+D)} \times \sqrt{\frac{R \times V_{OUT} \times D \times T_s \times C_{OUT}}{}}}{V_{OUT} \times D \times T_s + 2 \times n \times C_{OUT} \times R \times V_{IN}} \quad (7)$$

After inputting the relevant values, Q can be estimated with Equation (8):

$$Q = \frac{\sqrt{\frac{(0.54)^3 \times 12 \times \frac{12}{3.33}}{n^2 \times L_M} + 2 \times \frac{1}{6} \times 85 \times \sqrt{2} \times (1+0.46)} \times \sqrt{\frac{12}{3.33} \times 12 \times (0.54) \times \frac{1}{65 \times 10^3} \times 950 \times 10^{-6}}}{12 \times (0.54) \times \frac{1}{65 \times 10^3} + 2 \times \frac{1}{6} \times 85 \times \sqrt{2} \times \frac{12}{3.33} \times 85 \times \sqrt{2}} = 0.034 \quad (8)$$

The DC gain (K) can be calculated with Equation (9):

$$K = \frac{2 \times G \times V_{IN} \times D \times R}{\frac{D^3 \times V_{OUT} \times T_s \times R}{n^2 \times L_M} + 2 \times n \times V_{IN} \times (1+D)} \quad \text{where } G = \frac{1}{R_{SHUNT}} \quad (9)$$

After inputting the relevant values, K can be estimated with Equation (10):

$$K = \frac{2 \times \frac{1}{0.4} \times 85 \times \sqrt{2} \times (0.54) \times \frac{12}{3.33}}{\frac{(0.54)^3 \times 12 \times \frac{12}{3.33}}{n^2 \times L_M} + 2 \times \frac{1}{6} \times 85 \times \sqrt{2} \times (1+0.46)} = 18.08 = 25.14 \text{dB} \quad (10)$$

The high-frequency zero (f_{HF}) can be calculated with Equation (11):

$$f_{HF} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{ESR}} = \frac{1}{2 \times \pi \times 950 \times 10^{-6} \times 15 \times 10^{-3}} = 16.75 \text{kHz} \quad (11)$$

It is important to note that with current mode control, it is common to obtain values well below 0.5 for Q . With this in mind, the result of the second-degree polynomial in the denominator of the transfer function ends up giving two real and negative poles. This is different from voltage-control mode or when there is a very large compensation ramp, which results in two complex conjugate poles.

The two real and negative poles can be estimated with Equation (12):

$$f_{P1} = Q \times f_0 = 0.034 \times 2191 = 74.5 \text{Hz} \quad \text{and} \quad f_{P2} = \frac{f_0}{Q} = \frac{2191}{0.034} = 64.44 \text{kHz} \quad (12)$$

The new open-loop transfer function can be calculated with Equation (13):

$$\left. \frac{V_O(s)}{V_C(s)} \right|_{V_g=0} = K \times \frac{\left(1 + \frac{s}{\omega_{RHP}}\right) \times \left(1 + \frac{s}{\omega_{HF}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \times \left(1 + \frac{s}{\omega_{p2}}\right)} = 25.14 \times \frac{\left(1 + \frac{s}{2\pi \times 21.46 \times 10^3}\right) \times \left(1 + \frac{s}{2\pi \times 16.75 \times 10^3}\right)}{\left(1 + \frac{s}{2\pi \times 74.5}\right) \times \left(1 + \frac{s}{2\pi \times 64.44 \times 10^3}\right)} \quad (13)$$

The cutoff frequency (f_c) can be estimated with Equation (14):

$$f_c = f_{p1} \times K = 74.5 \times 18.08 = 1.35\text{kHz} \quad (14)$$

The following sections will explain how the frequency compensator design achieves power supply stability and excellent performance.

Step 3: Frequency Compensator Design

Once the open-loop transfer function is modelled, it is necessary to design the frequency compensator such that it achieves the best performance possible. Because the frequency response of the above transfer function has two separate poles (one at a low frequency and one at a high frequency), a simple Type II compensator can be designed. This compensator does not need an additional zero, which is not the case in voltage-control mode because there is a double pole that produces a resonance.

To minimize the steady-state error, it is necessary to design an inverted-zero (or a pole at the origin) because it produces higher gains at low frequencies. To ensure that the system's stability is not impacted, the frequency must be at least 10 times lower than the first pole, calculated with Equation (15):

$$f_{z1} \leq \frac{f_{p1}}{10} \rightarrow f_{z1} \leq \frac{74.5}{10} \rightarrow f_{z1} \leq 7.45\text{Hz} \quad (15)$$

Due to the ESR parasitic effect at high frequencies, it is necessary to design a high-frequency pole to compensate for and remove this effect. The pole can be estimated with Equation (16):

$$f_{p3} \approx f_{HF} \rightarrow f_{p3} \approx 16.75\text{kHz} \quad (16)$$

On the other hand, it is common to modify the cutoff frequency to achieve a higher or lower bandwidth and produce faster or slower dynamic responses, respectively. Once the cutoff frequency is selected (in this case, f_c is increased up to 6.5kHz, or 10% of f_{SW}), then the compensator's middle-frequency gain can be calculated with Equation (17):

$$G_{COMP} = \frac{f_{c, NEW}}{f_{p1}} \times \frac{1}{K} \times \frac{\sqrt{1 + \left(\frac{\omega_{z1}}{\omega_{c, new}}\right)^2}}{\sqrt{1 + \left(\frac{\omega_{c, new}}{\omega_{p3}}\right)^2}} = \frac{6.5 \times 10^3}{74.5} \times \frac{1}{18.08} \times \frac{\sqrt{1 + \left(\frac{2\pi \times 7.45}{2\pi \times 6.5 \times 10^3}\right)^2}}{\sqrt{1 + \left(\frac{2\pi \times 6.5 \times 10^3}{2\pi \times 16.75 \times 10^3}\right)^2}} = 4.5 = 13.06\text{dB} \quad (17)$$

Once the compensator has been designed within the frequency range, calculate the values of the passive components.

Step 4: Design the Compensator's Passive Components

The most common Type II compensator used for stabilization in current control mode flyback converters with cross-regulation is made up of an optocoupler feedback (see Figure 3).

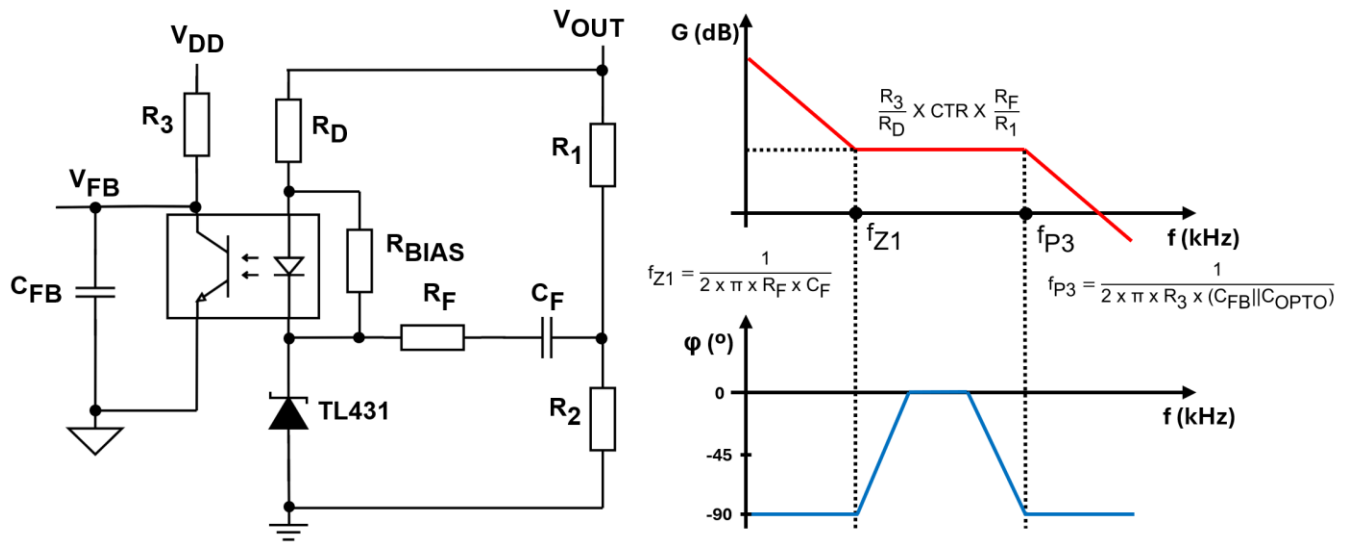


Figure 3: Type-II Compensator Made Up with Optocoupler Feedback

The compensator transfer function based on optocoupler feedback can be estimated with Equation (18):

$$G_{COMP}(s) = -\frac{R_3}{R_D} \times CTR \times \frac{R_F}{R_1} \times \frac{(1 + R_F \times C_F \times s)}{s \times (R_3 \times (C_{FB} \parallel C_{OPTO}) \times s + 1)} \quad (18)$$

The middle-frequency gain is formed by two stages: the optocoupler gain and the adjustable voltage reference compensator gain, calculated with Equation (19):

$$\|G_{COMP}\| = \frac{R_3}{R_D} \times CTR \times \frac{R_F}{R_1} \quad (19)$$

It is important to calculate the maximum resistance to correctly bias the optocoupler. This resistance can be estimated with Equation (20):

$$R_D \leq \frac{(V_{OUT} - V_F - V_{DZ1,MIN}) \times R_3 \times CTR_{MIN}}{V_{DD} - V_{CE,SAT} + CTR_{MIN} \times R_3 \times I_{BIAS}} \quad (20)$$

The parameters necessary to calculate R_D can be found in the optocoupler and the adjustable voltage reference datasheets. Table 2 shows the typical values for these parameters from the optocoupler.

Table 2: Main Optocoupler Parameters

Input Parameters	Value
Forward voltage (V_F)	1V
Bias current (I_{BIAS})	1mA
Optocoupler minimum current transfer ratio (CTR_{MIN})	0.3
Optocoupler nominal current transfer ratio (CTR)	1
Collector-emitter saturation voltage ($V_{CE,SAT}$)	0.2V
Optocoupler output capacitance (C_{OPTO})	200pF

Table 3 shows the typical values for these parameters from the adjustable voltage reference.

Table 3: Adjustable Voltage Reference Parameters

Input Parameters	Value
Minimum reference voltage (V_{DZ1_MIN})	2.495V
Feedback resistor (R_1)	100k Ω
Feedback resistor (R_2)	26.3k Ω
Maximum V_{FB}	3.9V

Once the above parameters have been obtained, R_D can be calculated with Equation (21):

$$R_D \leq \frac{(V_{OUT} - V_F - V_{DZ1_MIN}) \times R_3 \times CTR_{MIN}}{V_{DD} - V_{CE_SAT} + CTR_{MIN} \times R_3 \times I_{BIAS}} \leq \frac{(12 - 1 - 2.495) \times 12 \times 10^3 \times 0.3}{3.9 - 0.2 + 0.3 \times 12 \times 10^3 \times 1 \times 10^{-3}} \leq 4.2k\Omega \quad (21)$$

Once the value of R_3 is obtained (in this case, R_3 is internal to the HF500-40 controller, with a minimum value of 12k Ω), as well as the values for R_1 , R_2 , and R_D (where $R_D = 2k\Omega$), then R_F can be estimated with Equation (22):

$$R_F = \frac{G_{COMP}}{\frac{R_3 \times CTR_{NOM}}{R_D}} \times R_1 = \frac{4.5}{\frac{12 \times 10^3}{2 \times 10^3} \times 1} \times 100 \times 10^3 = 75k\Omega \quad (22)$$

Where G_{COMP} is the compensator's middle frequency gain, calculated with Equation (17). G_{COMP} is used to adjust the power supply's bandwidth.

Because the inverted zero and high-frequency pole were already calculated, C_F and C_{FB} can be calculated with Equation (23) and Equation (24), respectively:

$$f_{z1} = \frac{1}{2\pi \times R_F \times C_F} \rightarrow C_F = \frac{1}{2\pi \times R_F \times f_{z1}} = \frac{1}{2\pi \times 75 \times 10^3 \times 7.45} = 285nF \quad (23)$$

$$f_{p3} = \frac{1}{2\pi \times R_3 \times (C_{FB} \parallel C_{OPTO})} \rightarrow C_{FB} = \frac{1}{2\pi \times f_{p3} \times R_3} - C_{OPTO} = \frac{1}{2\pi \times 16.75 \times 10^3 \times 12 \times 10^3} - 200 \times 10^{-12} = 592pF \quad (24)$$

Once the open-loop system and compensator have been designed, the loop gain transfer function can be estimated with Equation (25):

$$G_{TOTAL}(s) = 38.2 \times \frac{\left(1 + \frac{s}{2\pi \times 21.46 \times 10^3}\right) \times \left(1 + \frac{s}{2\pi \times 16.75 \times 10^3}\right)}{\left(1 + \frac{s}{2\pi \times 74.5}\right) \times \left(1 + \frac{s}{2\pi \times 64.44 \times 10^3}\right)} \times \frac{\left(1 + \frac{s}{2\pi \times 7.45}\right)}{s \times \left(\frac{s}{2\pi \times 16.75 \times 10^3} + 1\right)} \quad (25)$$

Equation (25) is based on Equation (13) and Equation (18).

It is important to calculate the phase and gain margins to ensure the stability of the power supply.

The phase margin can be calculated with Equation (26):

$$\gamma = 180^\circ - \tan^{-1}\left(\frac{\omega_{C_NEW}}{\omega_{RHP}}\right) - \tan^{-1}\left(\frac{\omega_{z1}}{\omega_{C_NEW}}\right) + \tan^{-1}\left(\frac{\omega_{C_NEW}}{\omega_{HF}}\right) - \tan^{-1}\left(\frac{\omega_{C_NEW}}{\omega_{p1}}\right) - \tan^{-1}\left(\frac{\omega_{C_NEW}}{\omega_{p2}}\right) - \tan^{-1}\left(\frac{\omega_{C_NEW}}{\omega_{p3}}\right) \quad (26)$$

After inputting the relevant values, the phase margin can be calculated with Equation (27):

$$\gamma = 180^\circ - \tan^{-1}\left(\frac{6.5 \times 10^3}{21.46 \times 10^3}\right) - \tan^{-1}\left(\frac{7.45}{6.5 \times 10^3}\right) + \tan^{-1}\left(\frac{6.5 \times 10^3}{16.75 \times 10^3}\right) - \tan^{-1}\left(\frac{6.5 \times 10^3}{74.5}\right) - \tan^{-1}\left(\frac{6.5 \times 10^3}{66.44 \times 10^3}\right) - \tan^{-1}\left(\frac{6.5 \times 10^3}{16.75 \times 10^3}\right) = 68^\circ \quad (27)$$

If the phase margin exceeds 50°, it is an important parameter necessary to comply with certain standards.

At the same time, the gain margin can be approximated with Equation (28):

$$\begin{aligned} \gamma &= 180^\circ - \tan^{-1}\left(\frac{\omega}{21.46 \times 10^3}\right) - \tan^{-1}\left(\frac{7.45}{\omega}\right) + \tan^{-1}\left(\frac{\omega}{16.75 \times 10^3}\right) - \tan^{-1}\left(\frac{\omega}{74.5}\right) - \\ &\tan^{-1}\left(\frac{\omega}{66.44 \times 10^3}\right) - \tan^{-1}\left(\frac{\omega}{16.75 \times 10^3}\right) = 0^\circ \rightarrow \omega = 37.84kHz \end{aligned} \quad (28)$$

Equation (29) is derived from Equation (25) at the specified frequency:

$$\|G_{TOTAL}(s)\| = 10^{\frac{38.2}{20}} \times \frac{\sqrt{1 + \left(\frac{2\pi \times 37.84 \times 10^3}{2\pi \times 21.46 \times 10^3}\right)^2} \times \sqrt{1 + \left(\frac{2\pi \times 37.84 \times 10^3}{2\pi \times 16.75 \times 10^3}\right)^2} \times \sqrt{1 + \left(\frac{2\pi \times 7.5}{2\pi \times 37.84 \times 10^3}\right)^2}}{\sqrt{1 + \left(\frac{2\pi \times 37.84 \times 10^3}{2\pi \times 74.5}\right)^2} \times \sqrt{1 + \left(\frac{2\pi \times 37.84 \times 10^3}{2\pi \times 66.44 \times 10^3}\right)^2} \times \sqrt{1 + \left(\frac{2\pi \times 37.84 \times 10^3}{2\pi \times 16.75 \times 10^3}\right)^2}}$$

$$\|G_{TOTAL}(s)\| = 0.282 \rightarrow \|G_{TOTAL}(s)\|_{dB} = -11dB \tag{29}$$

In this scenario, the gain margin is below -10dB, which is another important parameter to consider, particularly in regards to compliance with regulation specifications. If the result is close to 0dB, some iteration is necessary to decrease the value; otherwise, the performance is suboptimal. This iteration must start by decreasing the value of the cutoff frequency.

This complete transfer function provides stability to the power supply and the best performance as possible by:

- Minimizing steady-state error.
- Minimizing the ESR parasitic effect.
- Increasing the bandwidth of the power supply up to 6.5kHz.

Final Design

After calculating all of the passive component values for the feedback loop compensator and determining the converter’s main parameters, the entire flyback can be designed using the HF500-40. Figure 4 shows the circuit’s final design using all calculated parameters.

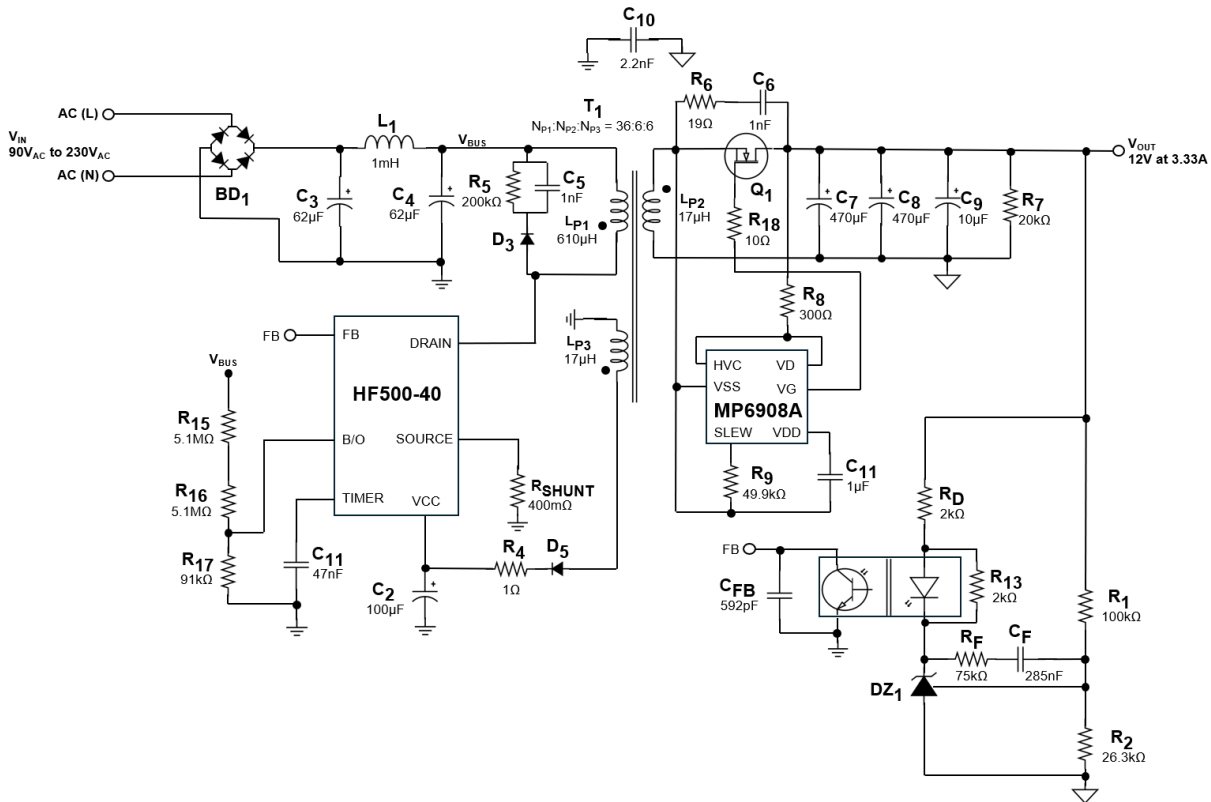


Figure 4: Final Design Circuit Schematic

Figure 5 shows the bode plot of the complete loop gain frequency response.

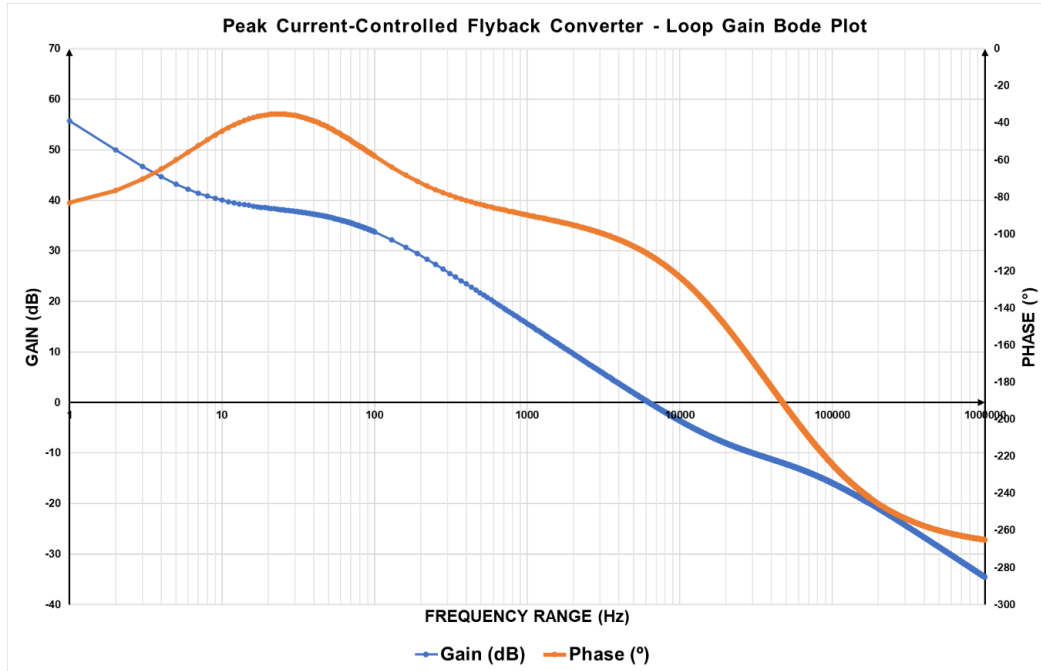


Figure 5: Bode Plot of the Complete Loop Gain Frequency Response

Conclusion

Obtaining the flyback averaged model via small-signal analysis is a complex process to most accurately approximation of the converter’s transfer functions. In addition, the cross-regulation technique involves secondary-side regulation through optocoupler feedback and an adjustable voltage reference, which complicates calculations.

However, by following the four steps explained in this article, a good approximation can be obtained to improve the power supply’s performance, as the output with the heaviest load is directly regulated. This means that the output can react quickly to load changes. Thus, designing an optocoupler feedback compensator using the [HF500-40](#) is not a complex process. Explore MPS’s [secondary-side regulation](#) solutions to optimize your flyback topology design.