



# Is Design Reuse a Myth for Analog Circuits?

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I have been invited to comment on electronic design automation (EDA). It is a subject in the industry to which I have not contributed much innovation, but I can say a few words as someone who has benefited from it during my long career as an analog designer.

With just over 25 years of experience designing DC/DC power converters as well as custom and standard analog IC products, I have seen some revolutionary changes in the EDA toolset over the years. I have worked for various companies and am currently with Monolithic Power Systems (MPS), so I have certainly seen diverse approaches to design methods.

From my perspective, the impetus behind the continued EDA development is its ever-improving design execution speed, in addition to its high confidence of success in the resulting silicon. Despite these improvements — including those in simulation engines, data visualization, and post-layout extraction of parasitic elements — it seems there is always another upgrade on the horizon. An old proverb comes to my mind: “Everything is going digital, but the world is still analog.” The analog here is engineers, so perhaps what is driving continuous EDA development is this human element.

A theme that dominates my work life is circuit reuse. It was even a subject in my interview before joining MPS: Why is it so difficult for those in the analog design community to reuse IP blocks? Caught off guard, I had no ready answer to describe the barriers to reuse; I was also hesitant to offer any definitive answer to the interviewer, as I knew nothing about the company’s internal systems for IP tracking. I have continued to give this question thought as I learn about the design processes and legacy circuits at MPS.

It is easy enough to answer that every experienced design engineer has their favorite bandgap (they do): some may prefer the use of MOSFETs, while a select few use bipolar. I have concluded that the answer is more fundamental, though, and these perennial struggles can be distilled to a few points: inadequate documentation leading to a poor understanding of function, and less than ideal discipline with design hierarchy. Good grief — it sounds like a situation one would find in software engineering.

That said, can EDA help in analog to facilitate the appropriate reuse of design blocks, and can it improve how engineers interact on a project so they finalize the design more quickly? Perhaps yes, but this is still a work in progress. I want to expand on six aspects of EDA tools that have helped me with reuse:

1. Macro-modeling blocks in a system facilitates understanding and team communication. I have previously used LTSpice™, and at my present job, I use Simplis™ because it provides periodic system stability analysis for the switch-mode converters I design. The resulting macro-model schematics are simple enough to understand and can run proof-of-concept simulations. These models can be shared with fellow team members to guide circuit design choices. After release, IC models can be sent to customers to simulate higher-level performance using an off-the-shelf simulation tool; this is a win-win-win situation using this type of EDA tool.
2. Good schematic documentation, such as adding notes directly on the schematic as well as presentations for each block, creates transparency that makes reviews quicker and leads to better reuse. For example, most simulators can effectively present DC operating points for the circuit, but this information would be even more useful if the design engineer interpreted the results, as they impact operating headroom, common-mode input/output ranges, gain/phase margins, and so on.
3. Hierarchical discipline is vital to maintaining clarity. I have seen bad examples that spread single functions, such as a comparator with blanking, across blocks separated by several levels of hierarchy. The appropriate use of hierarchy can simplify schematic appearance, which leads to better understanding, and it can facilitate the reuse of layout and functional sub-blocks and their layouts.

Engineers tend not to reuse something if its inner workings and timing interactions with external blocks are perceived to be “tweaky.”

4. The compatibility of symbols and device modeling between technologies facilitates migration and reuse. It is so painful to recreate schematics when the device pins change location that this effort is considered to be a fresh start from a scheduling perspective. A fresh start means it is likely any nuance in the circuit is discarded in favor of simplicity. Because engineers perceive that they lose their personal IP when recreating schematics, many engineers I know would prefer to stay in one technology for a few years...or if it were possible, for their career. But this is not possible, so engineers should make quick work to reuse designs across technologies by preserving form, fit, and function of the circuit elements, even if the modeling parameters must change.
5. A colleague with many years of experience put, “The layout is the circuit” in his signature block. Parasitic layout devices plague all levels of hierarchy, including the board, and they must be modeled for a successful design. At the board level, parasitic elements are usually inductances in series with switched currents. At the IC level, they are usually capacitors that couple noisy signals to sensitive signals or cause a high-speed signal (either digital or analog) to become slow. Post-layout extracted simulations are a very important step. A tip is to use net naming conventions on the schematics that facilitate debugging — that is, carefully choose signal names that will not conflict when propagated at multiple levels of the hierarchy.
6. Requirements-tracking software that can store metadata creates a framework for cross-functional collaboration — and after product release, for external auditing. Programs I have used include JAMA Connect and Gitlab. This last EDA tool can have a key role in synthesizing the outputs of the other EDA tools.

I hope this brief commentary on EDA tools is useful and ignites discussion. In summary, engineers are presented with many choices during design. When given a choice between a well-documented, well-modeled, and transparent-looking design versus a design that is less “gifted” in these attributes, they will choose the security of the design they can understand. Otherwise, they may redo the design altogether if no donors can be found that are intentionally transparent. That is my long-story answer to the question about analog circuit reuse.