揭开DCDC EMI中Layout的“神秘面纱”

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(特别鸣谢 **Francesc Estragues**)

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Contents

Introduction

In many seminars we are presented with a suite of techniques to improve the Electro-Magnetic Compatibility (EMC) of our designs.

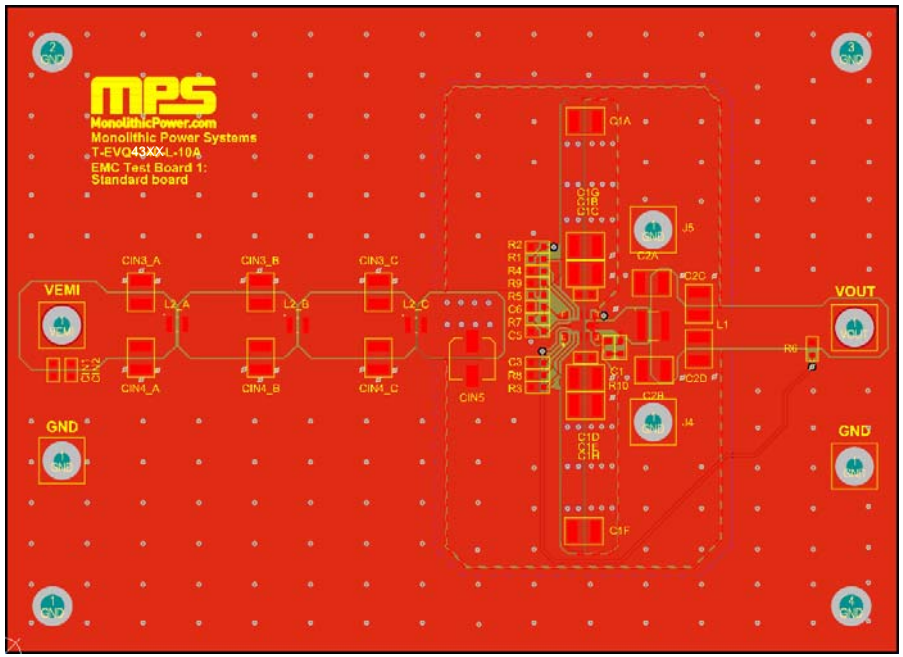
These techniques don't often come with accurate A to B comparisons to evaluate if they are true, or "quantify" the impact of a particular implementation.

EMC is a very "design specific" topic, there are general physics laws that always apply, but things that are good for a particular design may not be optimal for a different one.

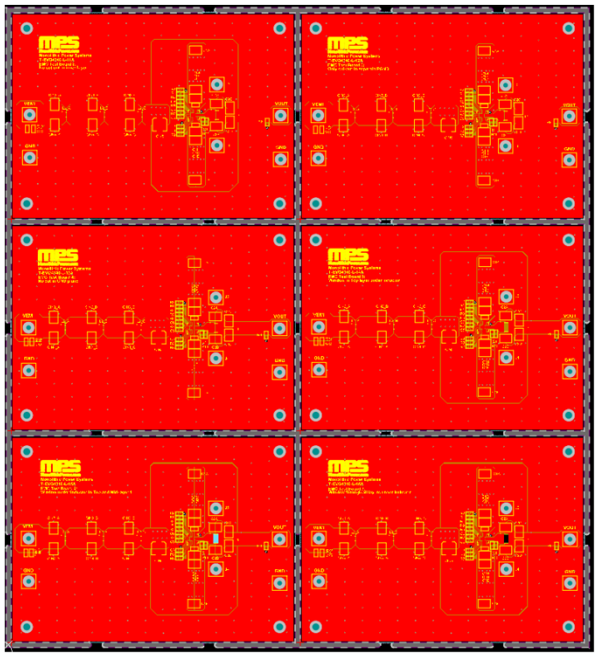
This presentation shows our efforts at trying to myth bust some of the most common EMC tips given in seminars.

Methodology

In order to accurately study the effect of each individual design technique we have designed a set of PCB that share a similar layout but each featuring a specific change.

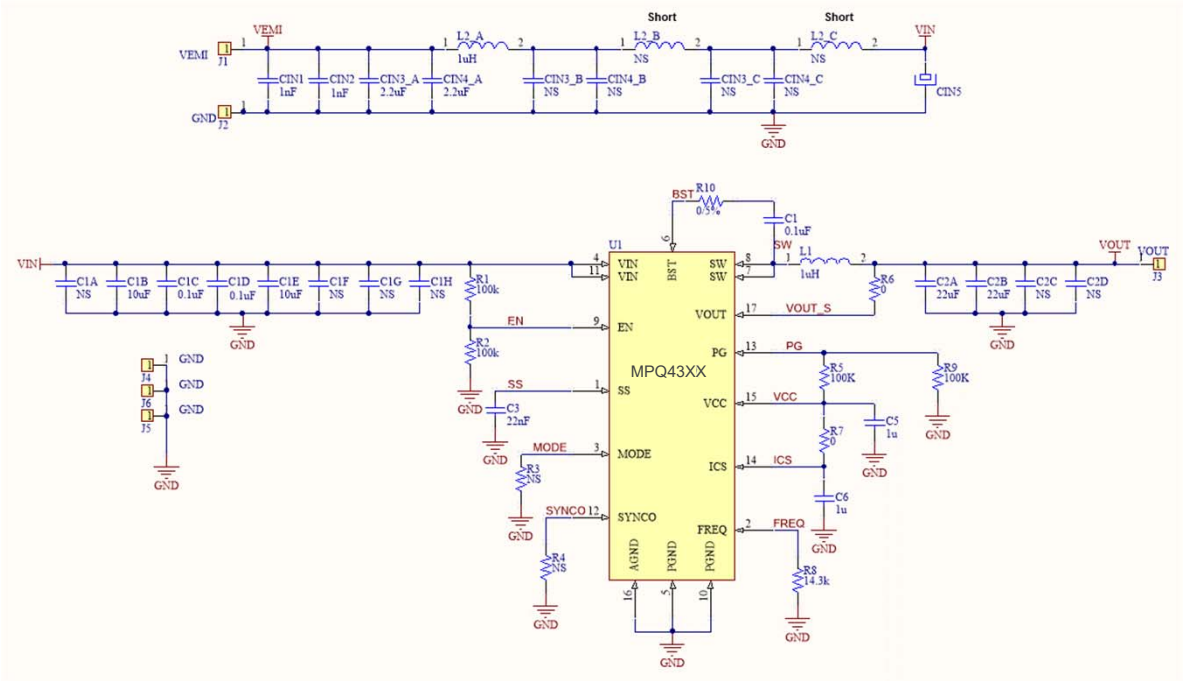


Standard Reference PCB



Methodology

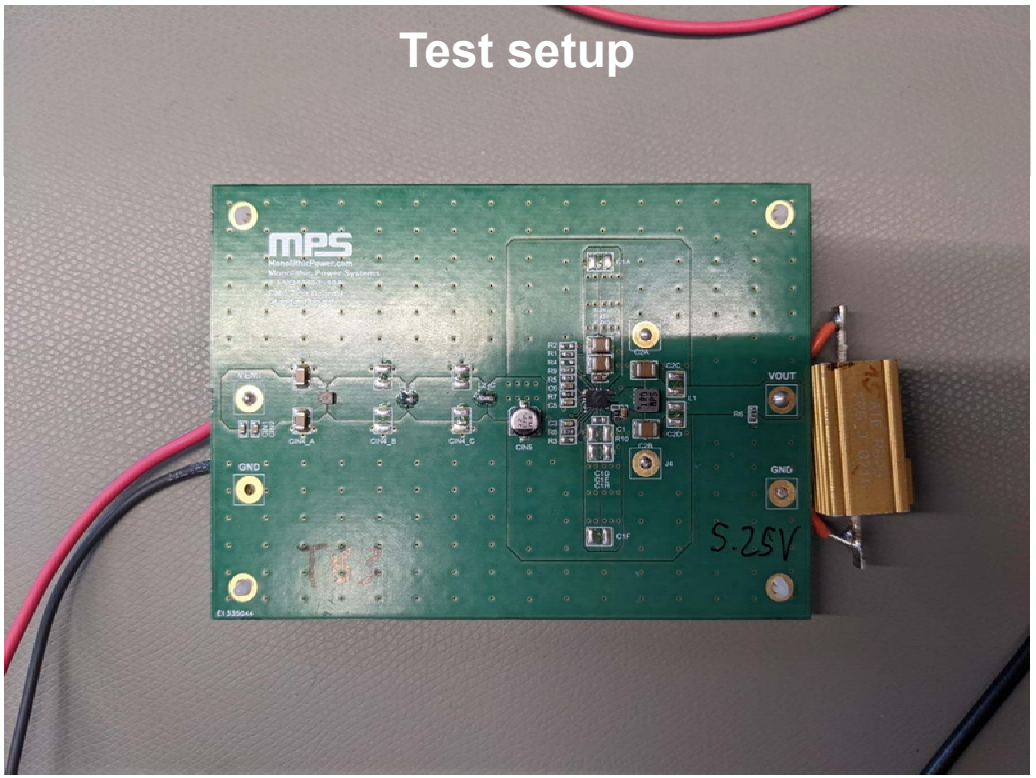
All PCB share the same schematics, but in some cases the components were populated in different footprints.



Standard Reference Schematics

Methodology

The input harness follows CISPR25 standard. The output resistor is connected with short cables to the PCB



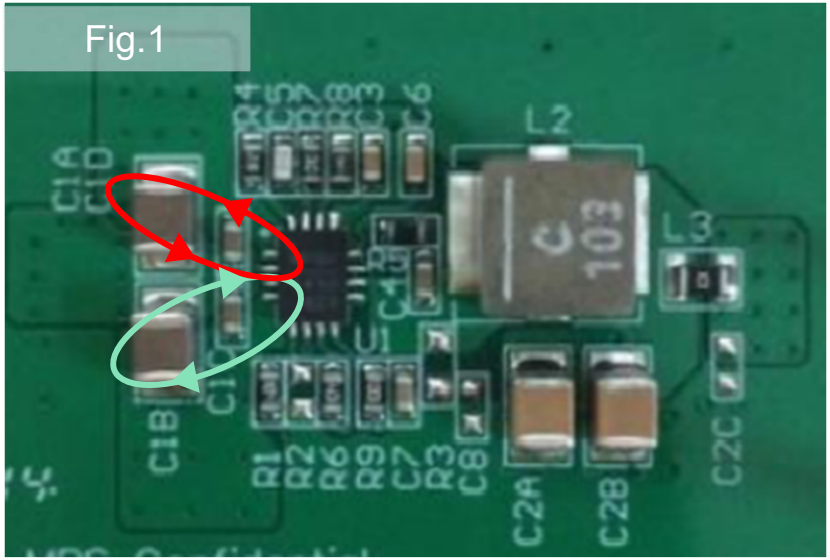
Myth EMC Techniques

Symmetrical input capacitors

Symmetric Input Capacitors: What is the *myth* about?

When placing the input capacitors symmetrically, creating 2 opposing current loops, the magnetic fields created by the dI/dt cancel each other as they have opposite directions.

Fig.1



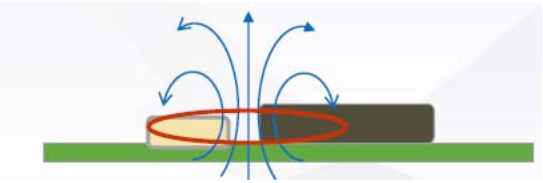
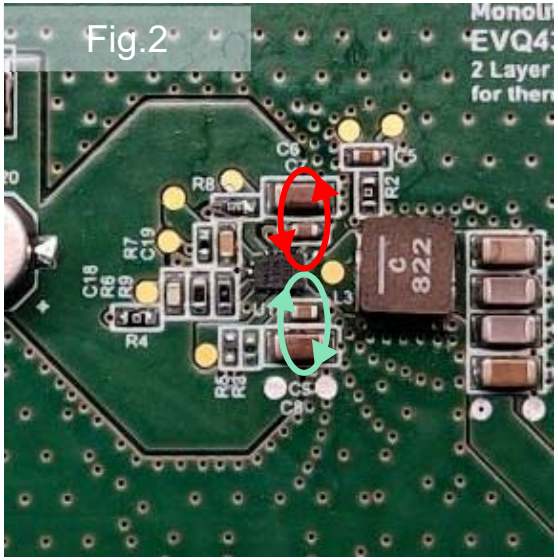
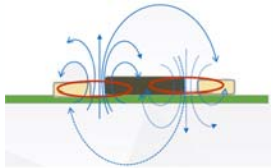
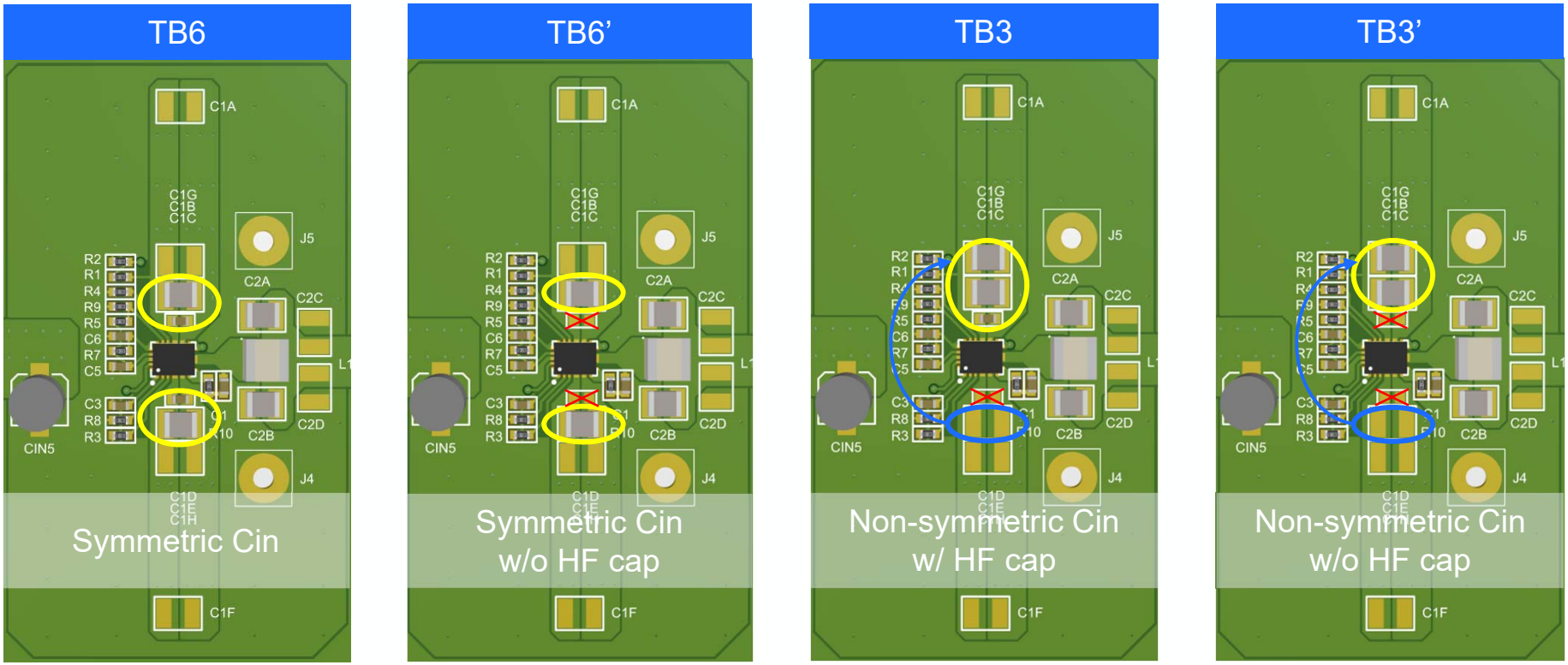


Fig.2



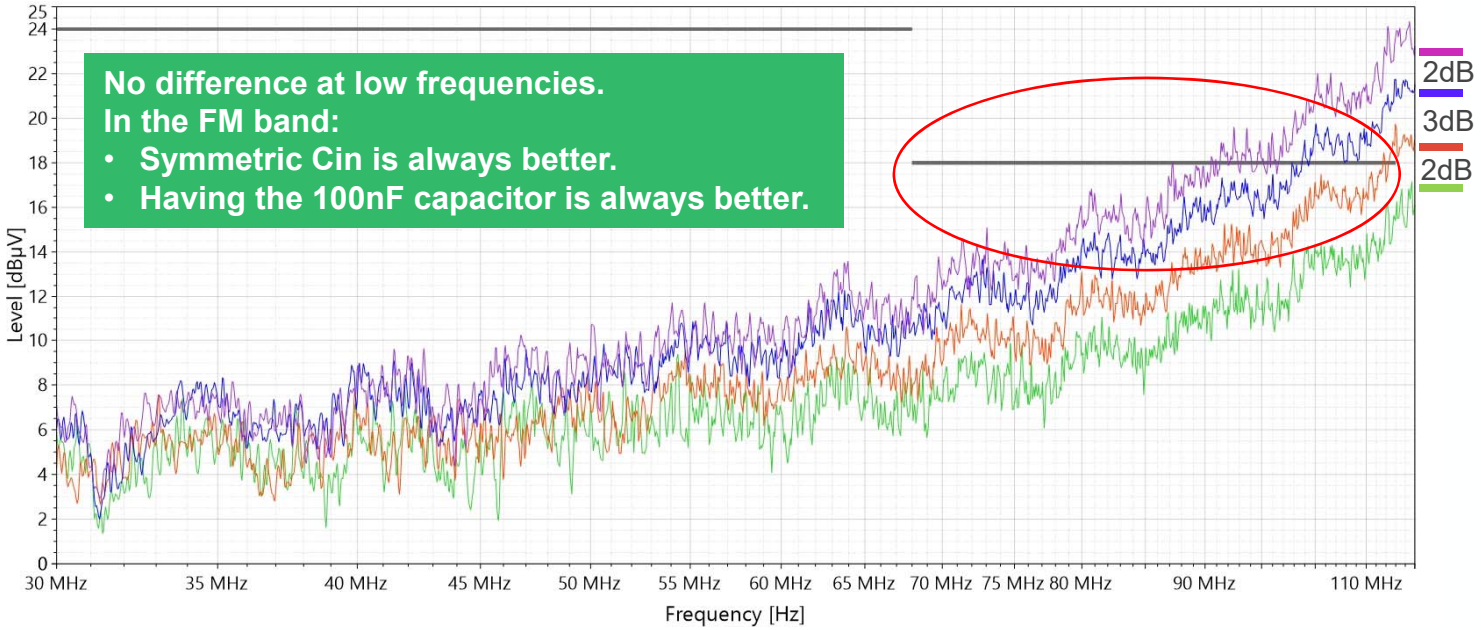


Symmetric Input Capacitors: How was it tested?



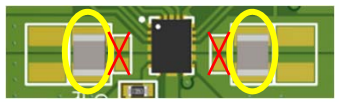
Symmetric Input Capacitors: Test results

CISPR25 Class 5: CE Average measurements

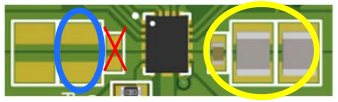


TB6: Symmetric Cin with 100nF

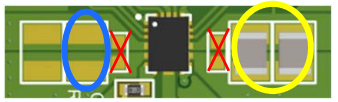
TB6': Symmetric Cin removing 100nF



TB3: Asymmetric Cin with 100nF

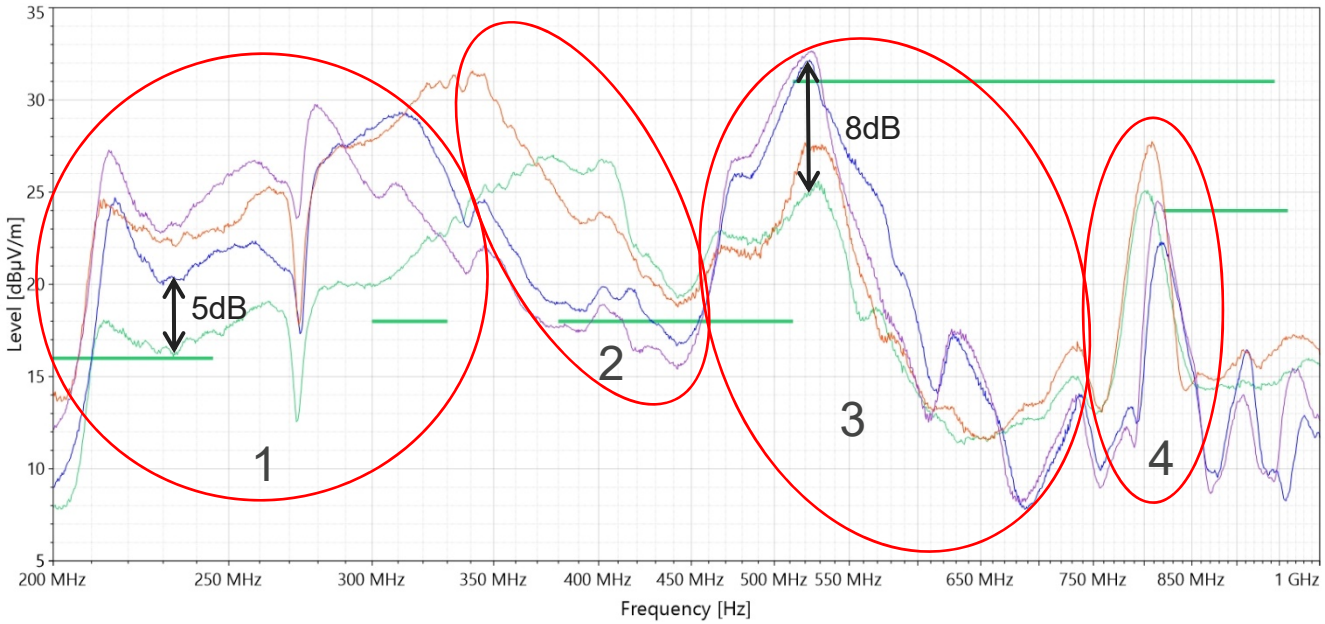


TB3': Asymmetric Cin removing 100nF



Symmetric Input Capacitors: Test results

CISPR25 Class 5: RE Log Average measurements (Vertical)

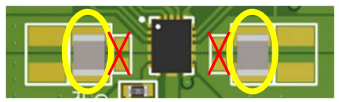


In 1 and 3 the symmetric Cin is ~8dB better.
In 2 the symmetric Cin is ~8dB worse.
In 4 it is ~3dB worse.

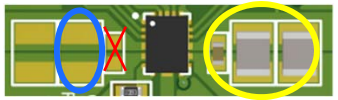
The 100nF capacitor is always better.

TB6: Symmetric Cin with 100nF

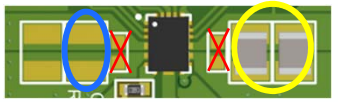
TB6': Symmetric Cin removing 100nF



TB3: Asymmetric Cin with 100nF

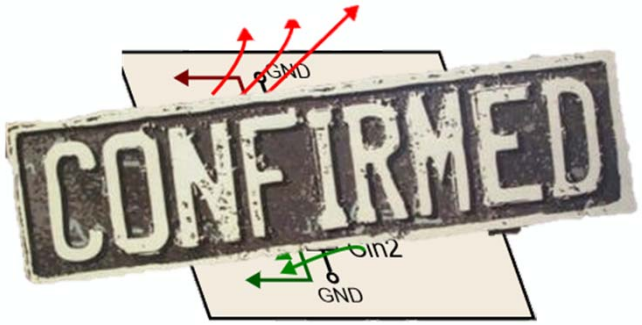


TB3': Asymmetric Cin removing 100nF



Symmetric Input Capacitors: Mythbusting

- The symmetrical input capacitors help improve the EMI in the critical FM band for the Conducted Emissions test.
- In the Radiated Emissions test, they improve the emissions in most bands, while in others they degrade the performance. This is probably due to the decrease of the parasitic L, which moves the resonances to higher frequencies.
- The 100nF capacitors are helpful in almost all frequencies.
- The more problematic bands for the symmetrical capacitors can be improved by other methods like using a Ferrite bead or the next topics.



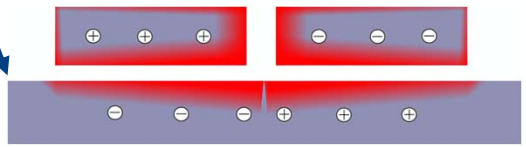
Myth EMC Techniques

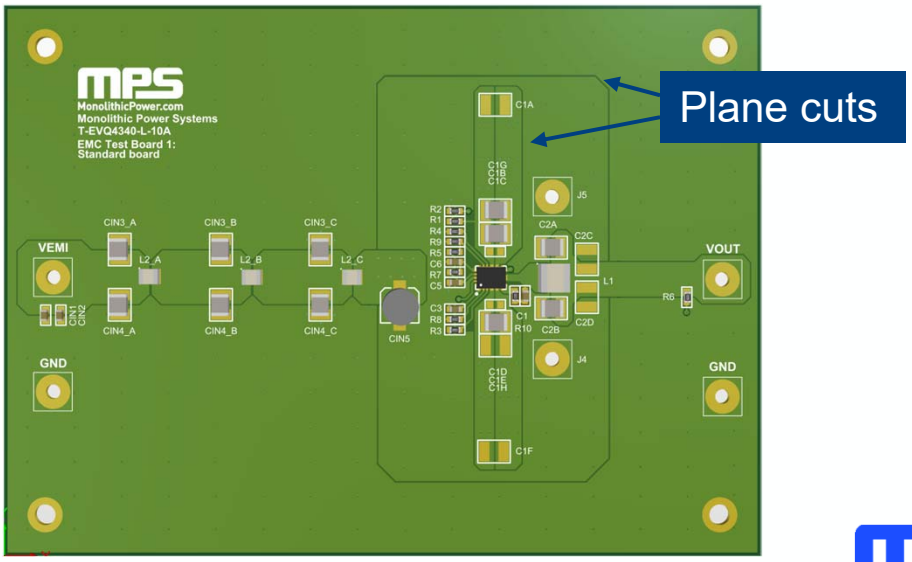
Splitting ground planes

Ground plane splitting: What is the *myth* about?

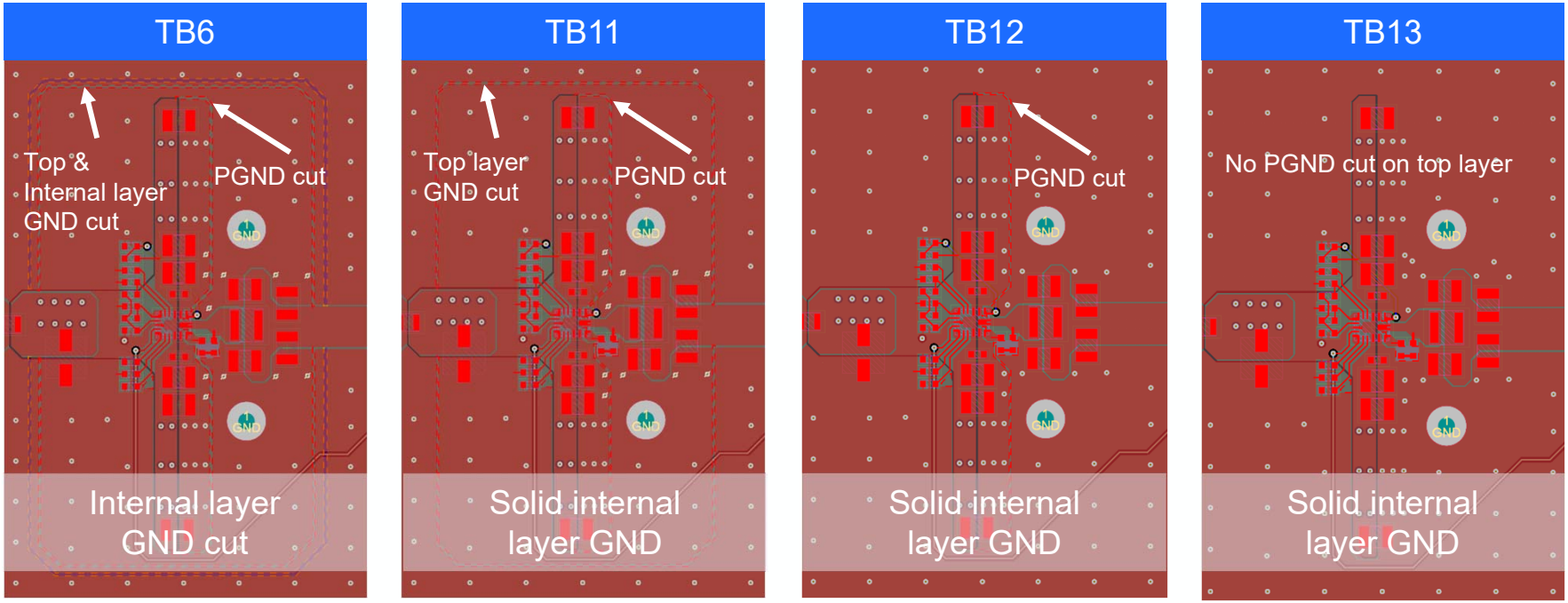
Return currents in the GND plane are mostly concentrated next to their source conductor, but part of them is spread over a wider surface of the plane. These larger current loops form a magnetic antenna and will radiate. By cutting the GND portion of the hot loop from the rest of the board's GND, these current loops are forced to be smaller and thus, the emission will be lower.

Current density is low, but not 0



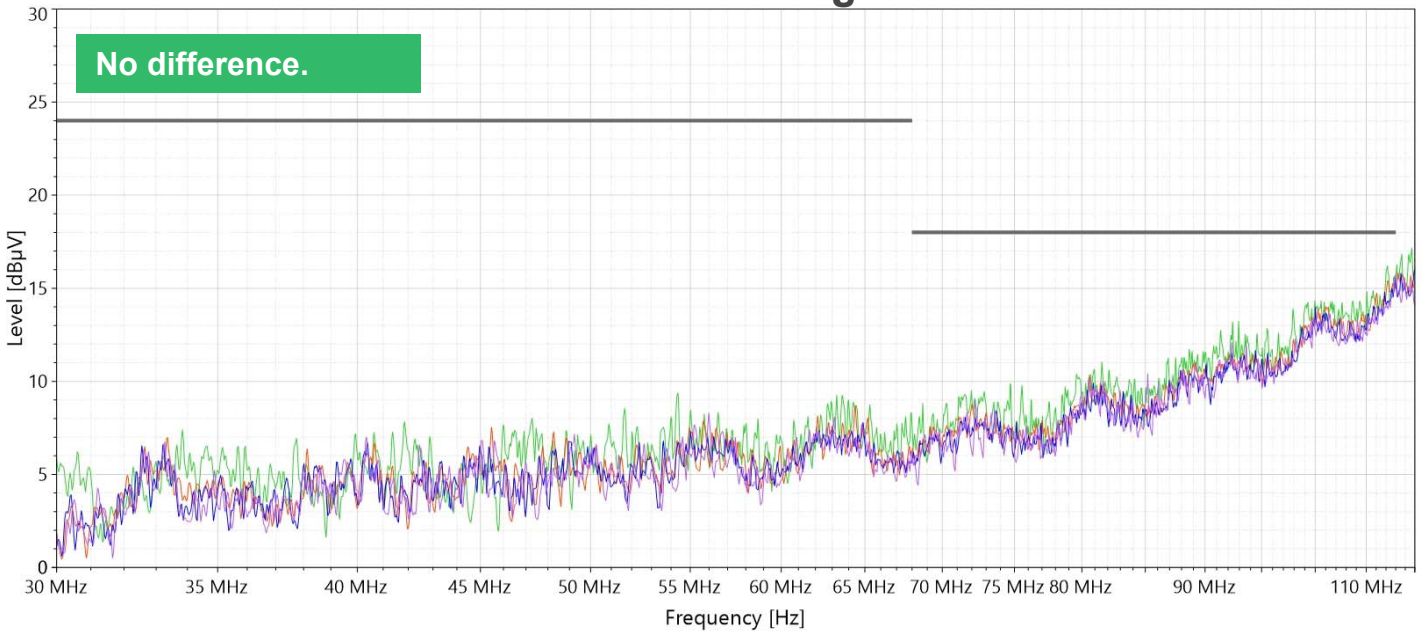


Ground plane splitting: How was it tested?



Ground plane splitting: Test results

CISPR25 Class 5: CE Average measurements



TB6: All GND cuts

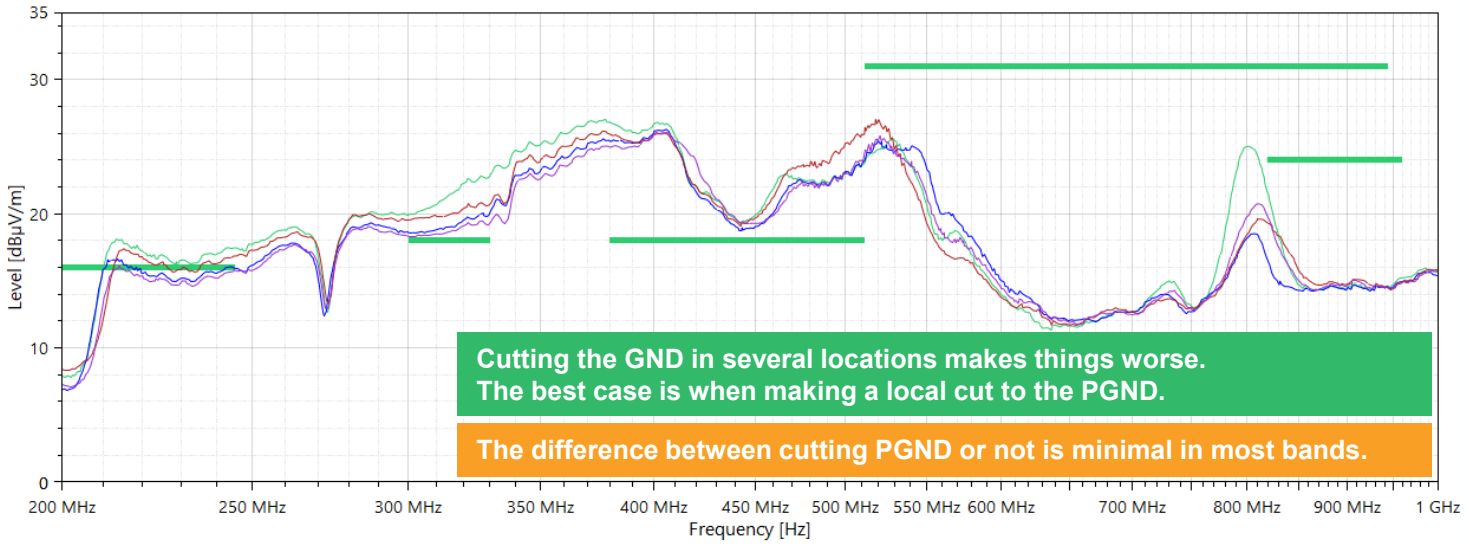
TB11: Removing Internal GND cut

TB12: Removing Internal and Top GND cut

TB13: Removing all cuts

Ground plane splitting: Test results

CISPR25 Class 5: RE Log Average measurements (Vertical)



TB6: All GND cuts

TB11: Removing Internal GND cut

TB12: Removing Internal and Top GND cut

TB13: Removing all cuts

Ground plane splitting: Mythbusting

- Splitting the GND plane in the power converter circuit does not have a significant impact on EMI (<1 dBμV/m).

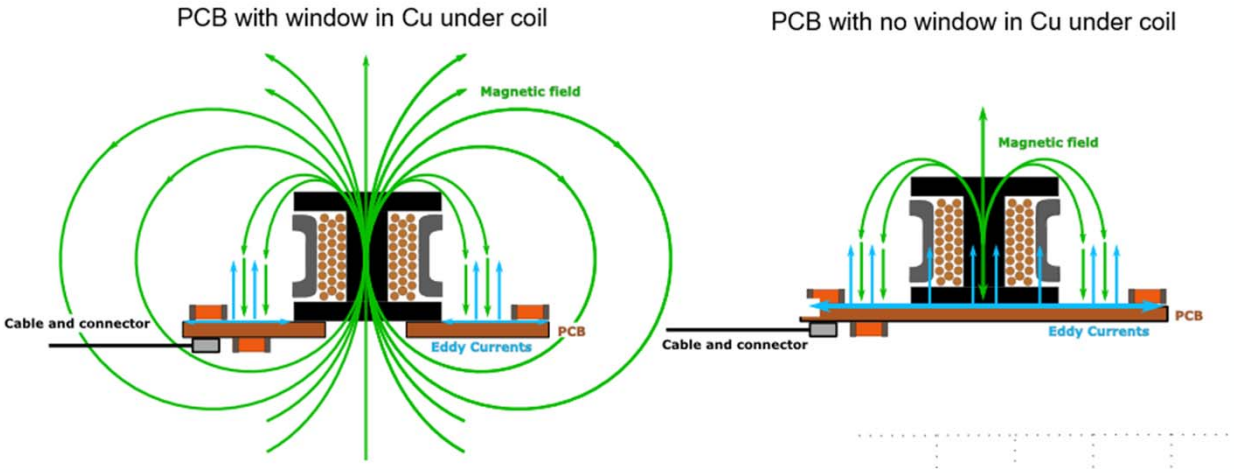
- When Cutting the GND plane in multiple areas, placing Vias as much as possible to reduce the influence of parasitic parameter.

Myth EMC Techniques

Having copper under the inductor

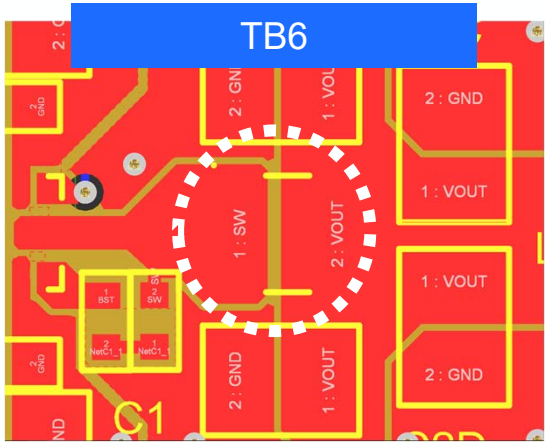
Copper under the inductor: What is the *myth* about?

The magnetic fields emitted by the inductor create eddy currents when they hit perpendicular to a conductor.
These eddy currents create losses in the form of heat and reduce the effective inductance. However, the eddy currents also generate magnetic fields which oppose the inductor's one. By placing copper under the inductor, most magnetic field is captured and converted to eddy currents so the emissions are lower.

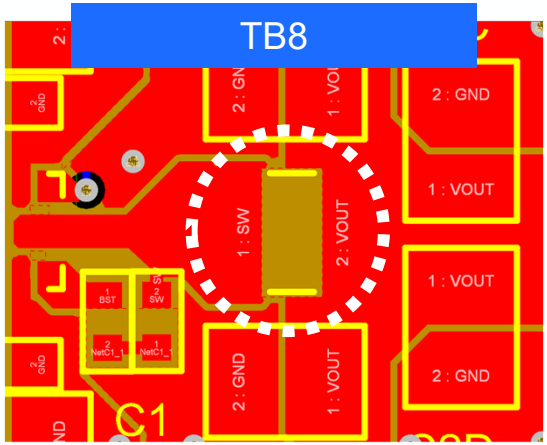


Copper under the inductor: How was it tested?

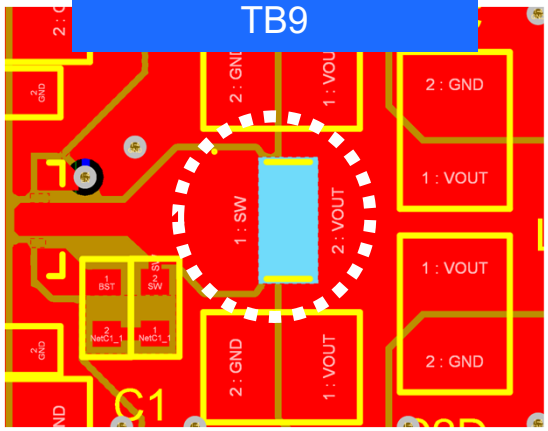
TB6



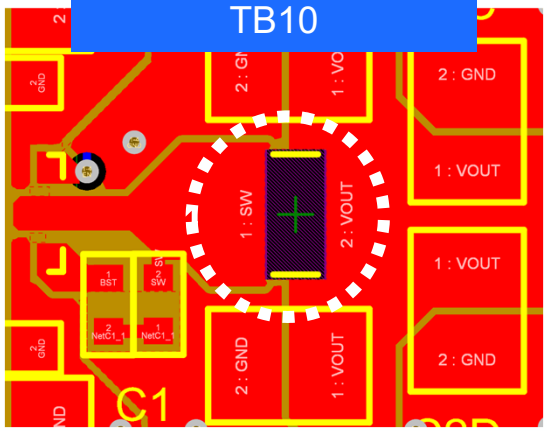
TB8



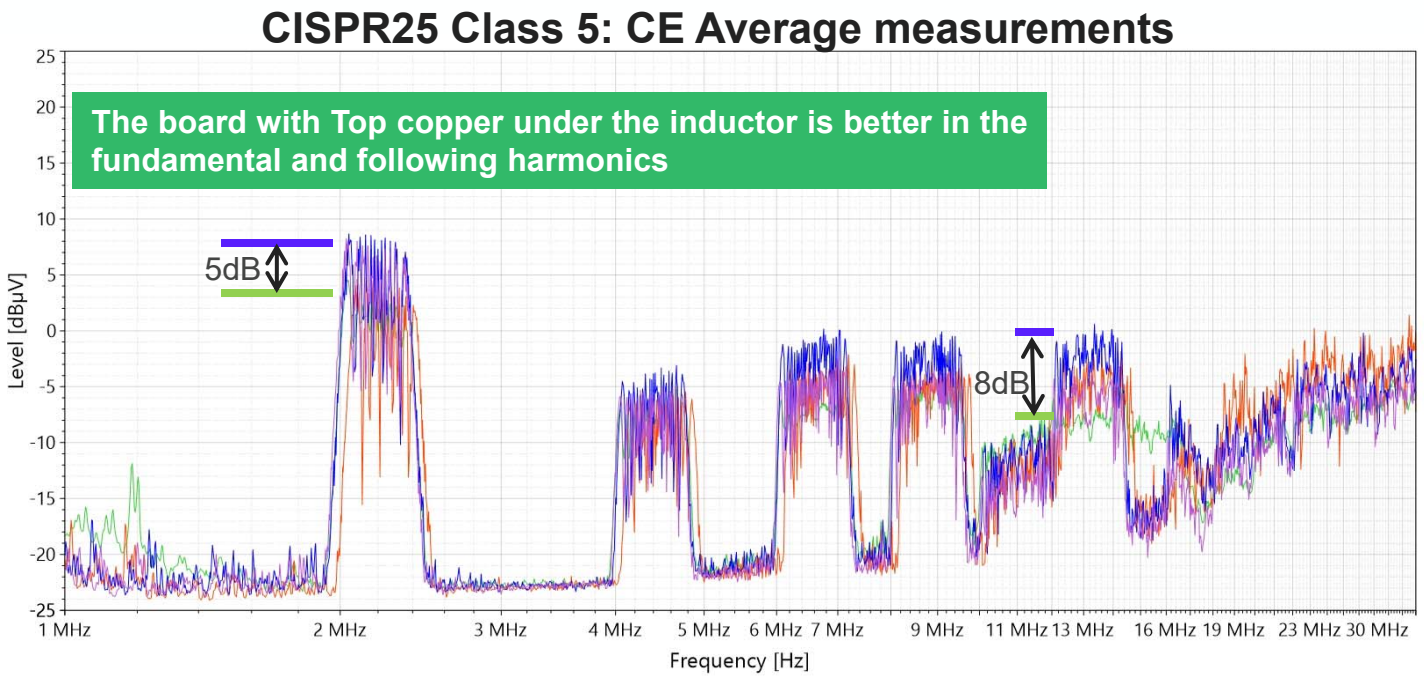
TB9



TB10



Copper under the inductor: Test results



TB6: Copper under L

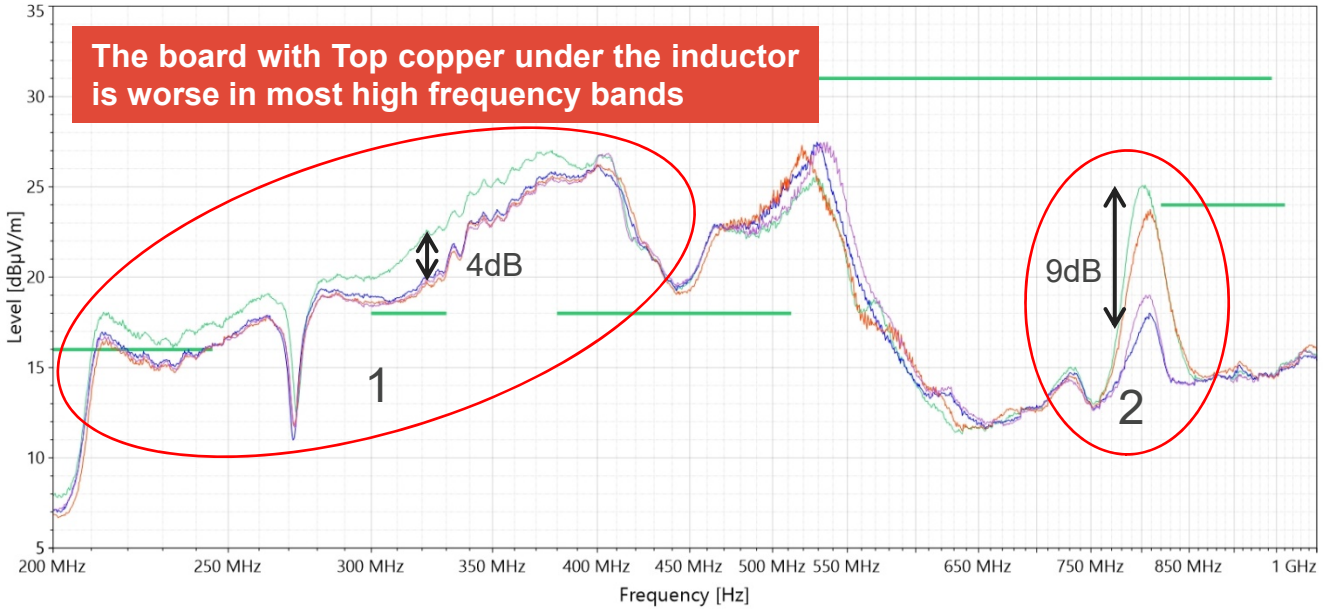
TB8: Removing Top copper

TB9: Removing Internal and Top copper

TB10: Removing all copper

Copper under the inductor: Test results

CISPR25 Class 5: RE Log Average measurements (Vertical)



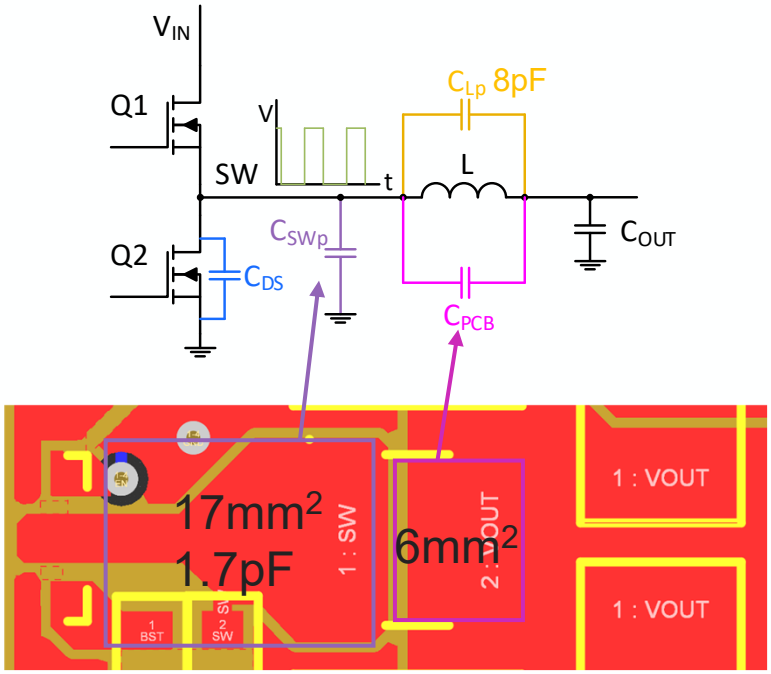
TB6: Copper under L

TB8: Removing Top copper

TB9: Removing Internal and Top copper

TB10: Removing all copper

Copper under the inductor: Analysis

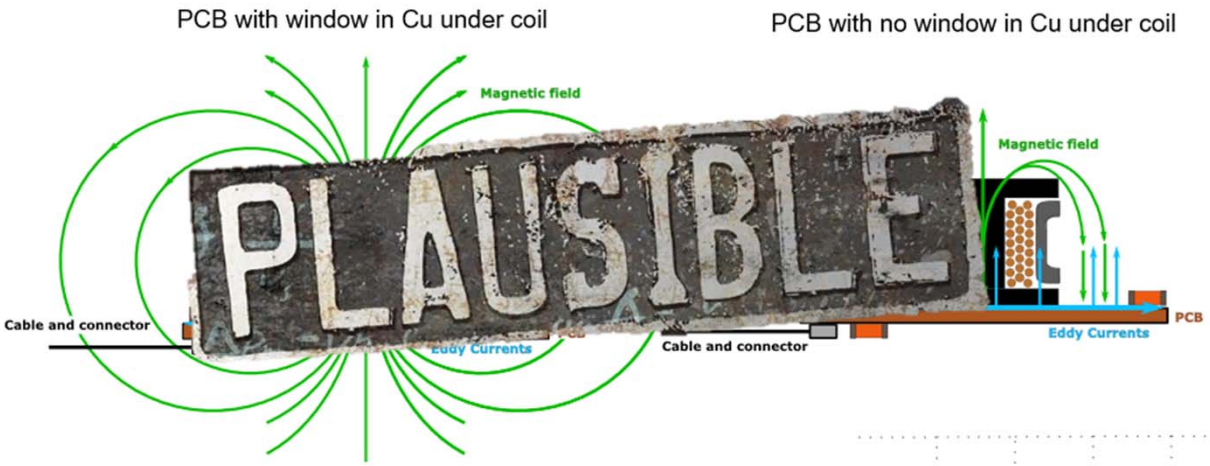


The copper area under the inductor in top layer is Vout. The eddy currents are induced there. The Parasitic Capacitance between SW and Vout is increased by this extra area.

Copper under the inductor: Mythbusting

The test results in CE show a reduction in the emitted noise when having copper directly under the inductor.

The test results in RE show an increase in the emitted noise when having copper directly under the inductor. This may be caused by the copper being Vout instead of GND.

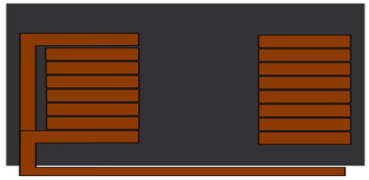


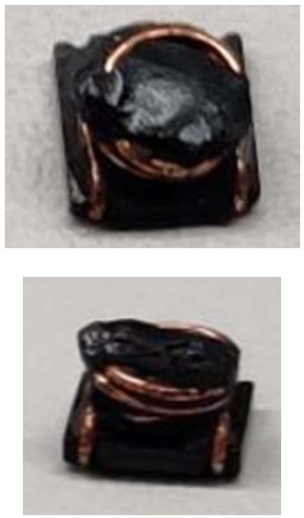
Myth EMC Techniques

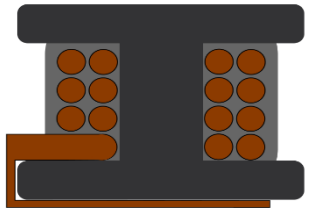
Shielded inductors

Shielded inductors: What is the *myth* about?

Shielded inductors are regarded as to always have better EMI performance compared to non-shielded or *semi-shielded inductors.*







Shielded (molded)

Semi-Shielded (epoxy coating)

Shielded inductors: How was it tested?

Changed the standard molded inductor used in all other test MPL-AY4020-1R0 to the semi-shielded MPL-SE4030-1R0

APPLICATIONS

- Battery-powered devices
- Embedded computing
- High-current SMPS
- High-frequency SMPS
- POL converters
- FPGA

FEATURES

- Size 4.1mmx4.1mmx1.9mm
- Low DCR
- Low AC Losses
- Low Audible Noise
- Molded Construction
- Soft Saturation
- Stable Over High Temperatures
- Max Operating Temp +155°C
- RoHS/REACH-Compliant, Halogen-Free

ELECTRICAL CHARACTERISTICS

Parameter			Value	Unit
Inductance (1)	L	±20%	1.0	µH
Resistance	R_{DC}	typ	10.1	mΩ
Resistance MAX	$R_{DC\ MAX}$	max	11.8	mΩ
Rated Current (2)	I_R	typ	7.9	A
Saturation Current 25°C (3)	$I_{SAT\ 25°C}$	typ	8.6	A
Saturation Current 100°C (4)	$I_{SAT\ 100°C}$	typ	8.6	A
Resonance Frequency	f_r	typ	56	MHz

Cp=8pF

APPLICATIONS

- Battery-powered devices
- High-efficiency SMPS
- Embedded computing
- Input filters

FEATURES

- Size 4mmx4mmx3mm
- Semi-Shielded Construction
- Low DCR
- Low Stray Field
- Max Operating Temp +125°C
- RoHS/REACH-Compliant, Halogen-Free

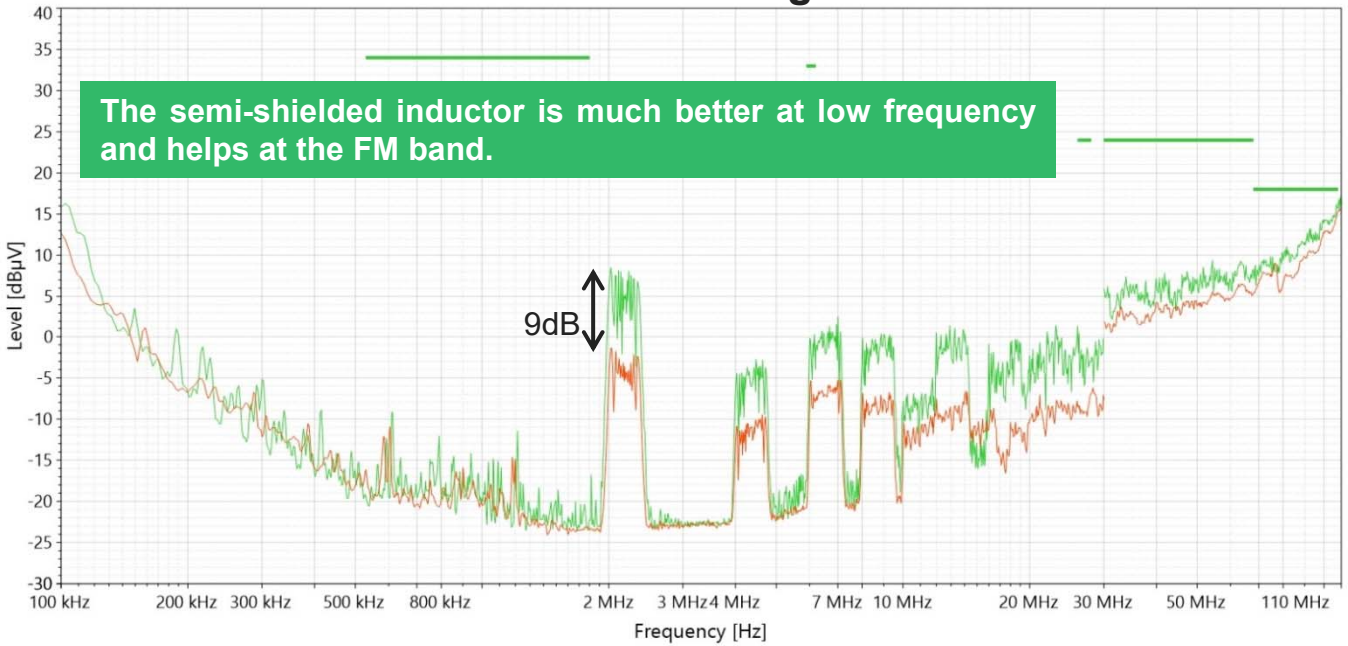
ELECTRICAL CHARACTERISTICS

Parameter			Value	Unit
Inductance (1)	L	±20%	1.0	µH
Resistance	R_{DC}	typ	12.5	mΩ
Resistance MAX	$R_{DC\ MAX}$	max	15	mΩ
Rated Current (2)	I_R	typ	6.3	A
Saturation Current 25°C (3)	$I_{SAT\ 25°C}$	typ	7.5	A
Saturation Current 100°C (4)	$I_{SAT\ 100°C}$	typ	7.2	A
Resonance Frequency	f_r	typ	90	MHz

Cp=3pF

Shielded inductors: Test results

CISPR25 Class 5: CE Average measurements

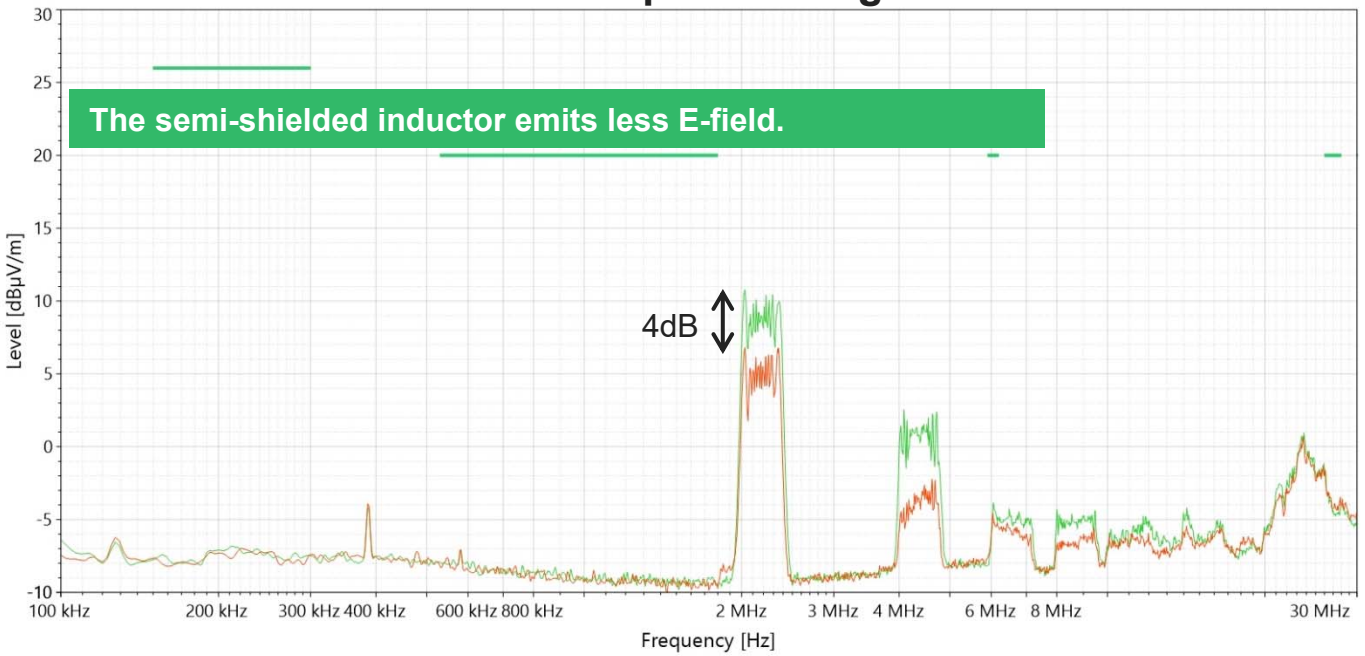


TB6: Molded Inductor

TB15: Semi-Shielded Inductor

Shielded inductors: Test results

CISPR25 Class 5: Monopole Average measurements

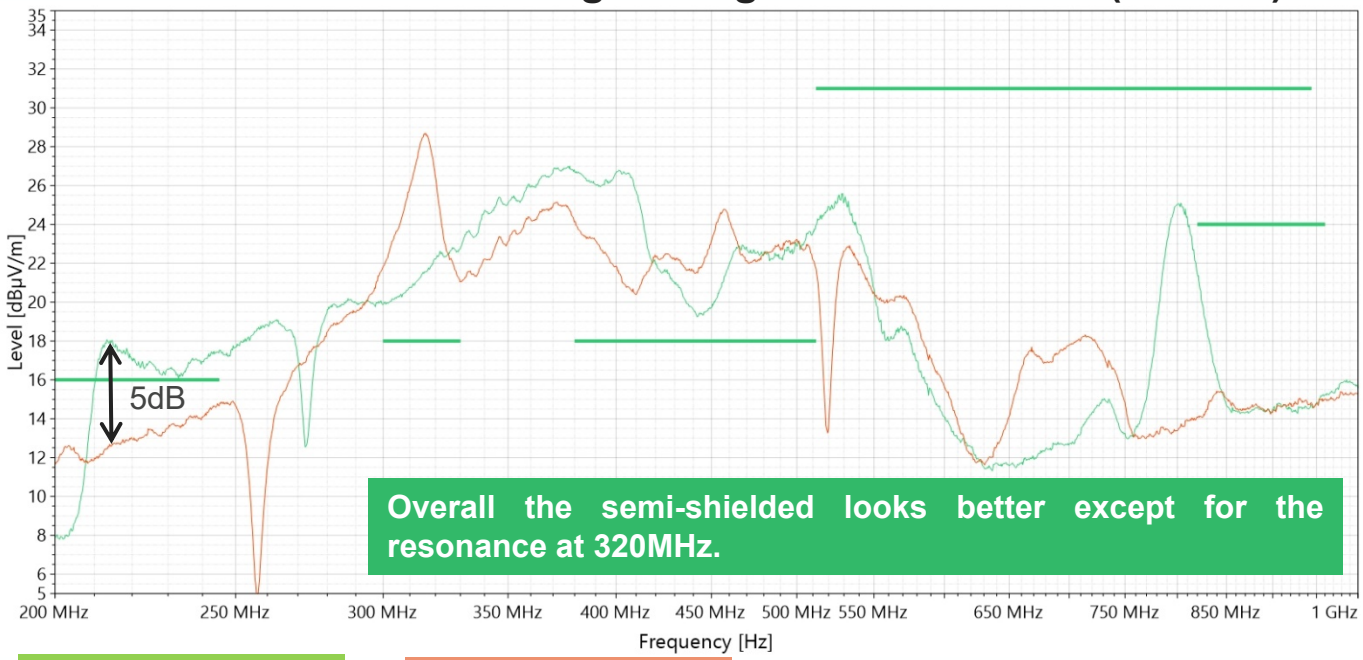


TB6: Molded Inductor

TB15: Semi-Shielded Inductor

Shielded inductors: Test results

CISPR25 Class 5: RE Log Average measurements (vertical)

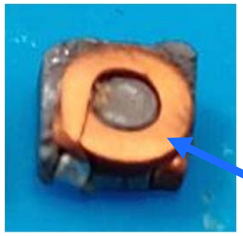


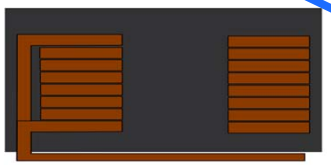
Overall the semi-shielded looks better except for the resonance at 320MHz.

TB6: Molded Inductor

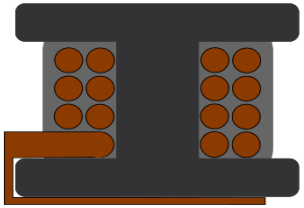
TB15: Semi-Shielded Inductor

Shielded inductors: Analysis

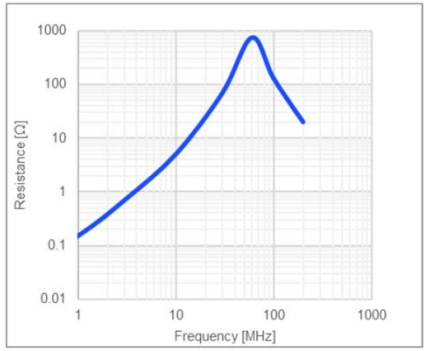




Larger area for E-field radiation

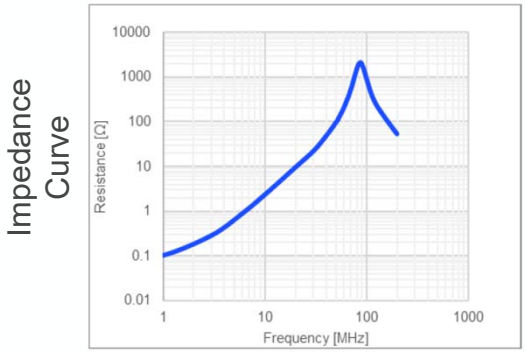


Shielded (molded)



Cp=8pF

Semi-Shielded (epoxy coating)



Cp=3pF

Shielded inductors: Mythbusting

From previous experience, it is true that in some cases shielded inductors improve the EMC results.

In this particular test, the shielded inductor exhibits worse EMI than the semi-shielded. This is due to the construction of the inductor.

Each design is unique, you have to test in the early stages and evaluate which components are best. Not all inductors are built equal.

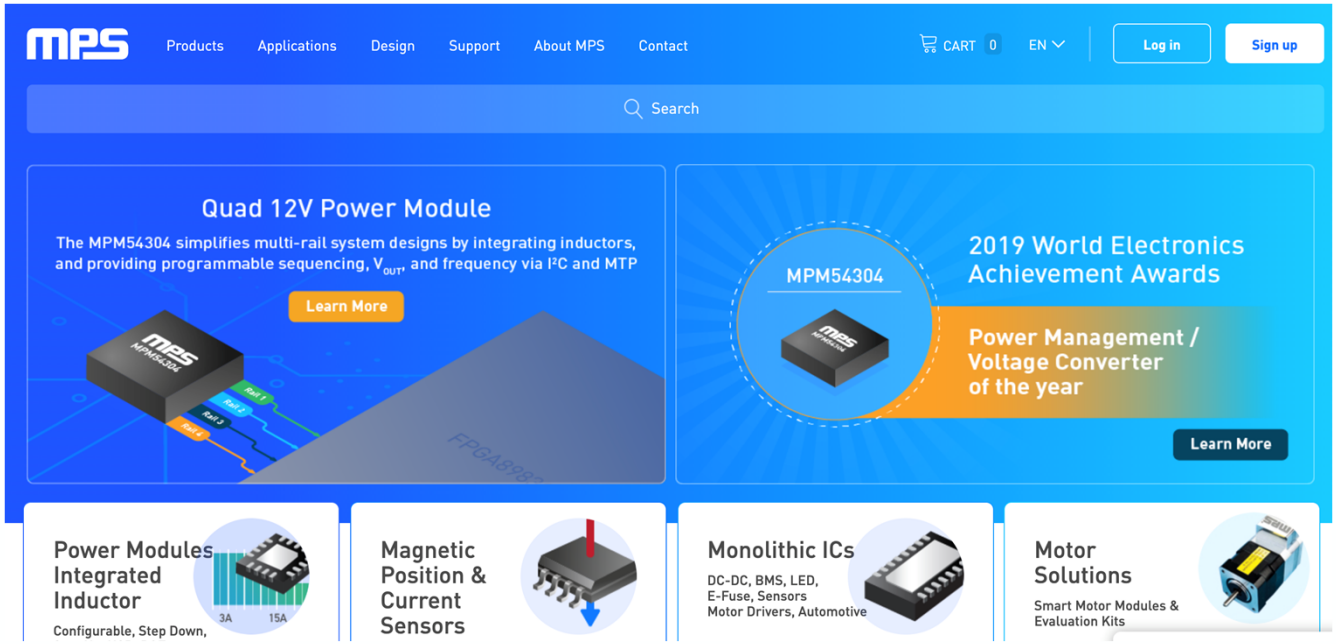
Lower radiation

Credit. Christian Kueck

Conclusions

- Many EMC recommendations given in seminars are not valid across all designs. There are several variables at play (PCB size, load type, harnesses…).
- The way to ensure if a design is going in the right direction is through testing in the early stages of development.
- Start the design following the typical EMC good practices like symmetrical input capacitance, adding a 100nF capacitor, choosing a good inductor…
- Test the initial design and see what are its shortcomings. Then come up with a plan to fix the issues in the identified frequencies.
- Execute the improvement plan, then repeat the testing to check if the new system is on the right track.

Q&A



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