# Load-Line Design for a Multi-Phase Buck Converter

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## Introduction

With the increase in 5G networks, cloud computing, Internet-of-Things (IoTs), and virtualization, IT infrastructure is driving the demand for high-performance computing servers.

Each new server generation requires higher computing power and efficiency, while also increasing power requirements. One of the key aspects in ensuring that servers meet market demands is to understand the effect that the microprocessor's power supply has on both the dynamic response and efficiency of the server as a whole, then to configure the power supply for optimal performance.

Server applications are especially demanding when it comes to transient response requirements. In order to meet these requirements, designers can implement load-line control, which is sometimes also referred to as active voltage positioning (AVP).

## Understanding DC Load-Line Design

Load line (LL) control refers to a modification of the voltage control loop where the buck converter's output voltage ($V_{OUT}$) is adjustable based on the load current. In other words, $V_{OUT}$ is no longer constant for all load values, and instead changes according to the power demand. The adjusted output voltage can be calculated with Equation (1):

$$V_{OUT} = V_{OUT(NOM)} - I_{OUT} \times R_{LL} \quad (1)$$

Where $V_{OUT(NOM)}$ is the maximum $V_{OUT}$ when there is no load connected to the power supply, $I_{OUT}$ is the load current, and $R_{LL}$ is the equivalent load-line impedance (in Ω).

Figure 1 shows how implementing load-line regulation degrades the DC load regulation (denoted with the blue line), causing $V_{OUT}$ to slope down as the current increases, compared to the traditional approach that fixes $V_{OUT}$ for all loads (denoted with the green line). Note that the voltage slope created by the load line must still be designed to meet the $V_{OUT}$ requirements for powering microprocessors. This means that $V_{OUT}$ must fall within specified voltage limits ($V_{MAX}$ and $V_{MIN}$) for the entire output current range.

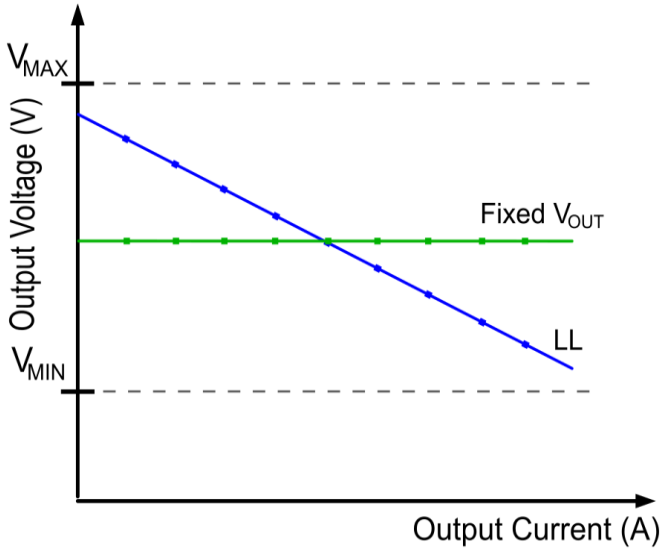


**Figure 1: $V_{OUT}$ with DC Load Line vs. the Fixed $V_{OUT}$ Method**

The main reason to implement load-line regulation is to lower the voltage when the load current is very large, and thereby reduce power consumption and dissipation loss. While this is a frequently discussed benefit, another advantage of implementing load-line control is how it improves the server's dynamic response.

Power supplies in server applications often have to support large load transients. This is because power supplies in server applications must power loads such as storage devices and CPUs, whose power requirements vary according to the task(s) they are executing. For example, it is not uncommon for a server power supply to deliver current steps well above 100A.

Figure 2 shows a power supply before and after implementing the load line. Due to the current step, the power supply without a load line (denoted with the purple line) experiences large overshoots and undershoots during load transients. If these peaks exceed the maximum or minimum voltage limits, this can cause the load to break down and cease functioning. By gradually adjusting $V_{OUT}$ with the implementation of a load line (denoted with the blue line), these peaks can be eliminated and the transient response is improved.

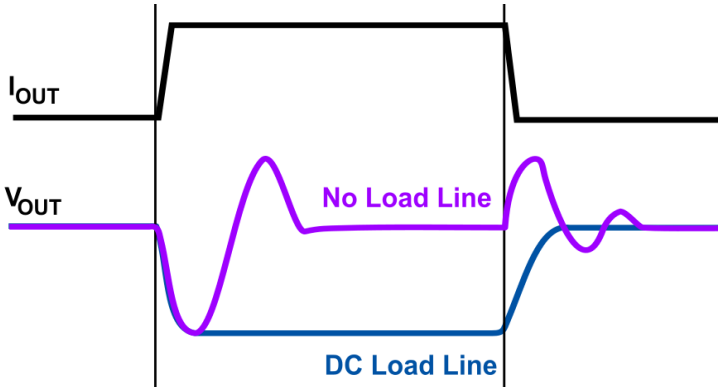


**Figure 2: Effect of Load Line on Transient Response**

While load line improves server performance and efficiency, the load-line configuration must be very accurate, since the converter must always operate within the set voltage limits. Most communication standards specify ideal load-line values, but these values may need to be tweaked due to different board materials and layouts. Otherwise, the load line may push the voltage below the minimum requirements when operating at high power (see Figure 3).

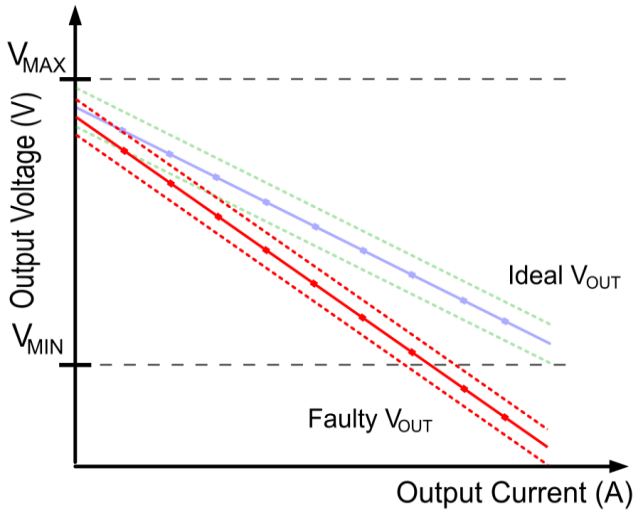


**Figure 3: Errors Caused by Suboptimal Load-Line Configurations**

### Reducing Output Capacitance with DC Load Line

To demonstrate the benefits of load line control, a general example was created with typical processor specifications for a power rail. The input voltage ($V_{IN}$) was set to 12V, the output current ($I_{TDC}$) was 220A, and the output voltage ($V_{OUT}$) was 1.8V — all of which are generic values for a voltage rail in server applications. Table 1 shows the specifications.

**Table 1: Power Rail Specifications**

| Parameter | Value |
|---|---|
| $V_{IN}$ | 12V |
| $V_{OUT}$ | 1.8V |
| $I_{TDC}$ | 220A |
| $\Delta V_{OUT}$ | ±108mV (216mVpp or 6%) |
| $I_{STEP}$ | 160A (0A to 160A) |

Table 2 shows the test conditions, such as output capacitance ($C_{OUT}$), switching frequency ($f_{SW}$), and the number of phases ($N_{PHASE}$).

**Table 2: Test Parameters**

| Parameter | Value |
|---|---|
| $f_{SW}$ | 700kHz |
| $N_{PHASE}$ | 5 |
| $C_{OUT}$ (close to VR) | 6 x 470µF, 12 x 47µF |
| $C_{OUT}$ (at the CPU load) | 60 x 22µF |

The MP2965 — a dual-loop, digital, multi-phase controller — was used to implement this example, since it supports load-line configuration and can be configured for up to 7-phase operation. The PMBus-configurable load line requires a droop resistor ($R_{DROOP}$) to be connected between the VDIFF and VFB pins, as well as internal register configurations (see Figure 4).

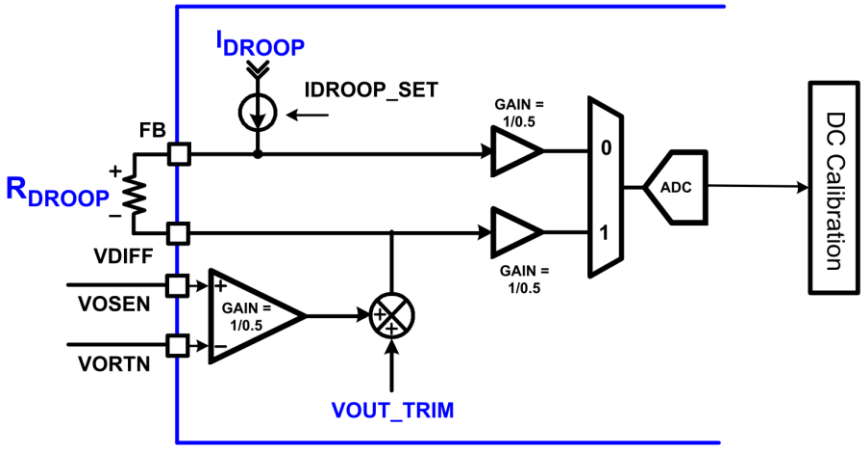


**Figure 4: Controller Load-Line Internal Structure**

First, a designer must establish the effect of the load line by observing the voltage regulation when the converter does not use a load line. A 160A current step was applied to the MP2965 to emulate a CPU load. Figure 5 shows the converter's response without a DC load line. Note the large $V_{OUT}$ spikes that occur during the current transients. This means there is a voltage variation of 205mV, which is barely inside the specifications shown in Table 1.

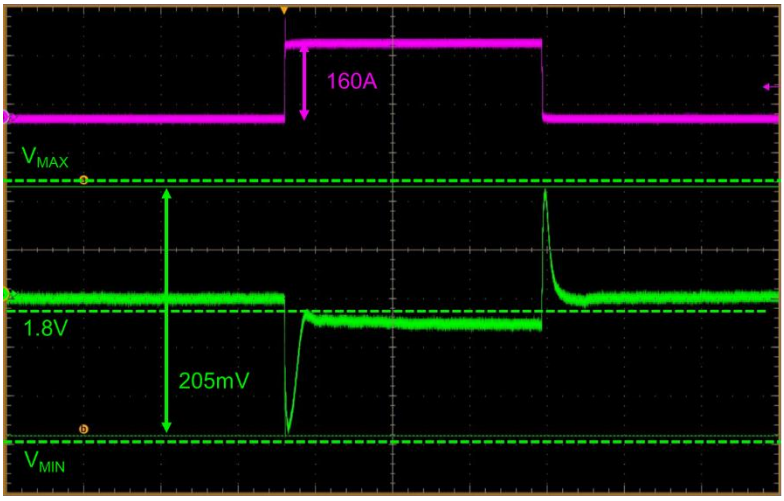


**Figure 5: Converter Response to a Current Step without DC Load Line**

Using Equation 1, a load line of 0.67mΩ was designed to meet the minimum $V_{OUT}$ specification, estimated with Equation (2):

$$V_{OUT} = V_{ID} - I_{OUT} \times R_{LL} \rightarrow R_{LL} = \frac{V_{OUT(NOM)} - V_{OUT(MIN)}}{I_{OUT(MAX)}} = \frac{108mV}{160A} = 0.675m\Omega \quad (2)$$

Figure 6 shows the resulting transient response after implementing a DC load line.

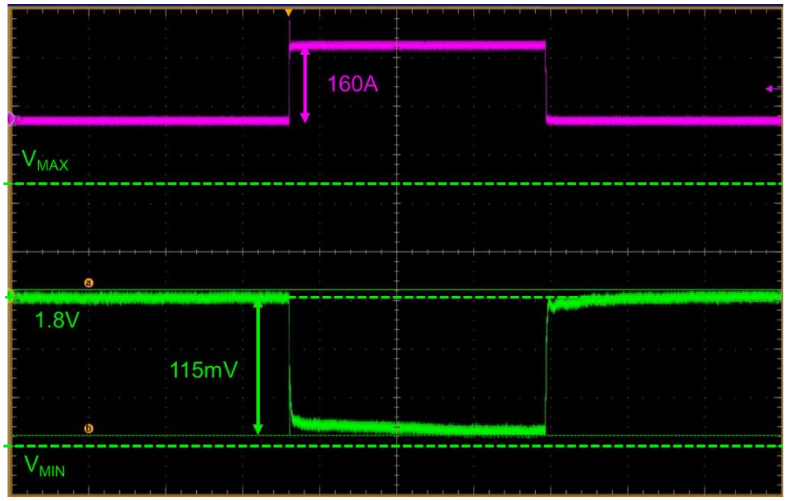


**Figure 6: Converter Response to a Current Step with DC Load Line**

By implementing a DC load line, $V_{OUT}$ stays well within the voltage range specified in Table 1, with a voltage margin of about 50% the permitted range. This increased voltage margin also means that certain design constraints can be loosened, such as the output capacitance, which is one of the key elements used to reduce the peaks in output voltage. As specified in Table 2, the voltage responses shown in Figure 5 and Figure 6 refer to a total output capacitance of 4.7mF, comprised of sixty 22µF MLCC capacitors placed close to the CPU load, along with a few aluminum electrolytic capacitors.

The MLCC capacitors filter out the high-frequency components of the current transient response, whereas the aluminum electrolytic capacitors filter out the low-frequency components. These aluminum capacitors, called bulk capacitors, are specially designed with a very low ESR, meaning that they are typically the most expensive capacitors in the circuit. As a result, fewer bulk capacitors reduces the overall cost and BOM.

Since implementing the DC load line already reduces the transient peaks, bulk capacitance becomes less crucial for transient response and the bulk capacitor's ESR requirements are also reduced. Therefore, some of the bulk capacitors can be removed without this having a significant effect on the circuit's transient response. Figure 7 shows the results after reducing the bulk capacitance by 50% (from 6 x 470µF to 3 x 470µF).

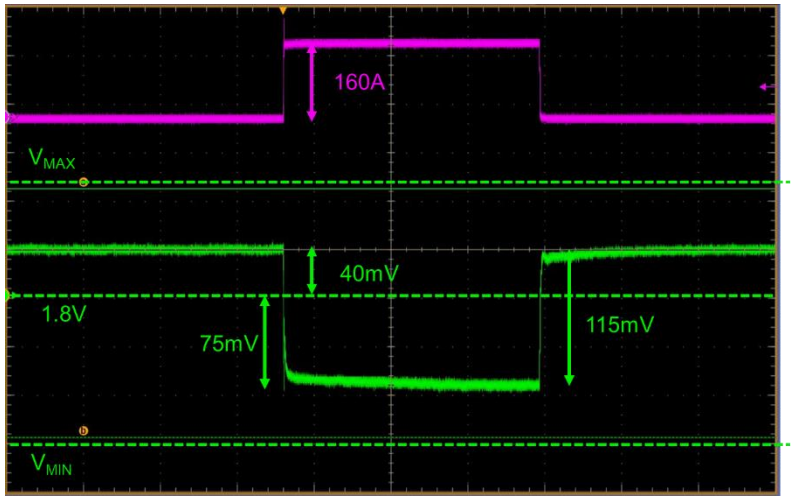


**Figure 7: Converter Response to Current Step with DC Load Line and Fewer Bulk Capacitors**

To increase the voltage margin for both positive and negative spikes, a 40mV DC offset was added to $V_{OUT}$. This places $V_{OUT}$ near the center of the voltage range defined by the specifications.

Although there are fewer bulk capacitors, there is no visible change in the power supply's transient response. However, this still provides the advantage of reduced cost and board space.

An additional benefit of load line is the reduced CPU power dissipation. When $V_{OUT}$ is set to 1.8V at 160A, the load power is 288W. By implementing the DC load line and decreasing $V_{OUT}$ to 1.725 at maximum current, the load power from Figure 7 is 276W, which represents a net power saving of 12W.

## Conclusion

Server and computing applications require power supplies that can handle large, sudden shifts in current while meeting strict $V_{OUT}$ regulation requirements.

Using the MP2965 digital controller to implement a PMBus-configurable load line, this article demonstrated the benefits of load-line control, such as improved efficiency and improved power supply transient response performance. This article also explained how implementing a DC load line reduces the minimum required bulk capacitance, allowing designers to reduce overall cost and minimize board space while still meeting specifications for server applications.