MPF32010 Reference Design

3kW Totem-Pole PFC

Table of Contents

1 Overview

1.1. Description

The EVF32010-18831 evaluation board is an AC/DC power factor correction (PFC) controller based on a totem-pole topology. The totem-pole topology has recently gained popularity due to its simplicity and efficiency. The main issue that had previously held back the wide implementation of Totem-pole topologies was that the transistors were required to be very fast while also being able to block high voltages. This problem has been overcome thanks to the implementation of wide bandgap transistors with fast reverse recovery.

This reference design discusses the ad hoc development of a specific totem-pole PFC controller, as well as optimal sizing and selection of components, to create a highly robust system. Furthermore, time-to-market can be significantly reduced due to the integrated GUI.

1.2. Features

- Efficiency Exceeding 98.5% at Nominal Conditions
- Power Factor Exceeding 99% at Nominal Conditions
- 3kW Rated Power
- GUI Interface
- **Meets the Following Standards:**
  - Harmonic Currents: IEC 61000-3-2
  - Conducted EMC: CISPR 32
  - Voltage Sags: IEC 61000-4-11

1.3. Applications

- Uninterruptible Power Supplies
- Energy Storage
- Server SMPSs

High Voltage

Warning: Although this board is designed to satisfy safety requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1.4. System Description

This converter is comprised of a main PCB and four daughter boards. Figure 1 shows a general hardware diagram.

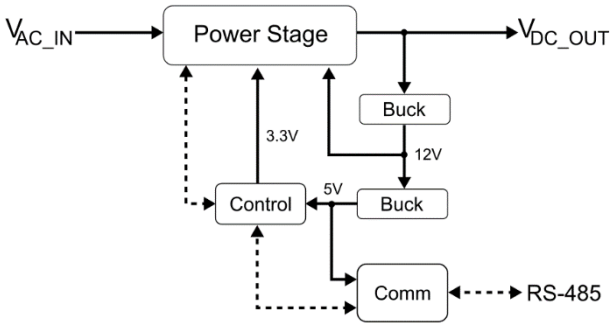


Figure 1: Hardware Diagram

Figure 2 shows a simplified circuit of the totem pole (TP).

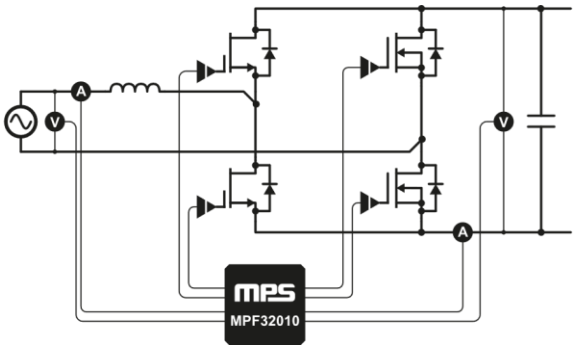


Figure 2: TP Simplified Circuit

The main components of the power stage include an inductor, capacitor, and a controlled full bridge. The branch of the full bridge that is connected to the coil has SiC devices that switch at a high frequency (65kHz). The switches on the lower frequency branch, which commutates at grid frequency, could be implemented with diodes, but Si transistors are recommended due to their lower conduction losses.

The TP PFC behaves as a boost converter in which the SiC devices are activated complementarily, and the Si devices are used as a return path for the current. For a more detailed explanation of the converter's operation, refer to the MPF32010 datasheet.

When compared to an interleaved boost PFC, TP has four semiconductor devices instead of eight. Out of these four devices, current only flows through two devices at any given moment, whereas the interleaved boost PFC has three elements conducting simultaneously. This is why TP has better overall efficiency.

Cascodes from UnitedSiC were selected for the fast-switching branch because they offer very good performance in terms of losses, reverse recovery, and more. Furthermore, they don't require a negative voltage to switch off. Therefore, only a 12V auxiliary voltage is required to drive all transistors (a high-side supply voltage is obtained when the drivers work in bootstrap operation). This simplicity improves the system's robustness and reduces board space. Because the input voltage is sensed with voltage dividers, there is no need to add comparator circuity in order to detect polarity. Instead, this is achieved with the controller's phase-locked loop (PLL).

1.5. Related Solutions

This reference design is based on the following MPS solutions:

Table 1: MPS ICs

MPS Integrated Circuit	Description
MPF32010	Totem-pole controller
MP18831-4CGY	Half-bridge driver
MCS1802GS-10	DC current sensor

2. Specifications

2.1. Electrical Specifications

Table 2: Electrical Input Specifications

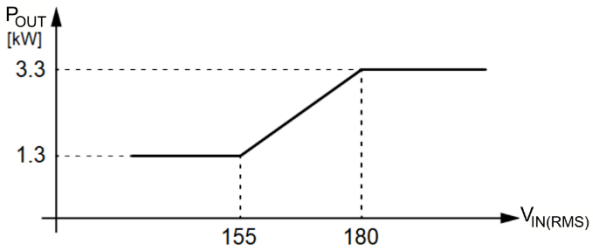
Parameter	Min	Typ	Max	Unit	Remarks
Voltage	80	230	250	V_{AC}	-
Frequency	45	50	66	Hz	-
Current	-	-	19.6	A	-
Power factor	0.99	-	-	-	Nominal conditions
Efficiency	0.985	-	-	%	Nominal conditions
Derating					-

Table 3: Electrical Output Specifications

Parameter	Min	Typ	Max	Unit	Remarks
Voltage	-	400	-	V_{DC}	-
Ripple	-	12.5	-	V	Nominal conditions
Power	-	3	3.3	kW	-
Line regulation	-	0.02	-	%	-
Load regulation	-	0.4	-	%	-

Table 4: Protections

OT	Over-temperature
OL	Overload
OC	Over-current (input and output)
UV	Under-voltage (input and output)
OV	Over-voltage (input and output)

Table 5: Standards

Harmonic Current	IEC 61000-3-2:2018+AMD1 (Class A)
Conducted Emissions	CISPR 32:2015+AMD1 (Class A)
Voltage Sag	IEC 61000-4-11:2020

2.2. Mechanical Specifications

Table 6: Mechanical Specifications

Cooling	Controlled fan based on temperature and power delivery
Weight	<3.2kg
Dimensions	195mmx127.5mmx108mm

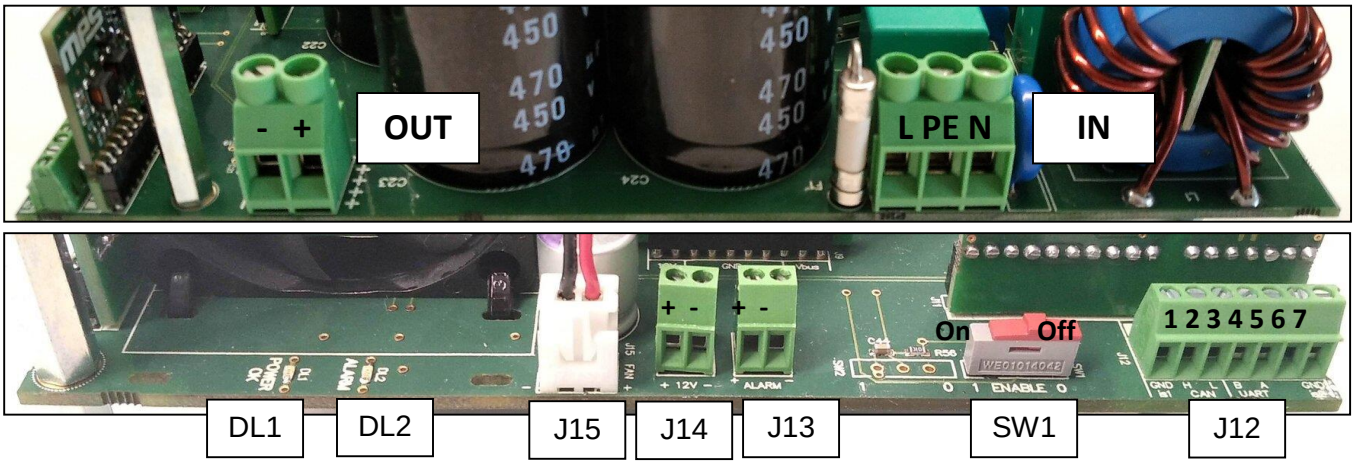


Figure 3: Connectors and LEDs

Table 7: Connectors and LEDs Description

Connector	Description
DL1	Power OK LED
DL2	Alarm LED
J15	Connector used to power the fan
J14	Checks the auxiliary voltage using a $12V_{AUX}$ connector
J13	Alarm connector (3.3V if asserted) • Used to trigger a circuit breaker if needed (not isolated from power)
SW1	Power ON/OFF switch
J12	Communications connector (isolated from power) • CAN: 1 GND 2 H 3 L • RS-485: 4 B 5 A 7 GND

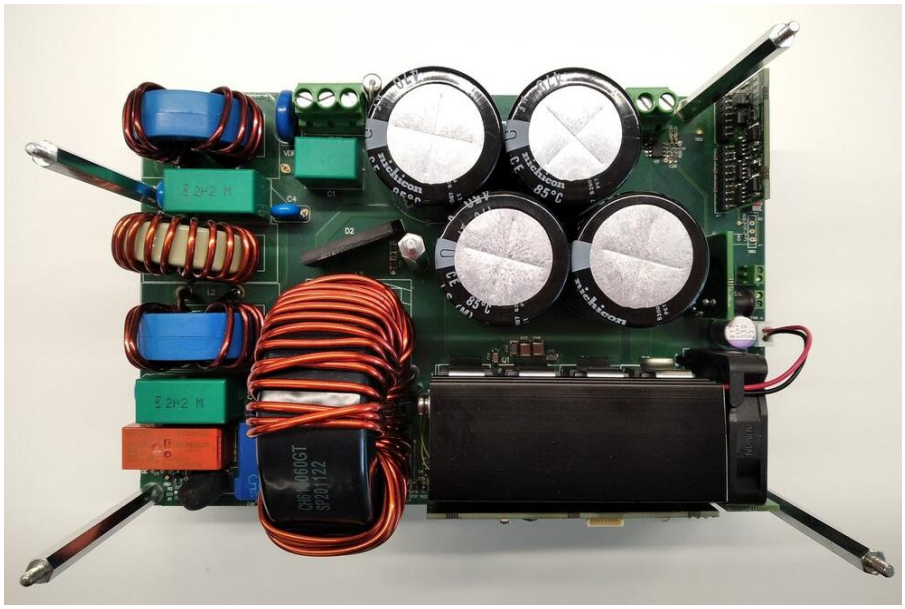


Figure 4: The EVF32010-18831

2.3. Communication Specifications

Users can use the Virtual Bench Pro 4.0 tool to read and write to the memory map via a proprietary communication protocol implemented using the RS-485 standard. For remote programming, the controller can be configured through a non-compliant Modbus RTL protocol. The register map is organized in pages and grouped by functionalities. Table 8 shows the access addresses.

Table 8: Access Addresses

Type	Page	Boundary Address	Registers Size (Bytes)	Access	Group
Holding register	0	0x0000~0x001F	2 (unit 16)	R/W	General settings
	1	0x0000~0x000F	4 (float 32)		Protections
	2		4 (float 32)		Calibration
	3		4 (float 32)		Controller
Input register	0		4 (mixed unit, float 32)	R	Information

Figure 5 shows a read request and response for holding input registers. Refer to the related datasheet for more information.

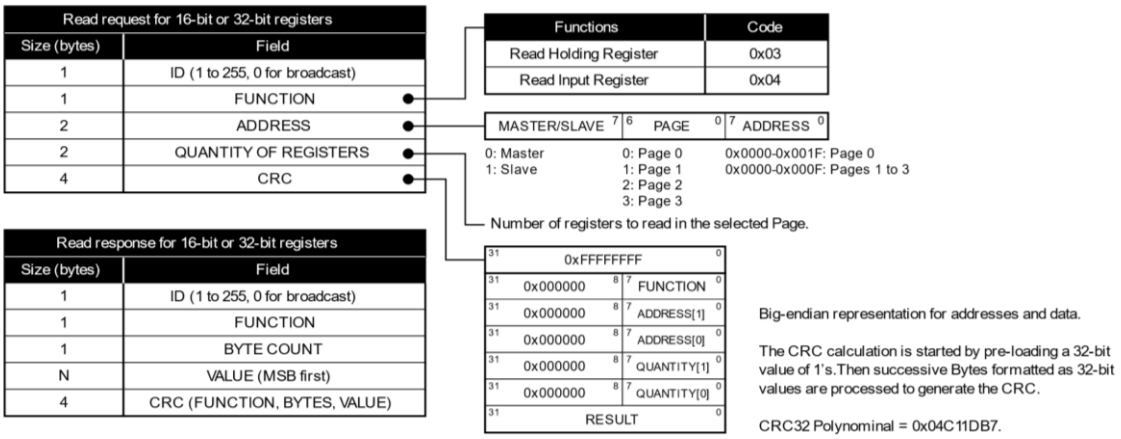


Figure 5: Read Request and Response for Holding

Figure 6 shows a write request for holding. Refer to the related datasheet for more information.

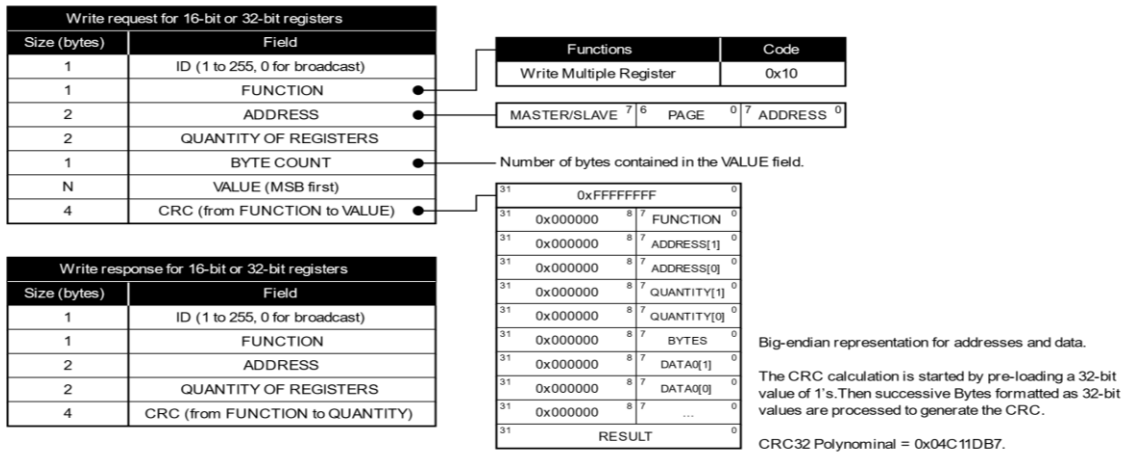


Figure 6: Write Request for Holding

3. Hardware Design

3.1. Selecting the Output Capacitor

The output capacitance has to deliver part of its stored energy when the instantaneous input power is below the power demanded by the load. At this time, the output voltage decreases. The capacitor is charged again when the instantaneous input power exceeds the output power. This cycle explains why the PFC's output ripple frequency is double that of the grid frequency (see Figure 7).

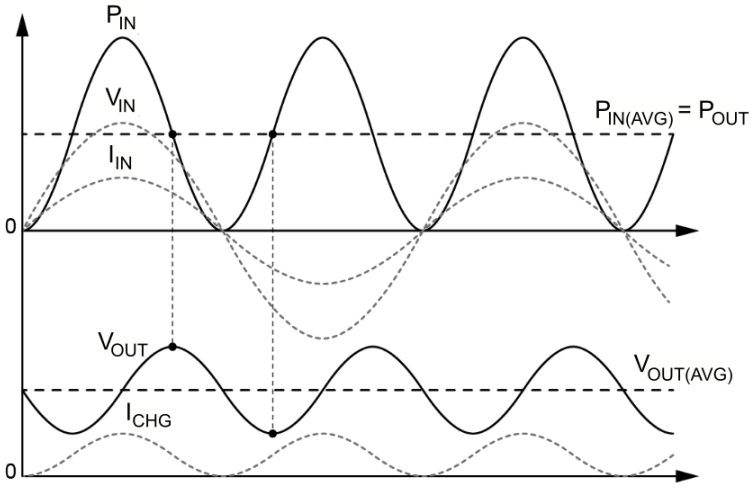


Figure 7: TP Instantaneous Power and Output Voltage (Excluding Losses)

The capacitance can be calculated with the output voltage ripple and/or the withstand time. The output voltage ripple is limited to 15V. The minimum value of the input capacitor (C) can be estimated with Equation (1):

$$C > \frac{P_{OUT}}{2\pi f_{GRID} \times V_{OUT} \times \Delta V_{OUT}} \rightarrow C > \frac{3000}{2\pi 50 \times 400 \times 15} = 1.59mF \quad (1)$$

For this reference design, four 470µF capacitors were used to a total of 1.88mF. This means that the final output voltage ripple is about 12.7V. The hold-up time (t_{HOLD}) can be calculated with Equation (2):

$$t_{HOLD} = \frac{C(V_{OUT}^2 - V_{OUT(MIN)}^2)}{2P_{OUT}} \rightarrow \underline{t_{HOLD}} = \frac{4 \times 470\mu F \times (400^2 - 340^2)}{2 \times 3000} = \underline{13.9ms} \quad (2)$$

The converter only allows grid power interruptions for about half a grid period. The RMS current (I_{C_RMS}) flowing through the capacitors can be calculated with Equation (3):

$$I_{c_{rms}} = \sqrt{\frac{8\sqrt{2} \times P_{OUT}^2}{3\pi \times V_{IN} \times V_{OUT}} - \frac{P_{OUT}^2}{V_{OUT}^2}} \rightarrow \underline{I_{C\_RMS}} = \sqrt{\frac{8\sqrt{2} \times 3000^2}{3\pi \times 230 \times 400} - \frac{3000^2}{400^2}} = \underline{7.82A} \quad (3)$$

The equivalent series resistance (ESR) can be estimated with the manufacturer dissipation factor (DF) in Equation (4):

$$ESR = \frac{DF}{2\pi(2 \times f_{GRID})C} \rightarrow \underline{ESR} = \frac{0.2}{2\pi \times 2 \times 50 \times (4 \times 470\mu F)} = \underline{169m\Omega} \quad (4)$$

The capacitor loss (P_C) can be calculated with Equation (5):

$$P_C = I_{C\_RMS}^2 \times ESR \rightarrow \underline{P_C} = 7.82^2 \times 0.169 = \underline{10.36W} \quad (5)$$

3.2. Selecting the PFC Inductor

A lower current ripple improves performance regarding core losses and EMC. A current ripple that is 16% of the maximum input current has been selected, calculated using Equation **Error! Reference source not found.**:

$$\Delta I_L = k \times \frac{P_{OUT}}{\eta \times V_{IN\_MIN}} \times \sqrt{2} \rightarrow \underline{\Delta I_L} = 0.16 \times \frac{3000}{0.98 \times 180} \times \sqrt{2} = \underline{3.85A} \quad (6)$$

Where the current ripple is set to be 16% of the maximum input current.

The inductance (L) that is required to limit the current ripple can be calculated with Equation (7):

$$L = \frac{V_{IN\_MIN\_PK} \times (V_{OUT} - V_{IN\_MIN\_PK})}{f_{SW} \times V_{OUT} \times \Delta I_L} \rightarrow \underline{L} = \frac{180\sqrt{2} \times (400 - 180\sqrt{2})}{65000 \times 400 \times 3.85} \approx \underline{370\mu H} \quad (7)$$

A toroid CH610060GT core was selected for this reference design. Table 9 shows the core data for this component. (1)

Table 9: Core Data

A_L (nH/T^2)	MPL (cm)
192	14.37

Note:

1) For more details, refer to http://changsung.com/file/product/cores/1.%20High%20Flux%20GT%20cores/TDS_CH610060GT.pdf.

The required number of turns (n) can be estimated with Equation (8):

$$n = \sqrt{\frac{L}{A_L}} \rightarrow \underline{n} = \sqrt{\frac{370\mu H}{0.192\mu}} \approx \underline{44} \quad (8)$$

The number of turns were calculated without considering the flow of current through the coil. Therefore, up to 52 turns should be wound to compensate for the DC bias. The inductance without current (L_{0A}) can be estimated with Equation (9):

$$L_{0A} = A_L \times n^2 \rightarrow \underline{L_{0A}} = 0.192\mu \times 52^2 = \underline{519\mu H} \quad (9)$$

To calculate the inductance at the maximum current, the magnetic force (H) must be calculated. H can be estimated with Equation (10):

$$H = \frac{0.4 \times \pi \times n \times I_{IN\_MAX\_PK}}{MPL} \rightarrow \underline{H} = \frac{0.4 \times \pi \times 52 \times \frac{3000}{0.98 \times 180} \times \sqrt{2}}{0.1437} = 10937 \ \frac{A}{m} = \underline{137.44Oe} \quad (10)$$

Then, the real inductor permeability can be calculated using Equation (11):

$$\%Perm = \frac{1}{a + b \times H^c} \rightarrow \underline{\%Perm} = \frac{1}{0.01 + 1.46 \times 10^{-8} \times 137.44^{2.552}} = \underline{70.54} \quad (11)$$

The biased inductance (L_{BIAS}) can be calculated with Equation (12):

$$L_{BIAS} = \%Perm \times L_{0A} \rightarrow \underline{L_{BIAS}} = 0.7054 \times 519\mu H = \underline{366\mu H} \quad (12)$$

The inductance calculated in Equation (7) is almost equal to the biased inductance calculated in Equation (12).

For the complete drawing of the inductor (and all manufacturer information), see Figure 74 on page 60.

3.3. Low-Frequency Switches

The transistors that switch at the grid frequency were selected with very low $R_{DS(ON)}$ value to reduce conduction losses as much as possible. Note that switching losses can be neglected.

Figure 8 shows the relationship between T_J and $R_{DS(ON)}$. With a junction temperature of about 50°C, $R_{DS(ON)}$ = 18mΩ is obtained using the datasheet:

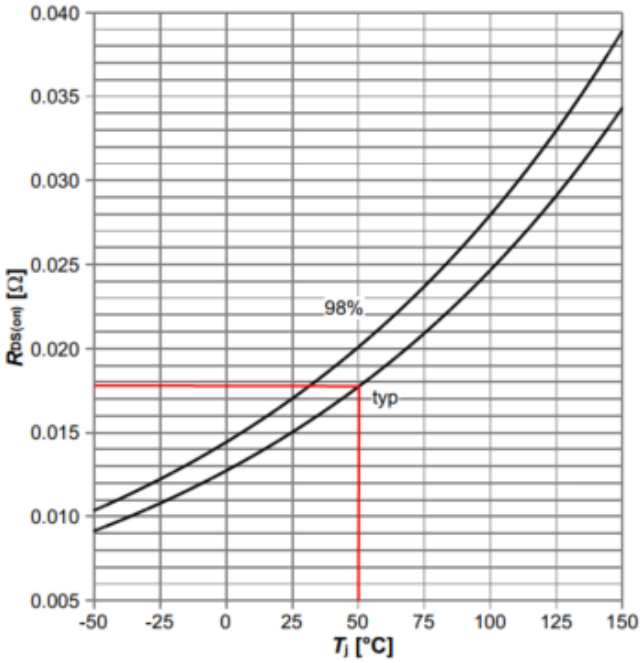


Figure 8: $R_{DS(ON)}$ vs. Temp

Each transistor conducts for half of a grid period. The RMS current value during one cycle ($I_{Q\_LF\_RMS}$) can be calculated with Equation (13):

$$I_{Q\_LF\_RMS}=\frac{I_{IN\_MAX\_RMS}}{\sqrt{2}} \rightarrow I_{Q\_LF\_RMS}=\frac{\frac{3000}{0.98\times180}}{\sqrt{2}}=12A \quad (13)$$

The conduction loss (P_{Q_LF}) on one transistor can be estimated with Equation (14):

$$P_{Q\_LF}=I_{Q\_LF\_RMS}^2\times R_{DS(ON)} \rightarrow P_{Q\_LF}=12^2\times18m=2.6W \quad (14)$$

The power loss (P_{LEG_LF}) during the low-frequency branch can be calculated with Equation (15):

$$P_{BRANCH(LF)}=2\times P_{Q\_LF} \rightarrow P_{BRANCH(LF)}=2\times2.6=5.2W \quad (15)$$

3.4. High-Frequency Switches

A SiC cascode from UnitedSiC was selected to implement the high-frequency switching branch. This particular cascode has very good performance, and it simplifies the hardware because it does not need a negative voltage to be applied to the gate.

Losses can be calculated with the UnitedSiC online tool (see Figure 9 on page 12). (2) The SiC device's losses are 17.1W. However, since a snubber was added in each cascode, the total losses are higher. (3)

Notes:

2) For more details, refer to https://unitedsic.com/fet-jet/.
3) For more details, refer to https://unitedsic.com/appnotes/Snubber%20AppNotes_V8.pdf.

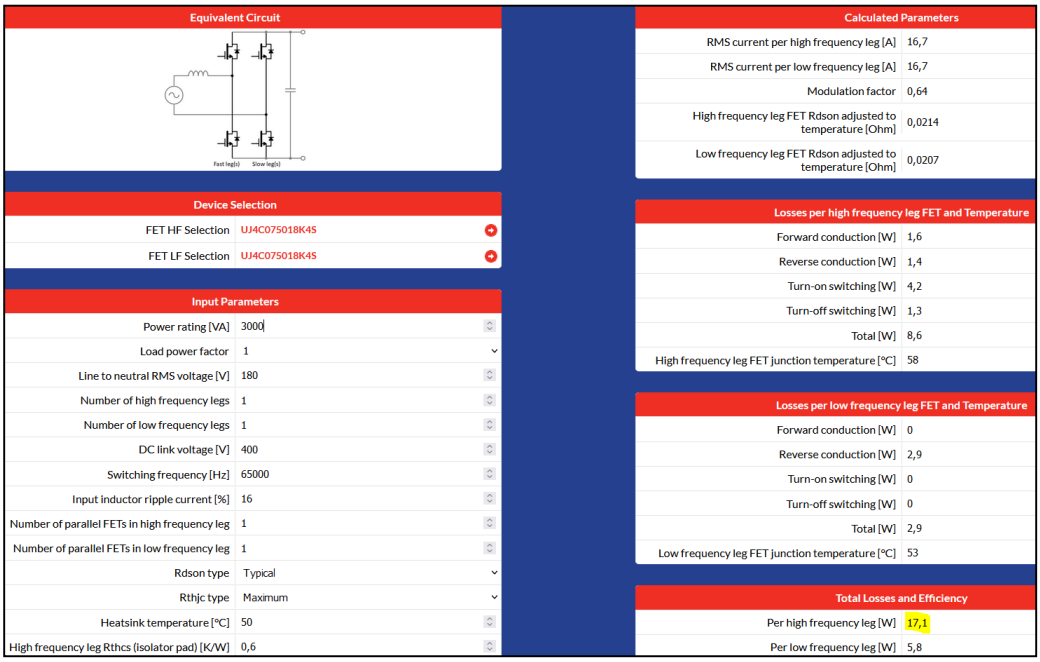


Figure 9: High-Frequency Losses

3.5. Input Current Sense

For this reference design, the CAS 25-NP from LEM was selected as the current sensor. The supply voltage is 5V, so the sensor output is 2.5V when there is no current flow. The 2.5V output was shifted to 1.65V to match the ADC's voltage levels using an operational amplifier (see Figure 10). (4)

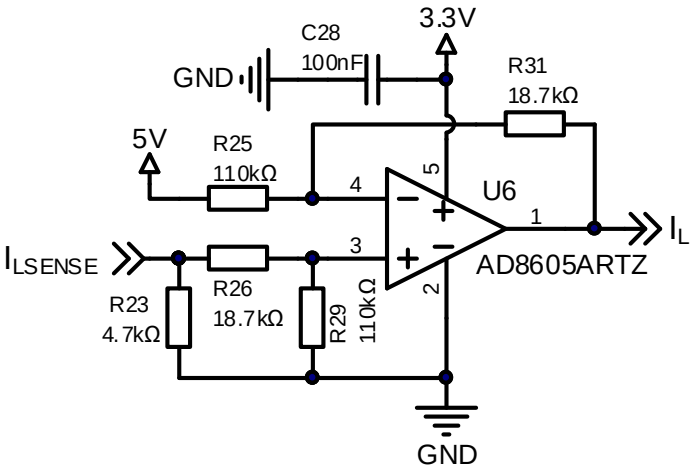


Figure 10: Input Current-Sense Signal Condition

Note:

4) For more details, refer to https://www.allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/shifting-the-offset-voltage-of-current-sensors.

If R_{25} and R_{29} are set to 110kΩ, R_{26} and R_{31} can be calculated with Equation (16):

$$R_{26}=R_{31}=\frac{V_{SHIFT}}{V_{CC}}\times R_{25} \rightarrow R_{26}=R_{31}=\frac{2.5-1.65}{5}\times 110k\Omega=18.7k\Omega \quad (16)$$

Due to tolerances, the final output voltage may not be exactly 1.65V, so auto-zero trimming is initiated each time the converter starts up. This feature can be disabled.

The maximum current as an absolute value ($|I_{MAX}|$) can be estimated with Equation (17):

$$\boxed{|I_{MAX}| = \left(V_{ADC\_MAX} - V_{SENSOR}(0A)\right)/\text{Sensitivity}} \rightarrow \underline{|I_{MAX}|} = (3.3-1.65)/0.025 = \underline{66A} \quad (17)$$

Another turn to the primary can be added to double the sensitivity and reduce the noise/signal ratio. However, this would reduce the current range, which could result in safety issues when the voltage sags.

The power losses (P) can be calculated with Equation (18):

$$\underline{P} = I_{IN\_RMS}^2 \times R = \left(\frac{P_{OUT}}{\eta \times V_{IN\_RMS}}\right)^2 \times R = \left(\frac{3000}{0.98 \times 230}\right)^2 \times 0.24m\Omega = \underline{42.5mW} \quad (18)$$

3.6. Output Current Sense

The MCS1802GS-10 Hall sensor measures the output current. The maximum DC current (I_{OUT_MAX}) can be estimated with Equation (19):

$$\underline{I_{OUT\_MAX}} = P_{OUT\_MAX}/V_{OUT} = 3300/400 = \underline{8.25A} \quad (19)$$

The sensor can measure up to ±10A, so the losses in the sensor can be calculated with Equation (20):

$$\underline{P} = I_{IN\_RMS}^2 \times R = (P_{OUT}/V_{OUT})^2 \times R = (3000/400)^2 \times 0.9m\Omega = \underline{50mW} \quad (20)$$

3.7. Selecting the NTC

When selecting the NTC, calculate the energy (E) required to charge the bulk capacitor with Equation (21):

$$\underline{E} = \frac{1}{2}CV^2 = \frac{1}{2} \times 4 \times 470\mu F \times \left(230\sqrt{2}\right)^2 = \underline{99.45J} \quad (21)$$

After calculating E, the MS15 30004 current limiter was selected (up to 135J). This device has a 30Ω resistance, so the maximum current (I_{P_NTC}) that flows through it can be calculated with Equation (22):

$$\underline{I_{P\_NTC}} = 230\sqrt{2}/30 = \underline{10.8A} \quad (22)$$

Based on Equation (22), a 20A fuse was selected.

3.8. Temperature Sense

An NTC (NTCALUG02A103G) senses the heatsink temperature, which ranges between 40°C and 100°C. When the heatsink temperature is between these values, the fan is activated. If the temperature reaches 90°C, the converter is switches off (see Figure 11 on page 14). This threshold value can be modified via the GUI.

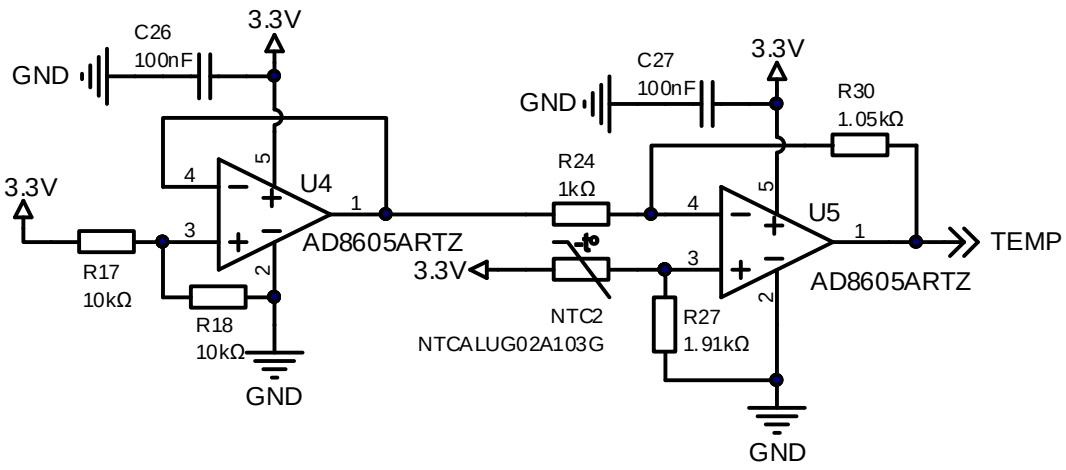


Figure 11: Temperature Signal Conditioning

Figure 11 shows how a resistor (R_{27}) can be placed in series with NTC2 to linearize NTC2's usable range. R_{27} can be calculated with Equation (23):

$$\underline{R_{27}}=\sqrt{R_{NTC\ 40ºC}\times R_{NTC\ 100ºC}}=\sqrt{5324\times 674.1}=1894\Omega\approx\underline{1.91k\Omega} \quad (23)$$

The voltage divider formed by NTC2 and R_{27} create minimum (V_{IN_MIN}) and maximum (V_{IN_MAX}) input voltages, estimated with Equation (24) and Equation (25), respectively:

$$V_{IN\_MIN}=V_{cc}\times\frac{R_{27}}{R_{NTC\ 40ºC}+R_{27}}=3.3\times\frac{1.91k\Omega}{5324+1.91k\Omega}=0.87V \quad (24)$$

$$V_{IN\_MAX}=V_{cc}\times\frac{R_{27}}{R_{NTC\ 100ºC}+R_{27}}=3.3\times\frac{1.91k\Omega}{674.1+1.91k\Omega}=2.44V \quad (25)$$

This output voltage range is amplified to improve the accuracy of the ADC reading. The amplification gain (Gain) can be calculated with Equation (26):

$$Gain=\frac{\Delta V_{OUT}}{\Delta V_{IN}}=\frac{3.25-0.05}{2.44-0.87}=2.04 \quad (26)$$

The amplification is implemented using an operational amplifier (U5) in a non-inverting amplifier configuration. The gain can be estimated with Equation (27):

$$Gain=1+\frac{R_{30}}{R_{24}} \quad (27)$$

Where R_{24} = 1kΩ, and R_{30} can be calculated with Equation (28):

$$\underline{R_{30}}=R_{24}\times(Gain-1)=1k\Omega\times(2.04-1)=1.04k\Omega\approx\underline{1.05k\Omega} \quad (28)$$

The final gain from U5 can be found using R_{30} and R_{24}, calculated with Equation (29):

$$Gain=1+\frac{R_{30}}{R_{24}}=1+\frac{1.05k\Omega}{1k\Omega}=2.05 \quad (29)$$

The maximum output voltage (V_{OUT_MAX}) can be calculated with Equation (30):

$$V_{OUT\_MAX}=\frac{V_{CC}}{2}+\frac{\Delta V_{OUT}}{2}=\frac{V_{CC}+\Delta V_{IN}\times Gain}{2}=\frac{3.3+(2.44-0.87)\times 2.05}{2}=3.26V \quad (30)$$

To obtain V_{OUT_MAX}, an offset must be introduced in the circuit. The value of this reference voltage can be found by applying the superposition principle, as calculated with Equation (31 and Equation (32):

$$V_{OUT\_MAX}=V_{IN\_MAX}\times Gain-\frac{R_{30}}{R_{24}}\times V_{REF}\rightarrow V_{REF}=\frac{R_{24}}{R_{30}}\times\left(V_{IN\_MAX}\times Gain-V_{OUT\_MAX}\right) \quad (31)$$

$$\underline{V_{REF}} = \frac{R_{24}}{R_{30}} \times \left(V_{IN\_MAX} \times Gain - V_{OUT\_MAX}\right) = \frac{1k\Omega}{1.05k\Omega} \times (2.44 \times 2.05 - 3.26) = 1.66V \approx \underline{1.65V} \quad (32)$$

The reference voltage is obtained using a resistive voltage divider. R_{17} and R_{18} are equal to one another, which cuts the 3.3V voltage in half (1.65V). The operational amplifier (U4) can be implemented as a voltage follower or, in other words, a non-inverting buffer.

The temperature readings obtained from the sensing circuitry trigger over-temperature protection (which can be configured via the OT register) and to set the fan's spinning speed. The fan spins at its maximum speed when the NTC's temperature exceeds 60°C. Otherwise, its speed is proportional to the output current. The minimum duty cycle can be defined in the FAND register.

4. Control Design

Set the parameters securely by using the provided GUI tool. Before testing the evaluation board, set safe operation conditions by configuring accurate measurements, safe electrical limits, and coherent control loop parameters. The MPF32010 is a totem-pole PFC controller that operates in continuous conduction mode (CCM). It is governed by an average current mode (ACM) control scheme. Figure 12 shows the dual control loop.

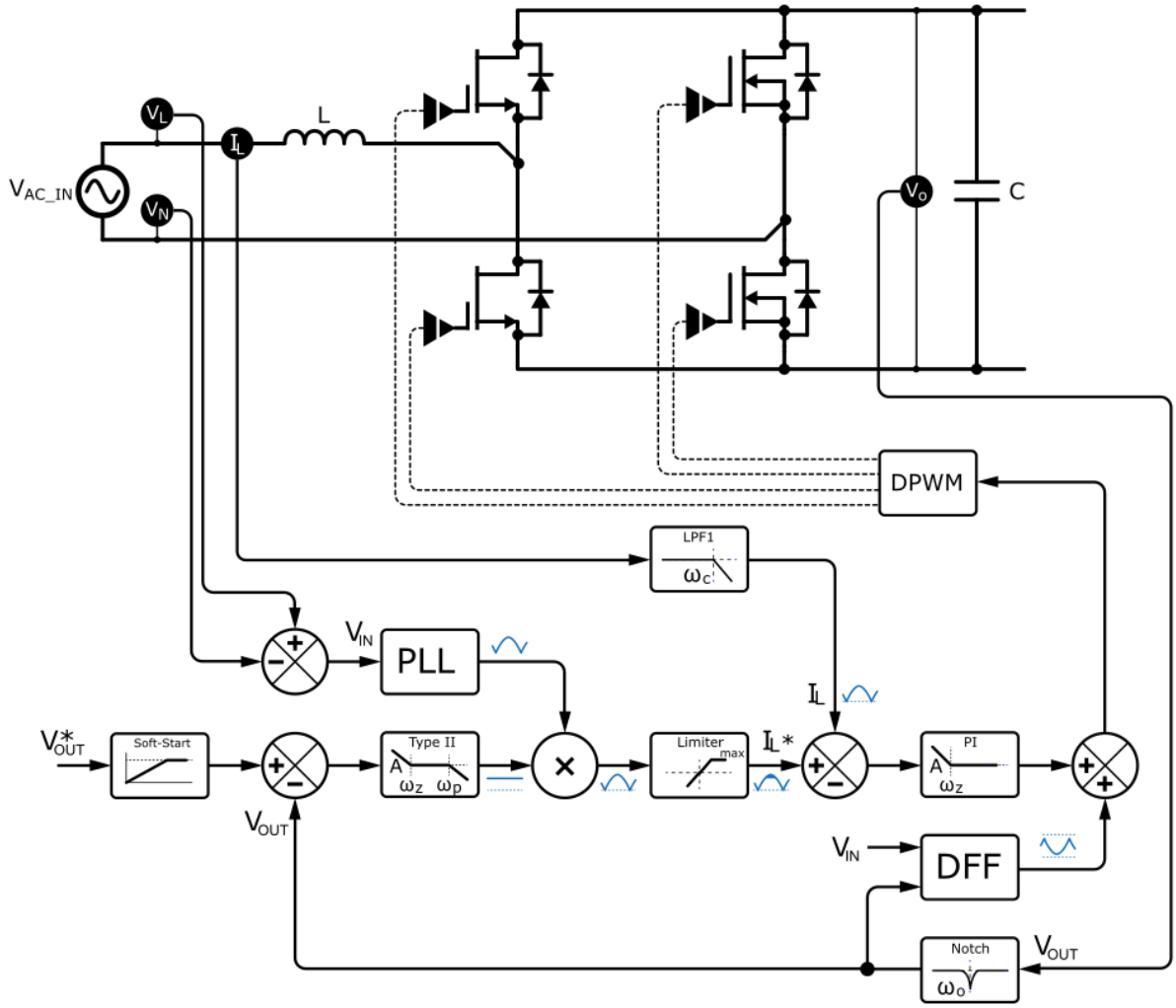


Figure 12: PFC Average Current Mode Control

The first parameter to set in the controller is the switching frequency (f_{SW}). f_{SW} also defines the time period for the digital control algorithm. If f_{SW} is changed, it must be saved in the internal memory before the control card is reset.

Table 10: Switching Frequency and Control Period

Parameter	Description	Value	Units
Switching frequency	Defines the PWM switching frequency and sets the control algorithm's execution time (0.5 x f_{SW}).	65	kHz

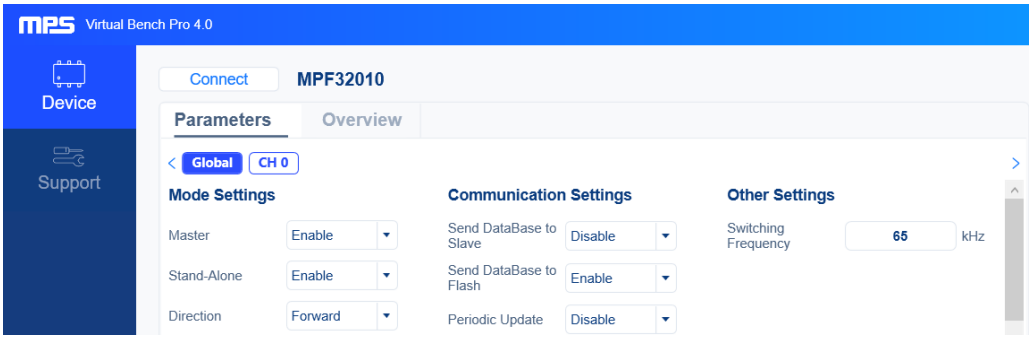
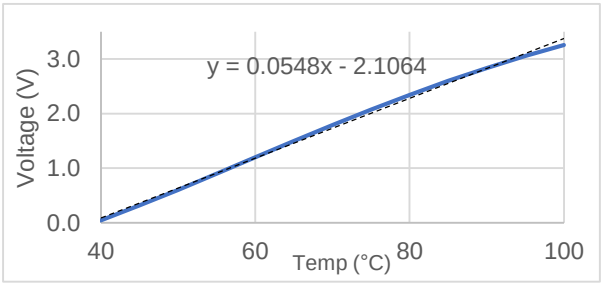


Figure 13: Update f_{SW} via the GUI

4.1. Calibration

The calibration registers are used for linear signal conditioning for gain and offset compensation. The calibration registers scale the sensed input voltages to their real magnitudes. The gain is determined by the inverse of the sensitivity of its respective transducer and conditioning circuit (see Table 11).

Table 11: Calibration Parameters

Parameter	Conditioning	Gain	Offset
Input line voltage Input neutral voltage Output voltage	$Gain=\frac{V_{IN}}{V_S}=\frac{\sum R}{R_S}=\frac{664.7k\Omega}{4.7k\Omega}=141.42$	141.42	0
Inductor current	$Gain=\frac{1}{G_{TH}}=\frac{1}{25mV/A}=40$ Offset=1.65	40	1.65
Output current	$Gain=\frac{1}{G_{TH}}=\frac{1}{132mV/A}=7.5758$ Offset=1.65	7.5758	1.65
Temperature	Gain=1/0.0548=18.248 	18.248	-2.1064

To improve accuracy, fine-tune the parameters by comparing the values from the monitoring window in the GUI to the values obtained by external instruments. The controller includes an auto-zero function for the current channels. When this feature is enabled, the offset registers are overwritten during start-up.

Figure 14 shows how to set the calibration values using the GUI .

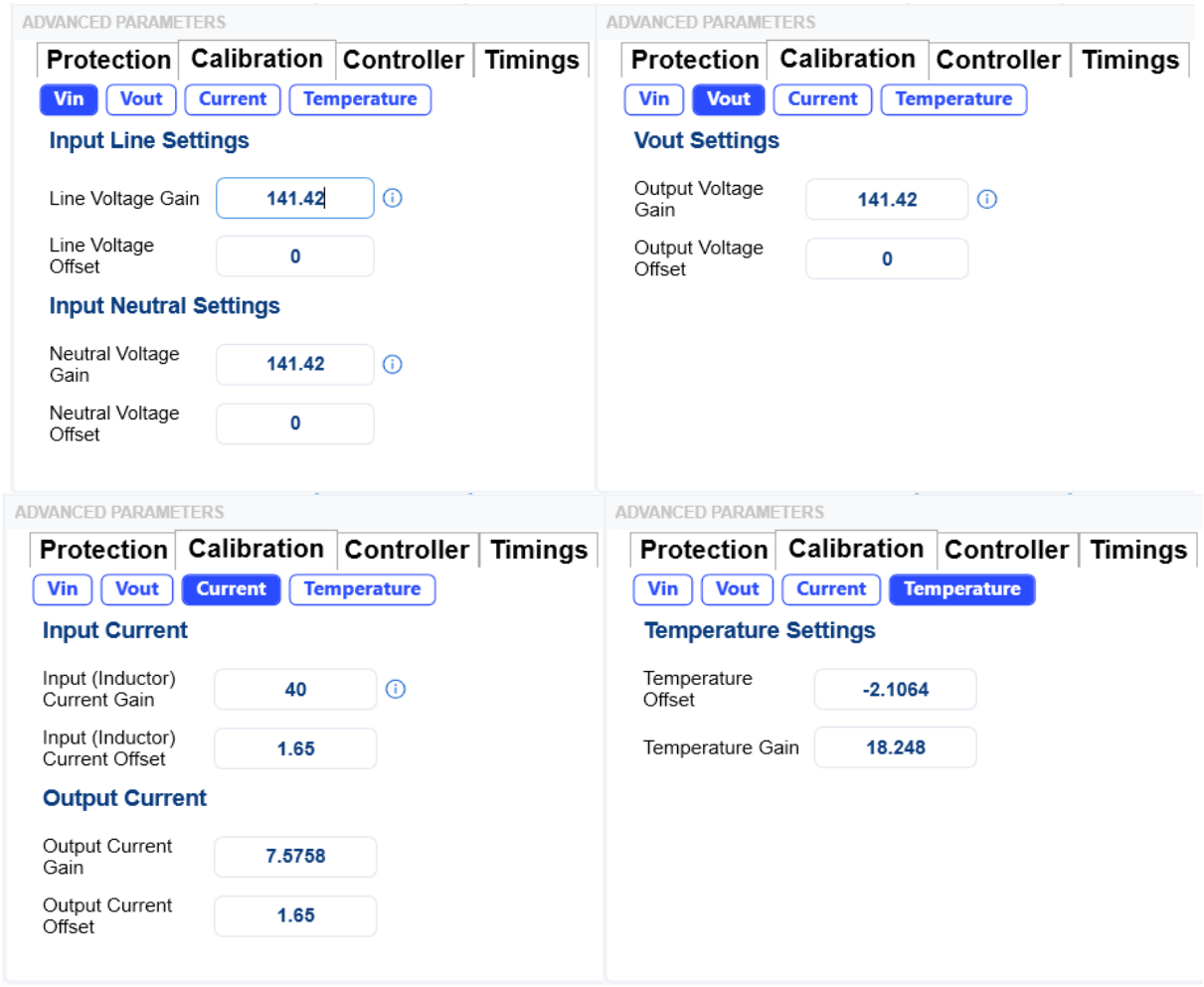


Figure 14: Using the GUI to Set the Calibration Values

4.2. Protections

This controller provides input and output over-voltage (OV), under-voltage (UV), over-current (OC), and temperature protections. These protections set safe operation conditions for the PFC and prevent damaging the load and converter parts. For a more detailed description, refer to the related datasheet.

Because limits depend on the electrical properties of the converter, refer to the datasheet's Electrical Specifications section. Table 12 on page 19 shows the threshold values for critical protections such as OV and UV conditions which, if passed, may stop the converter's switching operation.

Table 12: Critical Protections

Parameter	Description	Threshold Value	Units
Input under-voltage lockout on	Minimum operation input voltage. The response of this protection may be delayed by the voltage sag protection.	80	V_{RMS}
Input under-voltage lockout off		90	V_{RMS}
Input over-voltage	Maximum input voltage.	370	V_{PK}
Output over-voltage	Maximum output voltage, which protects the output capacitors.	450	V
Output under-voltage margin	Minimum output voltage to prevent diode rectification. The output voltage ripple must be considered before setting this value.	15	V
Average input over-current	Maximum average input current amplitude. It keeps current at a safe level for the power switches.	55	A
Input over-current level	Sets a value for an external comparator to fast stop the switching operation if the input current overpasses the threshold (disabled by default on this kit).	3.2	V
Output over-current	Maximum output current. The output ripple must be considered before setting this value.	15	A
Over-temperature	Maximum temperature measured in the NTC sensor placed on the power switches heatsink.	90	°C

Table 13 shows non-critical protections. These protections protect the converter while allowing it to operate normally.

Table 13: Non-Critical Protections

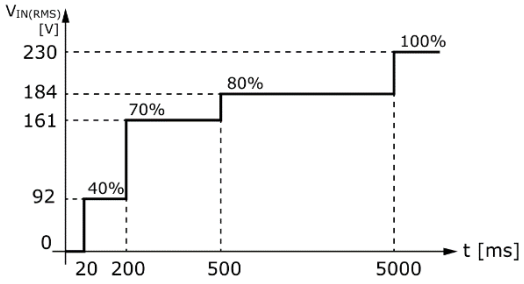
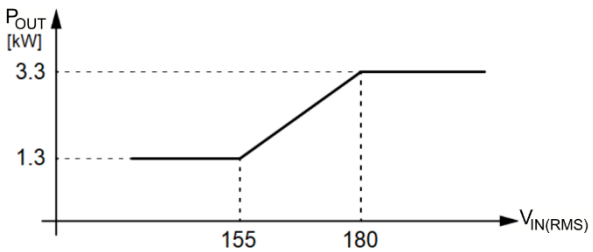
Parameter	Description	Value	Units
Sag voltage level	The voltage sag is defined in IEC61000-4-11 Class 3. See the figure below for more details.	0, 92, 161, 18	V_{RMS}
Sag time delay level		20, 200, 500, 5000	ms
Reference output current	Clamping current. This protection is triggered when the instantaneous value of the input current overpasses this level.	42	A
Power derating limit low		1300	W
Power derating limit high ($P_{O(MAX)}$)		3300	W
Power derating voltage limit low		155	V
Power derating voltage limit high		180	V

Figure 15 and Figure 16 on page 20 show how to configure critical and non-critical protections.

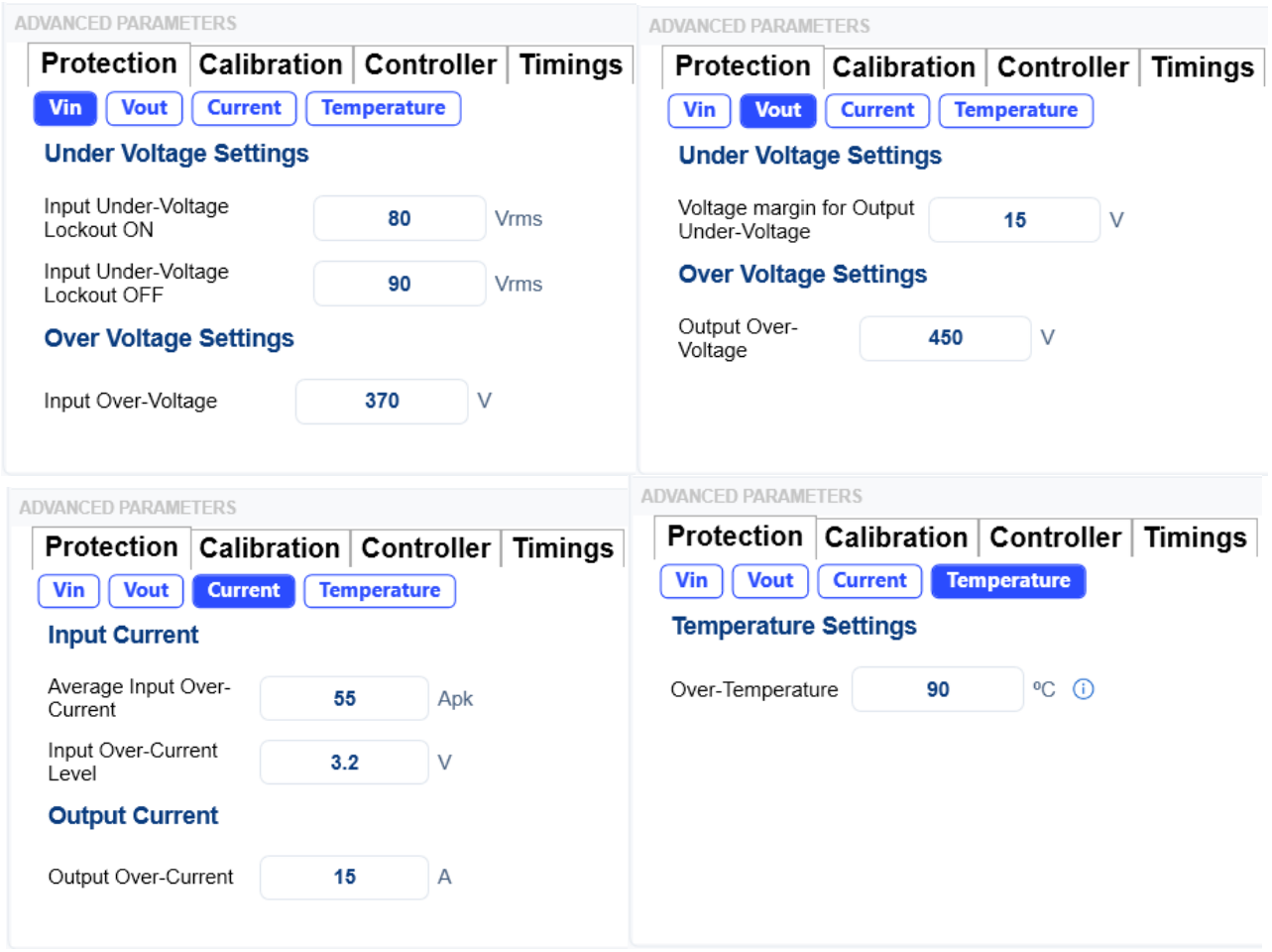


Figure 15: Using the GUI to Set Critical Protections

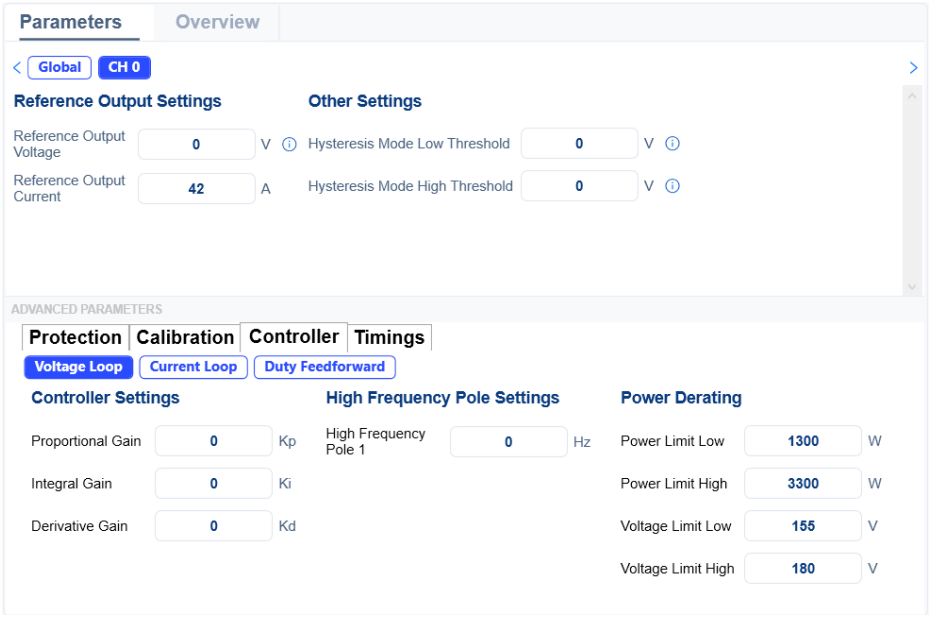
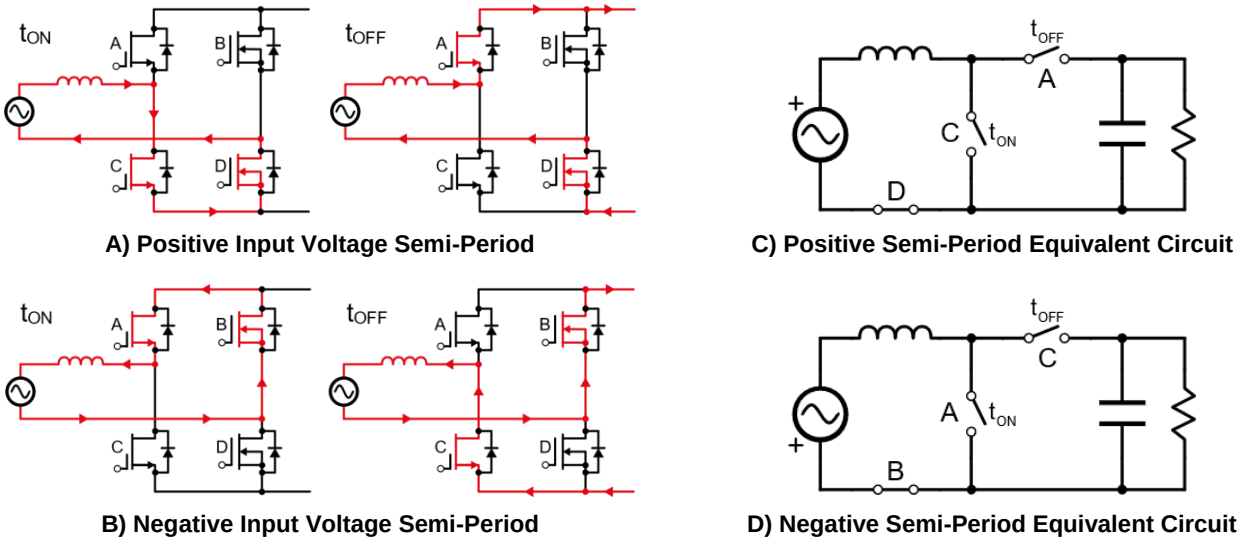


Figure 16: Using the GUI to Set Non-Critical Protections

4.3. Modulation

A PFC totem pole is a full-bridge topology that uses different switching modulations for each half-bridge branch. The modulation of the first branch depends on the ACM control scheme. The modulation of the second branch and the switch configuration depend on the input voltage polarity. The transition between these two configurations is responsible for high-current spikes (see Figure 17). To solve this issue, the controller combines an off time for all switches and initiates a soft start when switching operation resumes.



A) Positive Input Voltage Semi-Period

C) Positive Semi-Period Equivalent Circuit

B) Negative Input Voltage Semi-Period

D) Negative Semi-Period Equivalent Circuit

Figure 17: Totem-Pole Switch Configurations

Table 14: Totem-Pole Modulation Settings

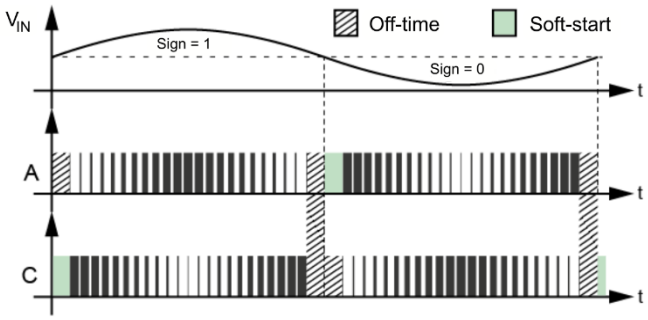
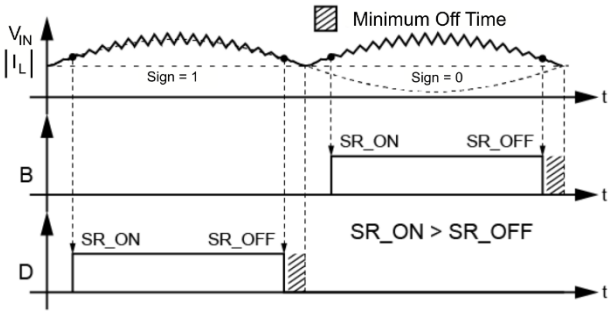
Parameter	Description	Value	Units
Dead time	Sets an off time to prevent shoot-through if the switches turn on too early during a high-frequency leg.	160	ns
Zero cross-off time	Sets an off-time period for all switches before a zero-crossing condition. Also sets the soft-start duration for the high-frequency half-bridge branch. 	100	µs
Synchronous rectifier enabled (SR_ON)	Sets the current level at which the power switches in the slow half-bridge branch turn on and off. 	3.5	A
Synchronous rectifier disabled (SR_OFF)		3.2	A

Figure 18 shows how to set totem-pole modulation settings via the GUI.

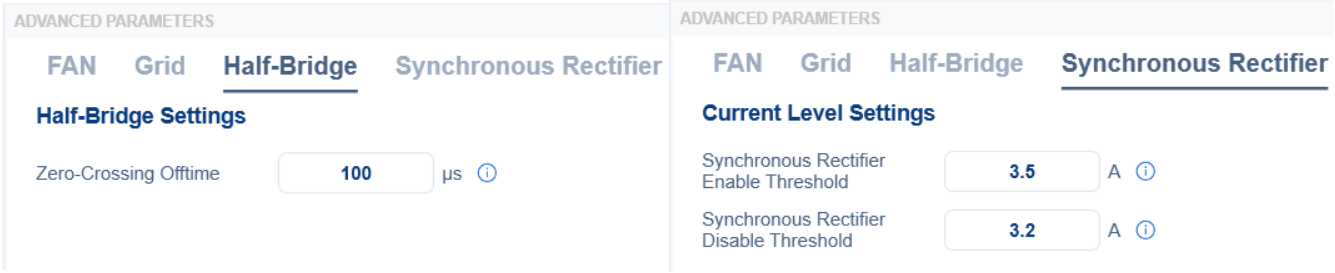


Figure 18: Using the GUI to set Totem-Pole Modulation Settings

4.4. Current Loop

The current loop is the fastest and innermost loop in the dual control loop scheme. The current loop is responsible for tracking the inductor current, generating a sinusoidal shape in phase with the input voltage, and showing the resistive behavior of the converter's input impedance. The goal is to establish a stable control loop with excellent dynamic performance. Therefore, selecting the right parameters for the current loop is vital to obtaining high power factors and low harmonic distortion.

The design of the current loop is based on the stability criteria from the linear control theory. First analyze the open loop transfer function (see Figure 19).

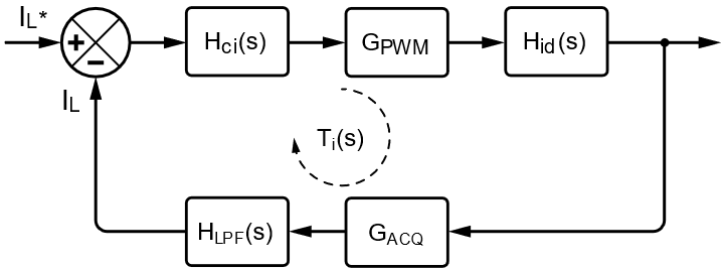


Figure 19: Current Loop

Table 15 lists the elements from Figure 19.

Table 15: Current Loop Parameters

Symbol	Parameter	Description
G_{ACQ}	Acquisition gain	Consider the gain of the sensor stage, the ADC, and the internal calibration. The gain compensation in this controller simplifies the entire design because G_{ACQ} can be set to 1.
G_{DPWM}	Digital PWM gain	Defined by the ratio between the selected switching frequency and the internal timer clock, calculated with the following equation: $G_{DPWM}=\frac{f_{SW}}{f_{PWM}}=\frac{65kHz}{60MHz}$
H_{ID} (s)	Duty to inductor current transfer function	Simplified boost transfer function, calculated with the following equation: $H_{ID}(s)=\frac{I_L(s)}{d(s)}=\frac{V_{OUT}}{sL}$
H_{LPF} (s)	Low-pass filter	$H_{LPF}(s)=\frac{1}{\left(\frac{s}{\omega_c}+1\right)}$, ω_c: filter cutoff frequency
H_{CI} (s)	PI controller (pole-zero compensation)	$H_{CI}(s)=\frac{\omega_{p0}}{s}\left(\frac{s}{\omega_{z1}}+1\right)$, $\omega_{p0}=K_{ii}$, $\omega_{z1}=\frac{K_{ii}}{K_{pi}}$

T_I can be calculated with Equation (33):

$$T_I(s)=H_{CI}(s)\times G_{DPWM}\times H_{ID}(s)\times G_{ACQ}\times H_{LPF}(s) \quad (33)$$

To accurately track the current shape, it is recommended to use a large bandwidth (BW) (about 10% of the switching frequency) since this results in a fast transient response. However, this leads to a tradeoff since large bandwidths also increase the presence of high-frequency noise.

To prevent instability due to the presence of noise during current acquisition, a first-order low-pass filter is added. Carefully select the cutoff frequency because it reduces both BW and the phase margin (PM). A duty feed-forward (DFF) with an adjustable gain is included to improve the resistive behavior of the PFC input impedance. Table 16 shows the selected control parameters for the current loop based on the control stability analysis and dynamic performance tests.

Table 16: Current Loop Parameters

Symbol	Parameter	Value
K_{PI}	Proportional gain	45
K_{II}	Integral gain	2000
ω_{PI1}	High-frequency pole (Hz) used as an input current filter	3000
DFF	Duty feedforward gain (estimated output duty cycle)	0.86

Figure 20 shows a bode diagram of a discretized current open-loop transfer function ($T_I(s)$), and the effects of the low-pass filter cutoff frequency.

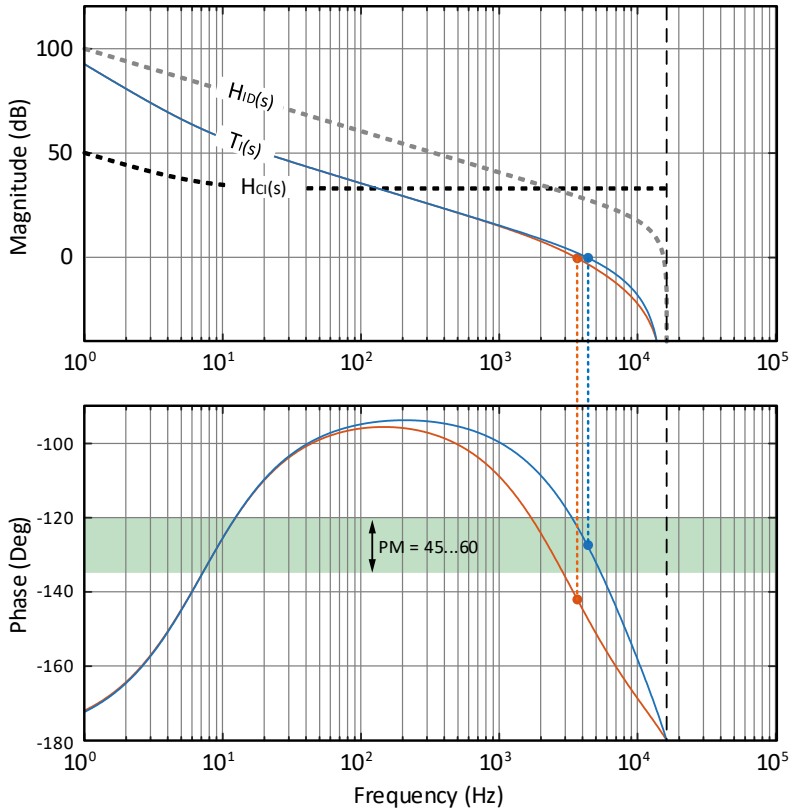


Figure 20: Current Open-Loop Bode Diagram and Effects of the Inductor Current Filter

Figure 21 shows how to set the current loop parameters using the GUI.

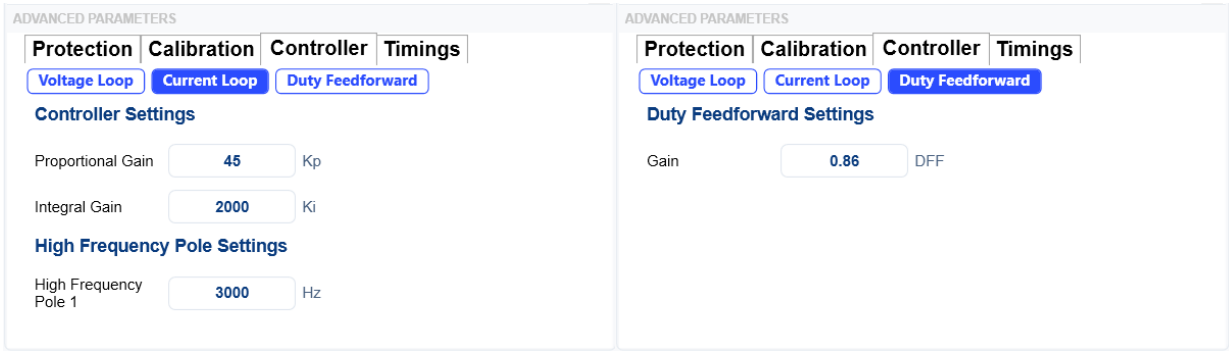


Figure 21: Using the GUI to Set the Current Loop Parameters

4.5. Voltage Loop

The voltage loop is the outer loop that sets the reference for the current loop (see Figure 22). The voltage loop must be slow enough to prevent adding distortions to the current loop, but it must be fast enough to have good dynamic performance, with a BW between 5Hz and 10Hz.

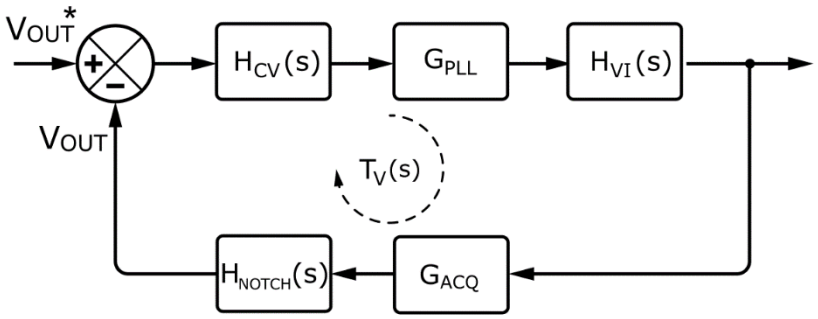


Figure 22: Voltage Loop

Table 17: Voltage Loop Description

Symbol	Parameter	Description
G_{ACQ}	Acquisition gain	G_{ACQ} = 1 due to the calibration gain compensation.
G_{PLL}	Input voltage feedforward	$PLL=G_{PLL}\lvert\sin\omega t\rvert$, $G_{PLL}=\frac{\hat{V}_{IN}}{V_{IN\_RMS}^2}=\frac{2}{\hat{V}_{IN}}$
H_{VI} (s)	Inductor current to voltage transfer function	$H_{VI}(s)=\frac{V_{OUT}(s)}{I_L(s)}=\frac{V_{IN}}{2V_{OUT}}\times\frac{R_{OUT}}{sCR_{OUT}+1}$, $R_{OUT}=\frac{V_{OUT}^2}{P_{OUT}}$
H_{NOTCH} (s)	Notch filter	$H_{NOTCH}(s)=\frac{\left(\frac{s^2}{\omega_0^2}+1\right)}{\left(\frac{s^2}{\omega_0^2}+\frac{s}{Q\omega_0}+1\right)}$, $Q=\frac{1}{\sqrt{2}}$
H_{CV} (s)	Type II compensator	$H_{CV}(s)=\frac{\omega_{P0}}{s}\times\frac{\left(\frac{s}{\omega_{Z1}}+1\right)}{\left(\frac{s}{\omega_{P1}}+1\right)}$, $\omega_{P0}=K_{IV}$, $\omega_{Z1}=\frac{K_{IV}}{K_{PV}}$

T_V can be estimated with Equation (34):

$$T_V(s)=H_{CV}(s)\times G_{PLL}\times H_{vi}(s)\times G_{ACQ}\times H_{NOTCH}(s) \quad (34)$$

The reference for the voltage loop is defined by the reference output voltage parameter. Three values set the V_{OUT} range. In normal operation, the output voltage reference sets the PFC's output voltage. Under light-load conditions, the controller operates in burst mode, and the two threshold levels specify the V_{OUT} range in this mode (see Table 18).

Table 18: Output Voltage Regulation

Parameter	Description	Value	Unit
Reference output voltage	Sets the output voltage for the PFC.	400	V
Hysteresis low threshold	Sets the output voltage range under light-load conditions when the controller operates in burst mode.	400	V
Hysteresis high threshold		425	V

Table 19 shows the selected control parameters for the voltage loop based on the control stability analysis and dynamic performance tests

Table 19: Voltage Loop Parameters

Symbol	Parameter	Value
K_{PV}	Proportional gain	40
K_{IV}	Integral gain	2000
ω_{PV1}	High frequency pole (Hz)	350

Figure 23 shows the bode diagram of the discretized T_V (s).

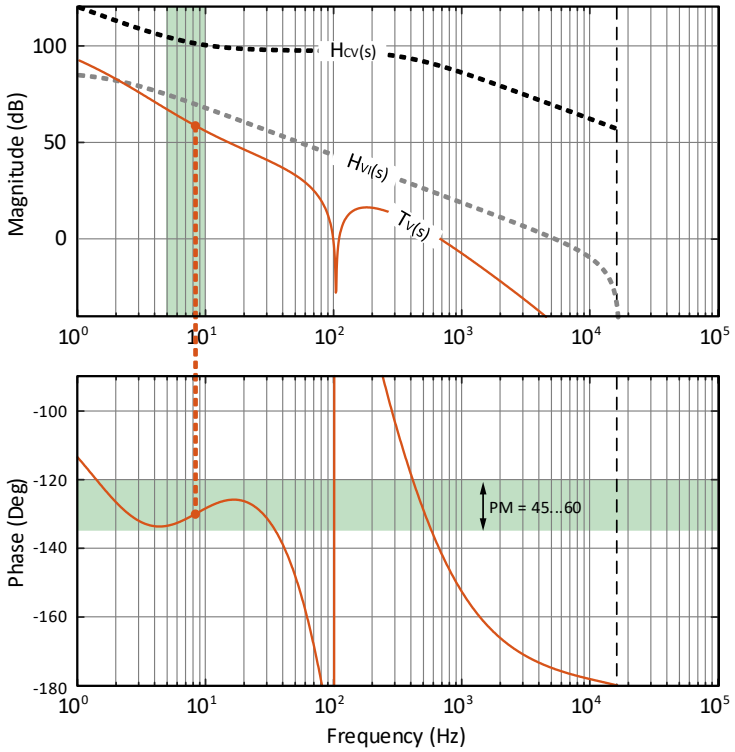


Figure 23: Bode Diagram for T_V

Figure 24 shows how to set the voltage loop parameters with the GUI.

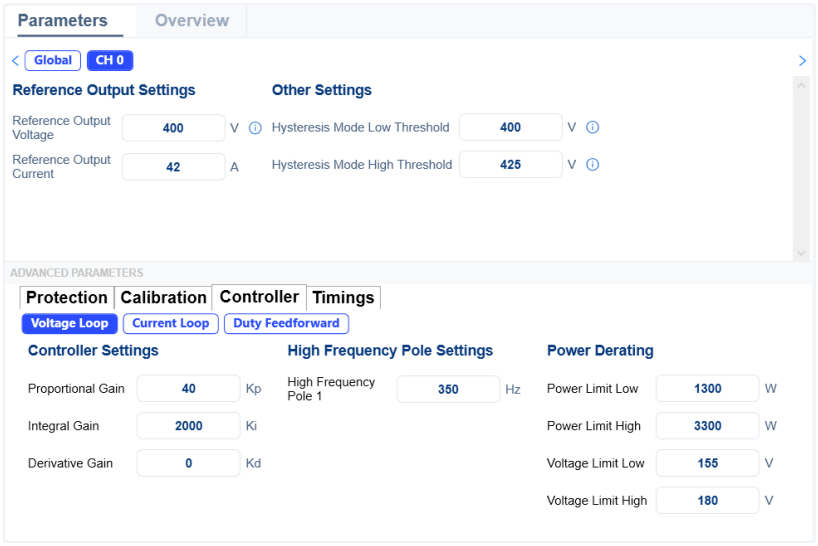


Figure 24: Using the GUI to Set the Voltage Loop Parameters

4.6. Additional Settings

Table 20 shows a brief description of the additional parameters used in this evaluation kit. For a more detailed description, refer to the related datasheet.

Table 20: Additional Controller Settings

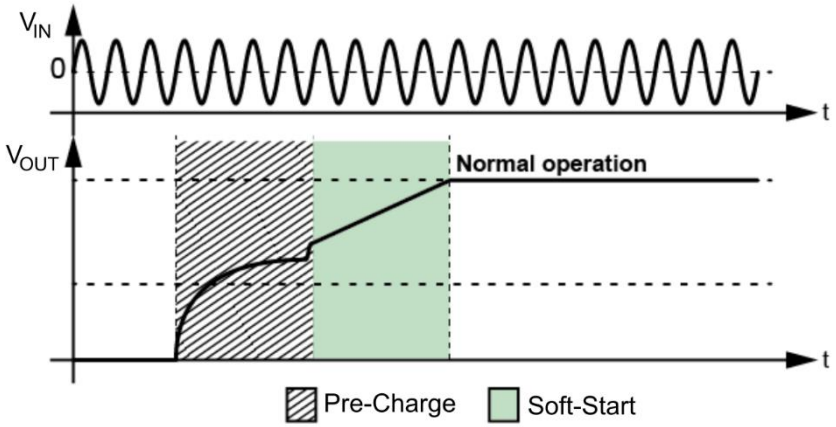
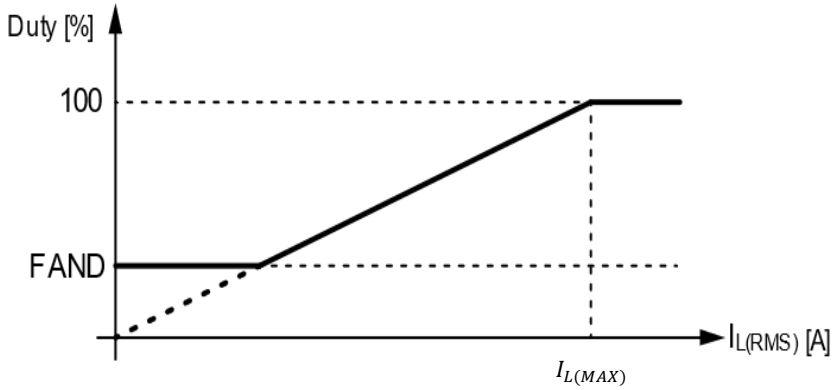
Parameter	Description	Value	Units
Grid frequency	Frequency of the input voltage. This value is used as a reference for the integrated PLL for grid synchronization.	50	Hz
Start delay	The start delay is used during the pre-charge phase when the evaluation kit is connected to an AC power supply. The soft-start duration sets the voltage ramp during the start-up according to the selected output voltage.	1000	ms
Soft-start duration		4000	ms
Minimum fan duty cycle (FAND)	When the temperature exceeds 60°C, the device operates at 100% duty cycle. The graph below shows the duty cycle when the temperature is below 60°C. 	20	%

Figure 25 shows how to set the additional parameters using the GUI.

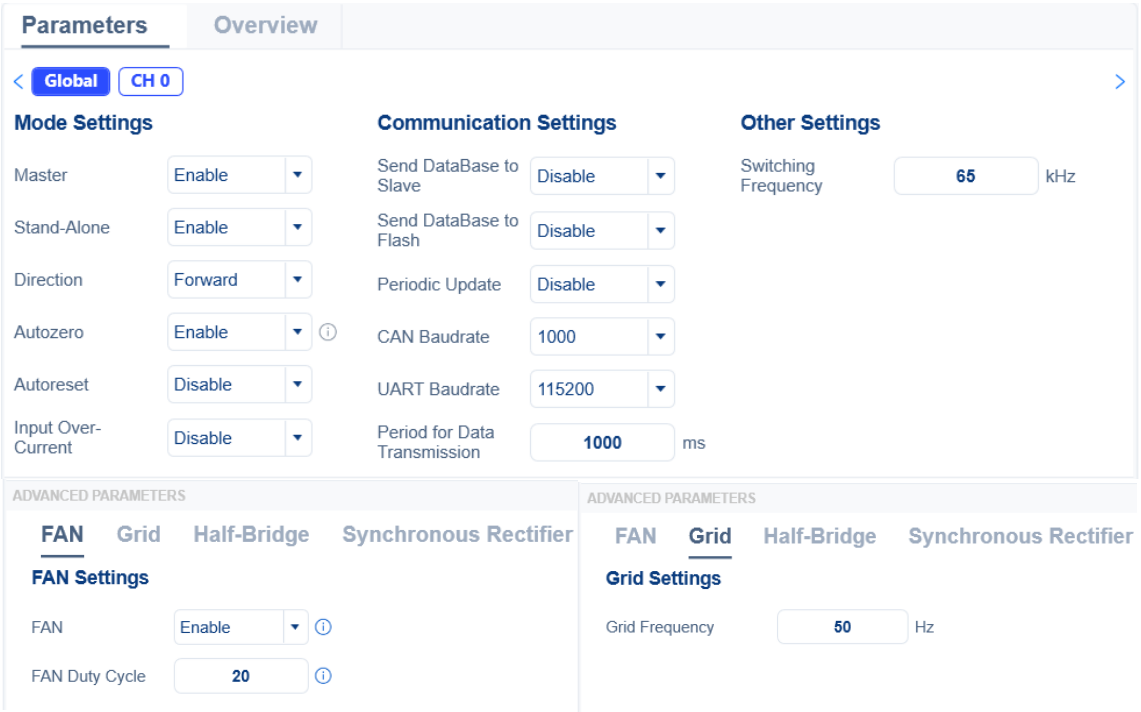


Figure 25: Using the GUI to Set Controller Settings

5. Test Results

5.1. Efficiency and Power Factor (PF)

Figure 26 and Figure 27 show the efficiency under different conditions.

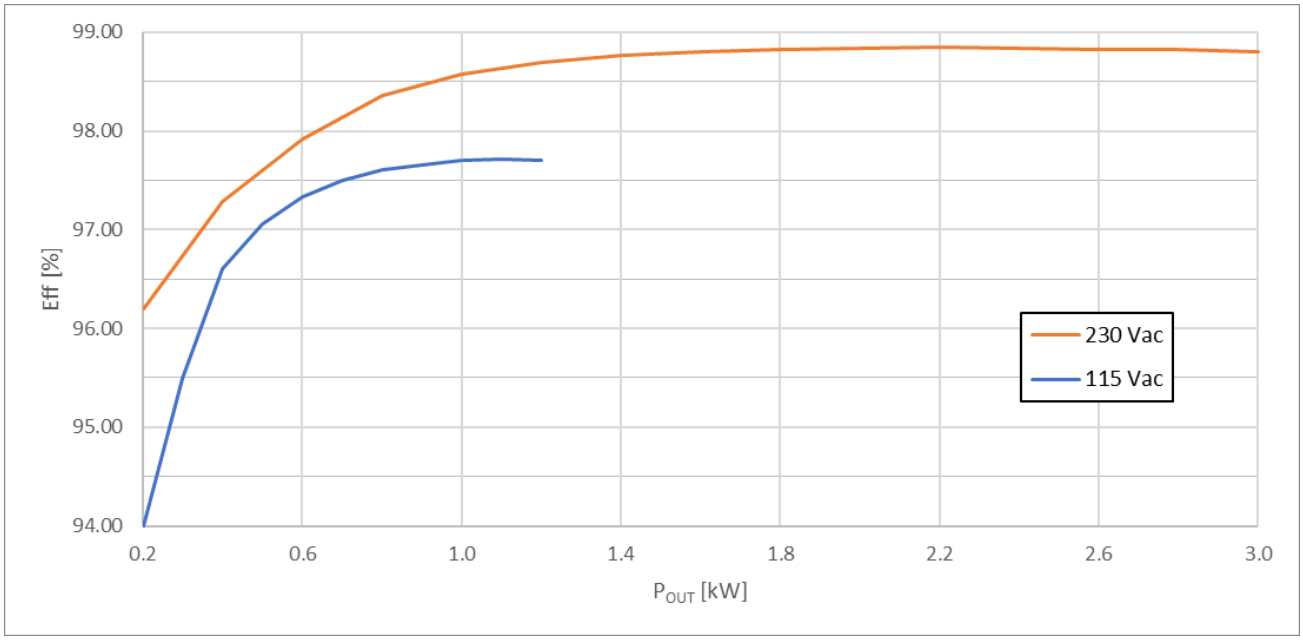


Figure 26: Standalone Efficiency ($115V_{AC}$ and $230V_{AC}$)

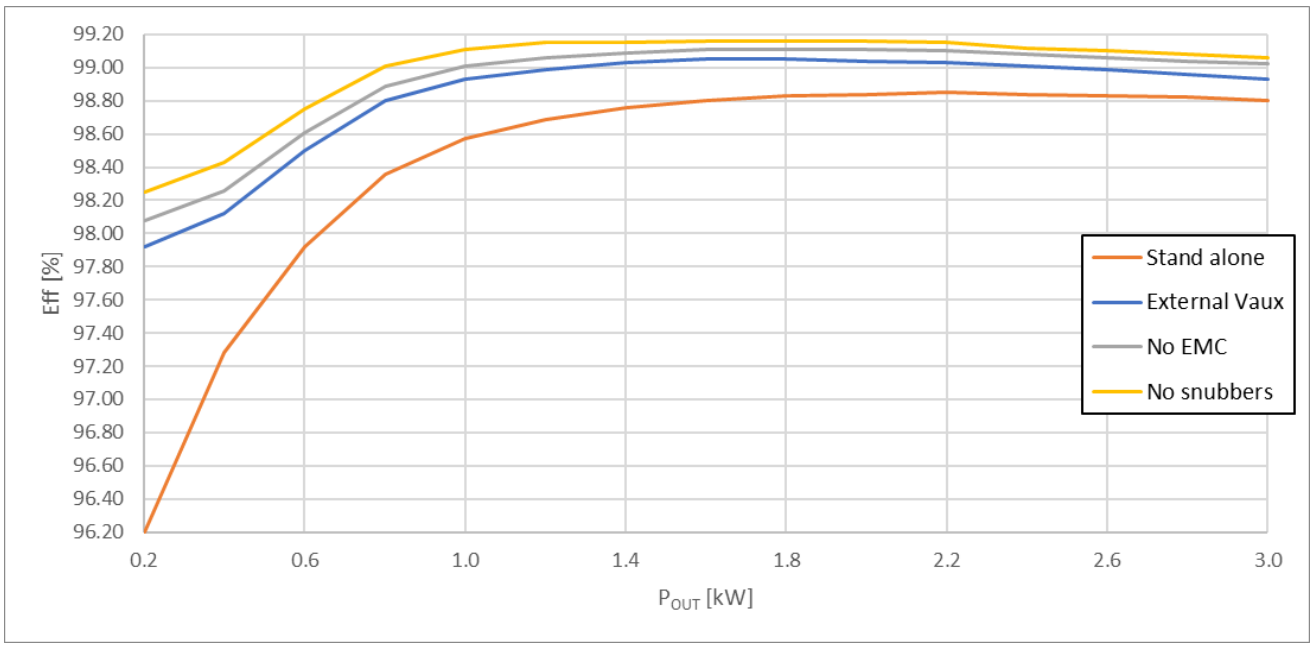


Figure 27: Efficiency ($230V_{AC}$)

Figure 28 shows the efficiency with a $115V_{AC}$. under different conditions.

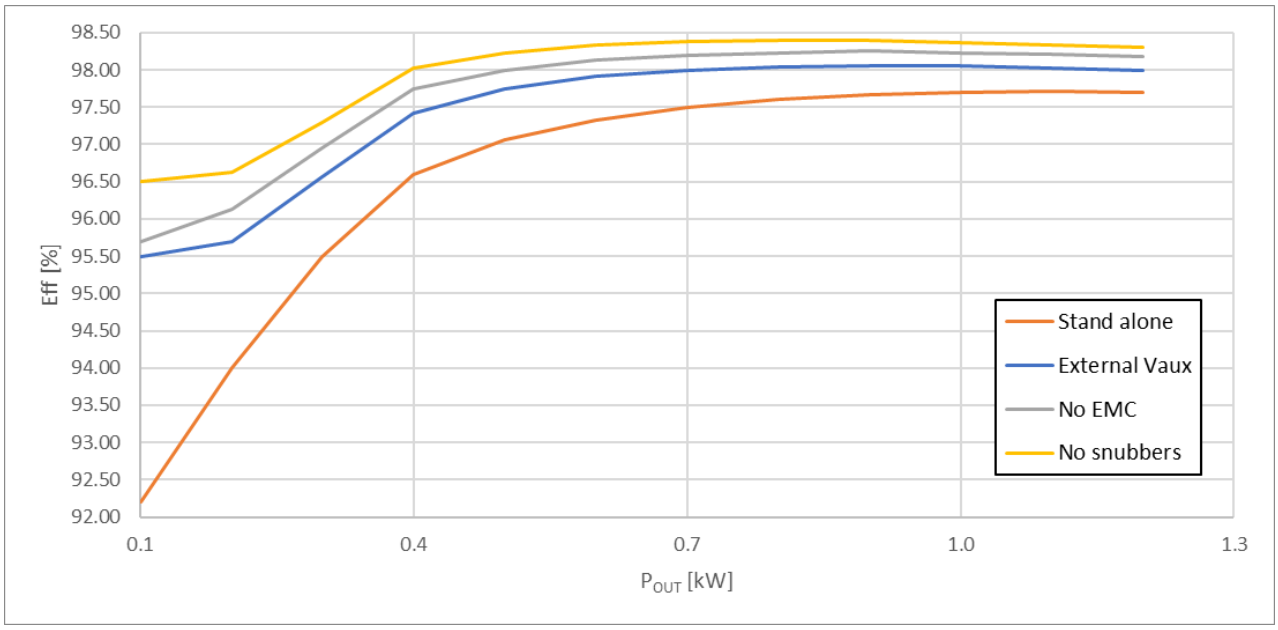


Figure 28: Efficiency ($115V_{AC}$)

Figure 29 shows the power factor obtained for different output power levels.

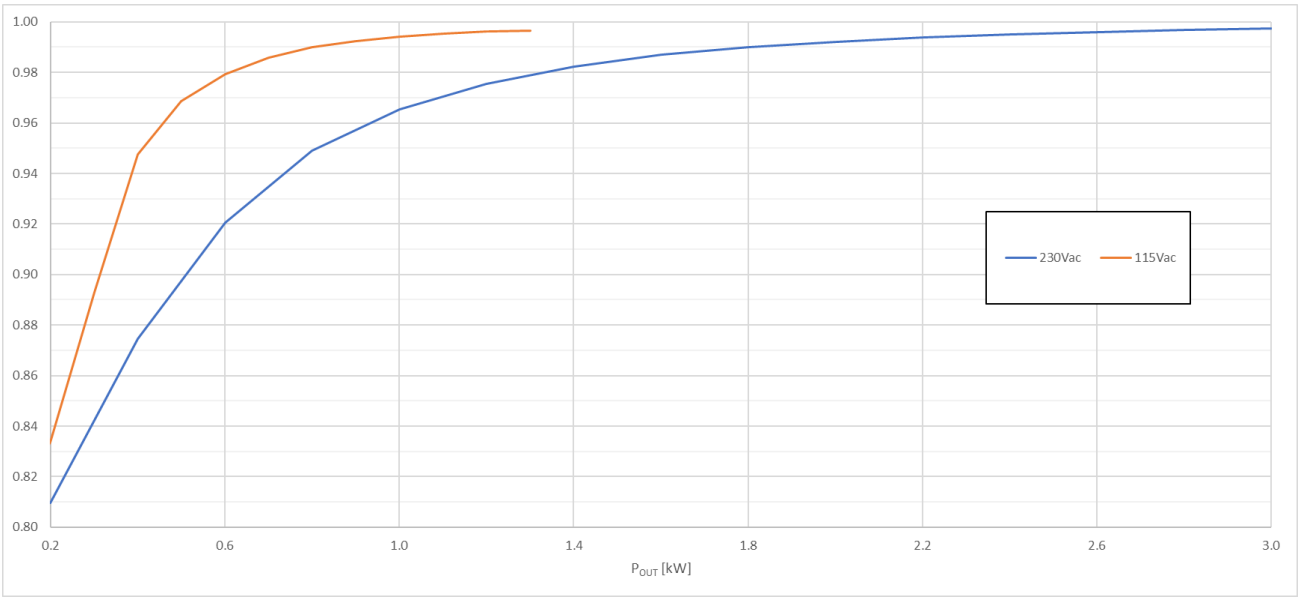


Figure 29: Power Factor

5.2. Total Harmonic Distortion (THD)

The following charts were obtained at nominal conditions.

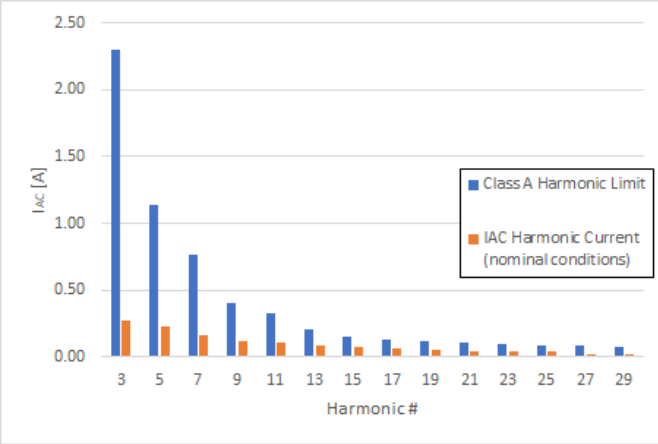


Figure 30: IEC 61000-3-2

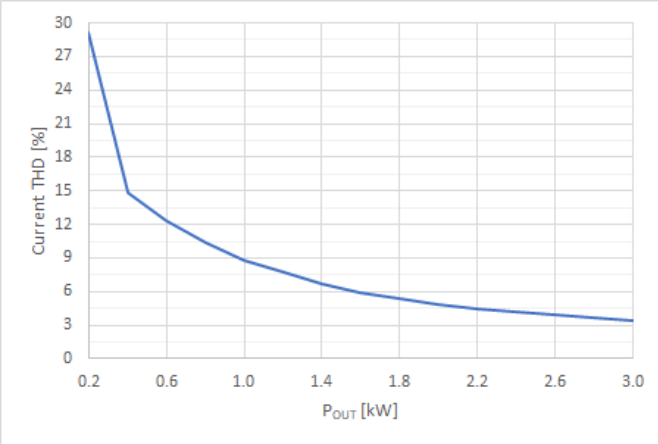


Figure 31: THD

5.3. Steady State Waveform

Figure 32 and Figure 33 show when the totem pole is connected to a power supply. Figure 34 and Figure 35 show when the totem pole is connected to the grid. In all instances, CH1 is V_{IN}, CH2 is I_L, and CH3 and V_{OUT}.

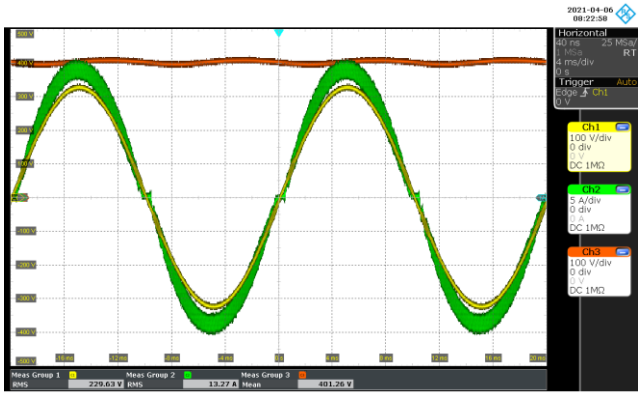


Figure 32: Nominal Conditions (Power Supply)

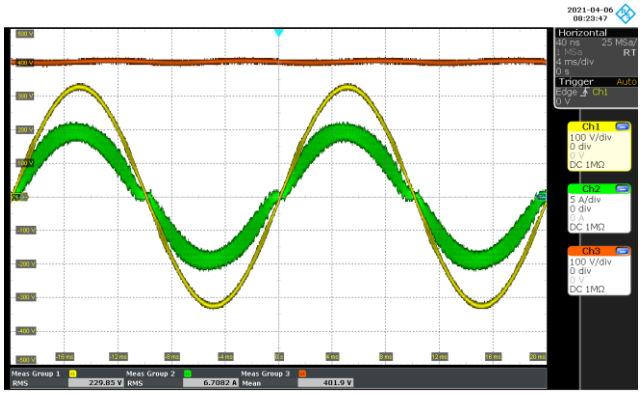


Figure 33: Half-Load (Power Supply)

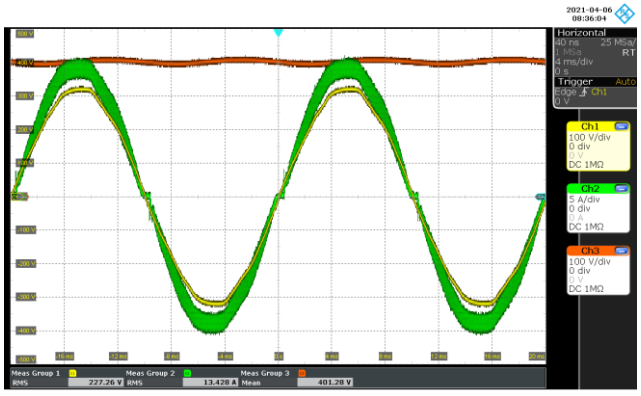


Figure 34: Nominal Conditions (Power Grid)

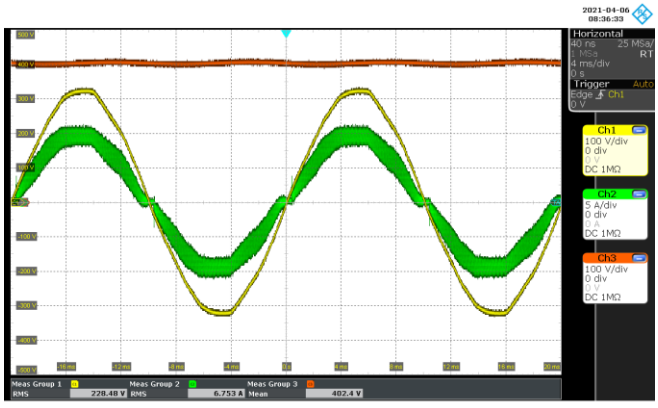


Figure 35: Half-Load (Power Grid)

Current spikes at the zero crossing can be seen when the converter is connected to the grid, though they are kept very low due to the PWM strategy. The cascode's switching speed is mainly controlled by gate resistors, but snubbers also play a part in keeping the drain-to-source voltage transition smooth. This, combined with the SMD decoupling capacitors, keeps the overshoot low (434V). Figure 36 shows the rising dV/dt, where CH2 is I_L and CH3 is V_{DS_LS}.

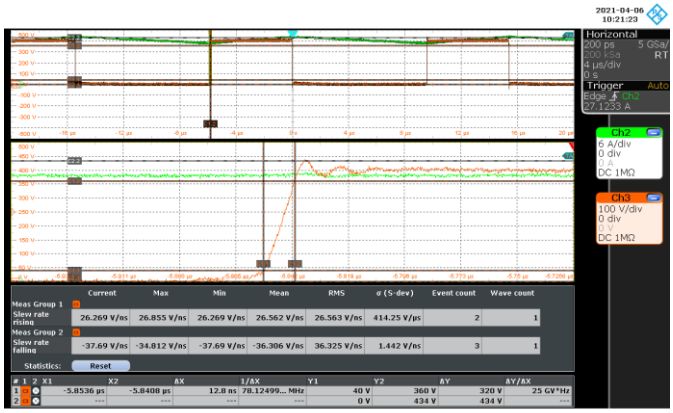


Figure 36: Rising dV/dt

Figure 37 shows the cascode waveforms, where CH2 is I_L, CH3 is V_{DS_LS}, and CH4 is V_{GS_LS}.

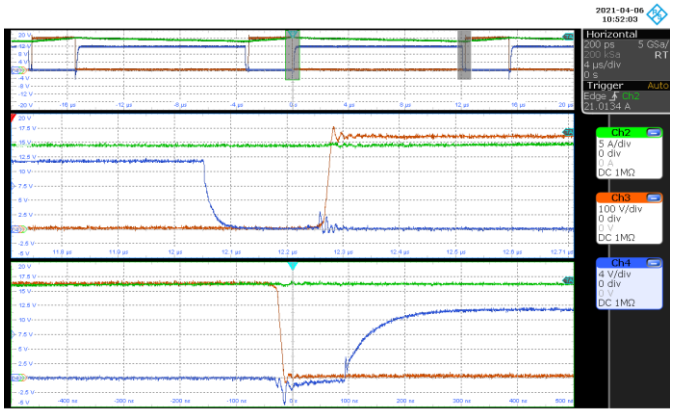


Figure 37: Cascode Waveforms

Under nominal loads, the transient speed at the minimum voltage is about 26kV/µs and -36kV/µs (for the rising and falling speeds, respectively). The MP18831 half-bridge driver can withstand these values with a sufficiently wide margin ($CMTI_{MIN}$ = 100kV/µs). This driver is well-suited for isolated converters due to its isolation between primary and secondary (1.5kV_{DC} functional isolation). The MP18831 also provides overlap protection and configurable dead time control.

While efficiency could be improved with a faster dV/dt, this would negatively impact EMC. This means that there is a trade-off between efficiency and EMC.

The gate-to-source voltage waveform is very clean due to the 4-lead package, which has a dedicated source for control. This improves the system robustness because it makes it difficult for noise to reach the voltage threshold.

Figure 38 shows the conduction of the slow Si-MOSFET in orange, where CH2 is I_L, CH3 is V_{DS_LS}, and CH4 is V_{GS_LS}. The inductor current is compared to the threshold values to enable and disable the MOSFET (SR_ON and SR_OFF registers). Without a hysteresis in the threshold (i.e. the same values were used for SR_ON and SR_OFF), the protection would be triggered many times in same semi-period. Note that this waveform uses a 2GHz oscilloscope BW and 500MHz voltage probe BW.

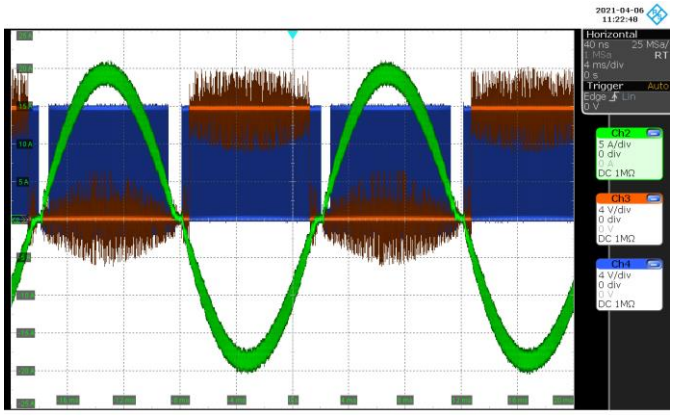


Figure 38: SR

5.4. Start-Up

When the input is connected, there is an inrush current to charge the bus capacitors. This current is limited by the NTC to avoid trigging circuit breakers. Figure 39 shows the NTC resistance value (R_{NTC} = 319V/10.7A, or about 30Ω) during the inrush current, where CH1 is V_{IN}, CH3 is V_{OUT}, and CH4 is I_I.

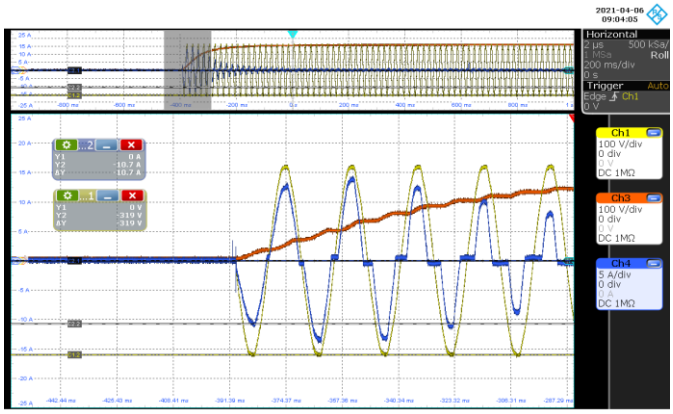


Figure 39: Inrush Current

Figure 40 shows start-up without a load, where CH1 is V_{IN}, CH2 is I_L, and CH3 is V_{OUT}. Start-up takes about 2.4s.

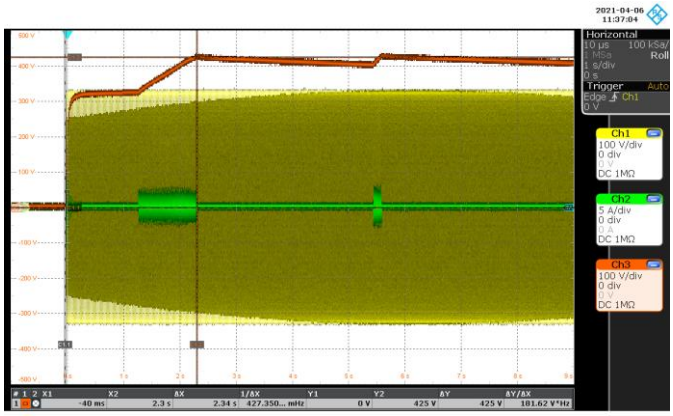


Figure 40: Start-Up Without Load

A soft-start ramp can be calculated with Equation (35)

$$\text{Soft start}=\left(V_{OUT\_MAX}-V_{IN\_PK}\right)\times\frac{SSD}{V_{REF}}=\left(425V-230\sqrt{2}V\right)\times\frac{4s}{400V}=\underline{1s} \quad (35)$$

The drivers are disabled when the output voltage reaches $425V_{DC}$, then enabled again at $400V_{DC}$. These two values can be changed in the VHYSTH and VHYSTL registers. Refer to the related datasheet for more details.

5.5. Load Transients

A full load step is applied under nominal conditions with a current slope of 0.062A/µs. The converter has an excellent response and steady state within four grid periods. Figure 41 shows the no-load to full-load step, while Figure 42 shows the full-load to no-load step. For both figures, CH1 and V_{IN}, CH2 is I_L, CH3 and V_{OUT}, and CH4 is I_{OUT}.

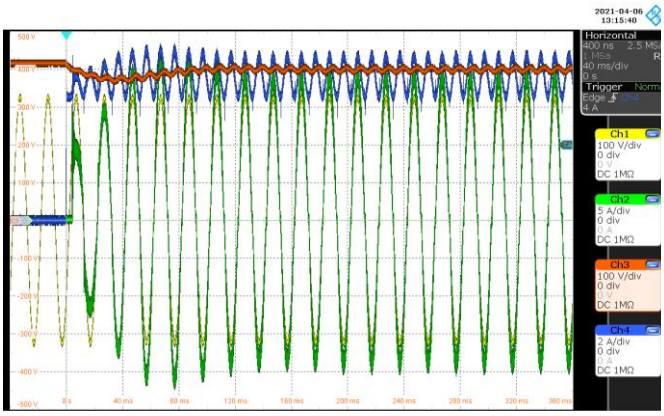


Figure 41: No-Load to Full-Load Step

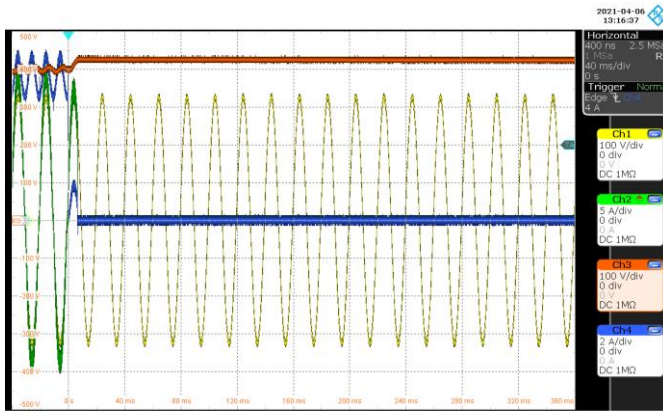


Figure 42: Full-Load to No-Load Step

The output voltage rises up to 425V when the output current goes to zero. Note that the output current ripple is due to the electronic load dynamics.

Figure 43 on page 35 shows what happens when the load demands 0.5A instead of 0A, where CH1 is V_{IN}, CH2 is I_L, CH3 is V_{OUT}, and CH4 is I_{OUT}.

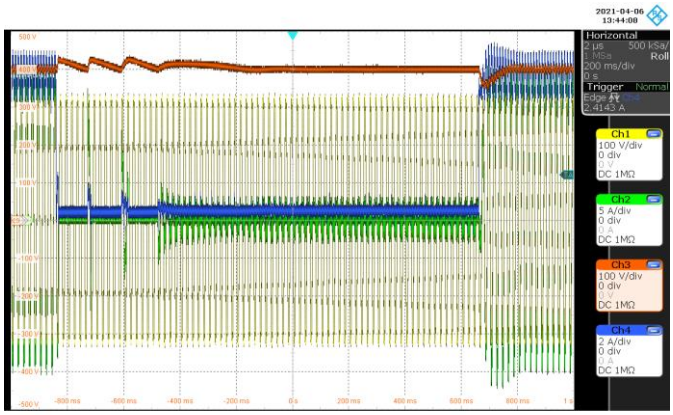


Figure 43: Light-Load Behavior

The output voltage has hysteretic behaviour when light loads are applied, but this behaviour only occurs for a short period of time.

5.6. Line Transients (Voltage Dips/Sags)

The IEC 61000-4-11 standard specifies voltage dips/sags, short interruptions, and voltage variation immunity tests. The first two tests are mandatory, but the last test is optional. The tests carried out for this reference design cover voltage sags, which have the most stringent requirements.

As stated in IEC 61000-4-11:2020, voltage sags occur due to faults in a network or in installations caused by large, sudden load changes.

Considering that U_T is the rated voltage for the equipment, Table 21 shows the test levels and the duration of the voltage dips used to test the system's response to line transients:

Table 21: Recommended Test Levels and Durations for Voltage Dips (Class 3 and 50Hz)

U_T (%)	0	0	40	70	80
# cycles	1	½	10	25	250

Changes in the supply voltage were carried out at the voltage's zero crossings. There was a total of three sags at 10s intervals.

Generally, the 80% voltage sag test is most likely to be passed, as the converter has to work under those conditions in a steady state. Figure 44 on page 36 shows this, where CH1 is V_{IN}, CH2 is I_L, and CH3 is V_{OUT}. The results from Figure 44 indicates normal operation within the specified limits.

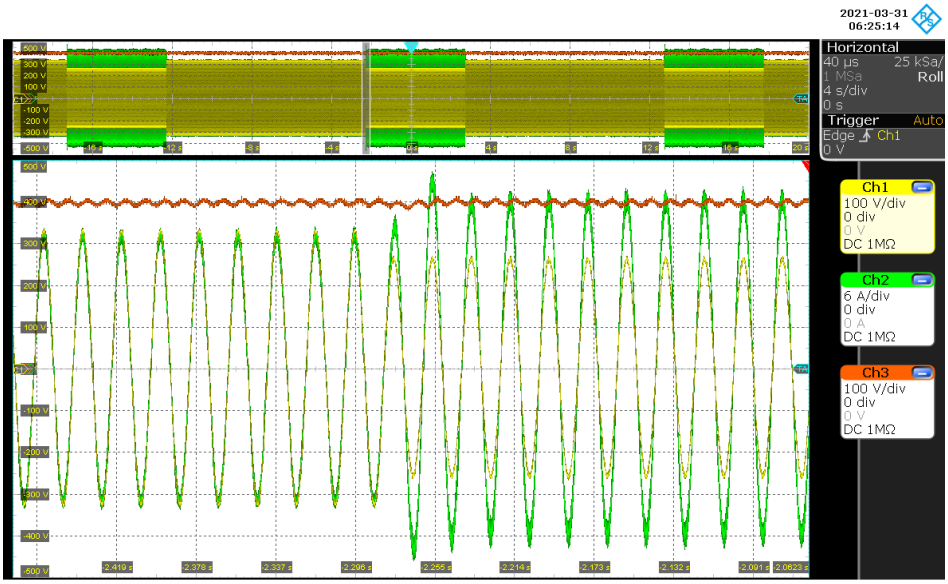


Figure 44: 80% Test During 5s Interval

The 70% voltage sag test can trigger the output power derating function if the input voltage is too low (161V_{RMS}). To mitigate this issue, derating was delayed to withstand sags. Figure 45 shows the results from the 70% test, where CH1 is V_{IN}, CH2 is I_L, and CH3 is V_{OUT}. The results from Figure 45 indicate normal operation within the specified limits.

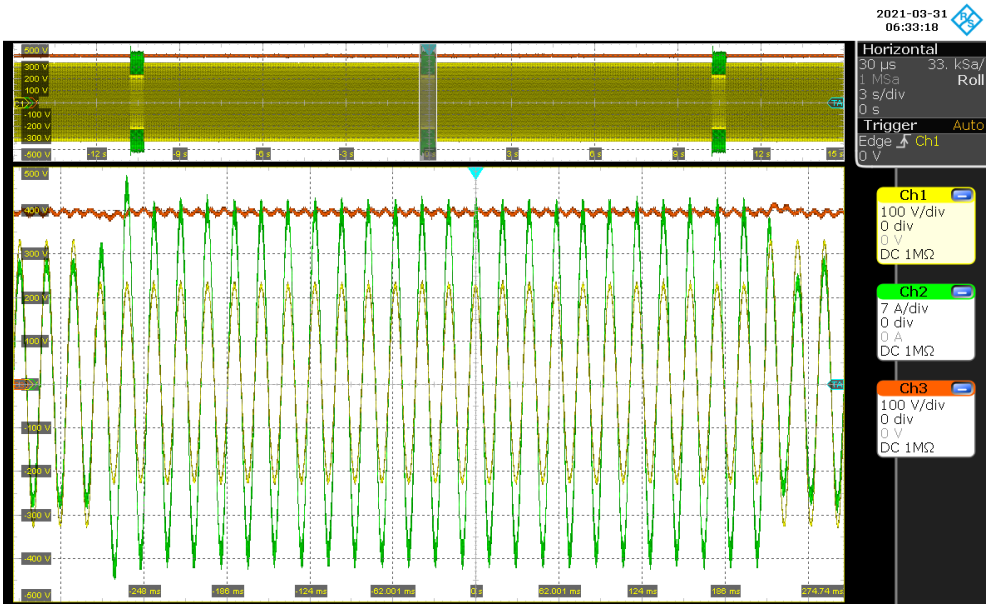


Figure 45: 70% Test During 500ms Interval

The 40% voltage sag test is the most difficult test to pass. If the device does not provide a protection under this scenario, the current through the transistors rises too high, which can result in transistor breakdown. The MPF32010's IREF register allows the totem pole to use this reference to clamp the input current and protect the transistors. The default threshold value for this protection is 42A. If the value is overpassed, the average current value is clamped at 42A. This value is not a constant, and can be modified using the GUI.

Figure 46 shows the result of the 40% voltage sag test, where CH1 is V_{IN}, CH2 is I_L, and CH3 is V_{OUT}. The output voltage drops since the load does not receive a sufficient current. The isolated DC/DC converter that is connected after the AC/DC converter should be able to work at this voltage level. The results from Figure 46 indicate a lower performance until the voltage stops sagging. Then the DUT recovers to normal operation without intervention.

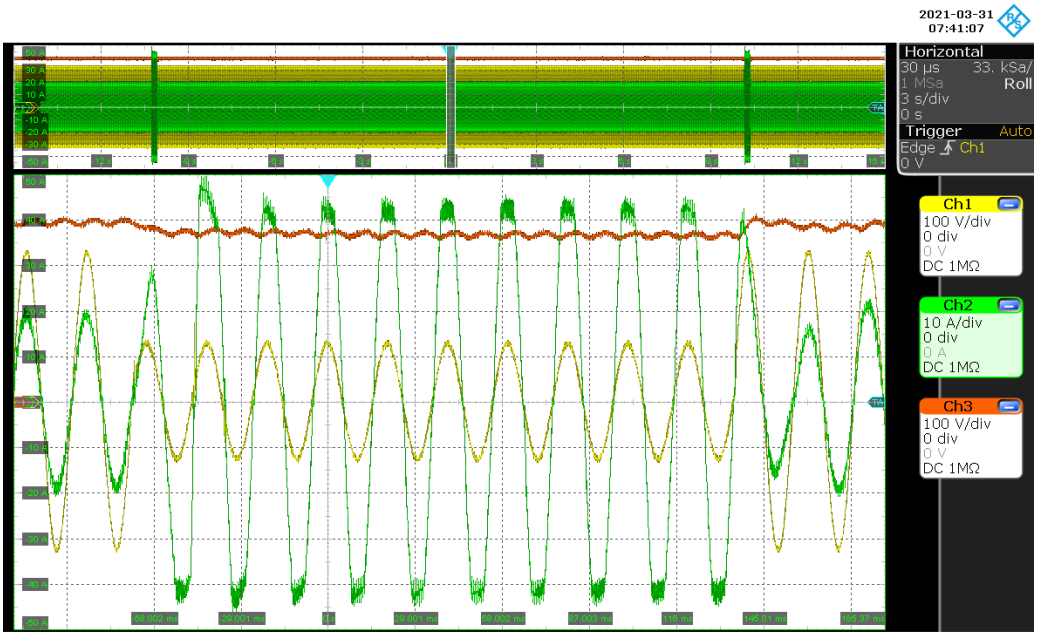


Figure 46: 40% Test During 200ms Interval

Figure 47 shows what happens when the grid power disappears and power loss lasts for an entire cycle, where CH1 is V_{IN}, CH2 is I_L, and CH3 is V_{OUT}. The results from Figure 47 indicate indicate a lower performance until grid power returns. Then the DUT recovers to normal operation without intervention. Please note that this test has been run with half the nominal load, due to the fact that the output capacitor (see Section 3.1) was selected was selected based on the output voltage ripple, which means the converter can only withstand a voltage sag of one half-cycle at full load.

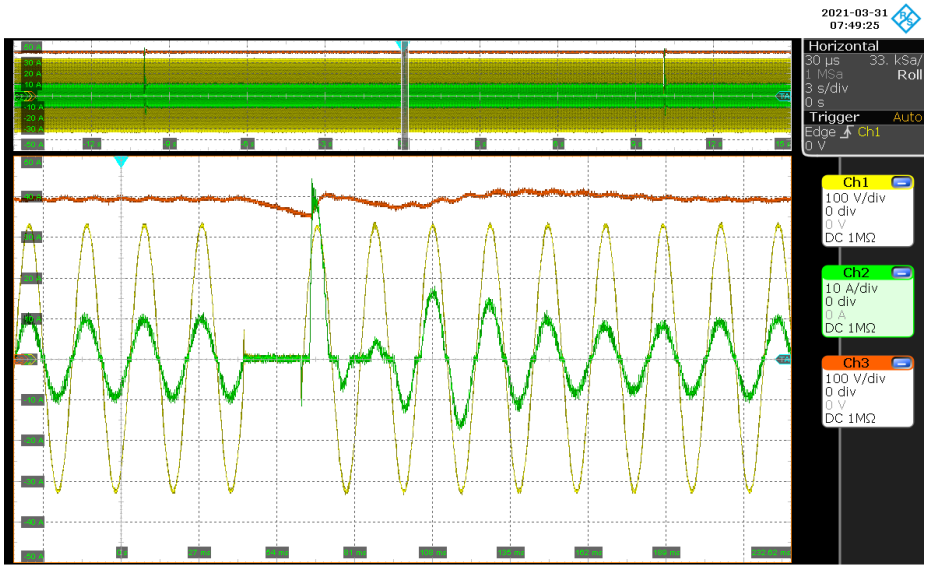


Figure 47: 0% Grid Power During 1 Cycle

Figure 48 shows what happens when the power grid disappears for only half a cycle, where CH1 is V_{IN}, CH2 is I_L, and CH3 is V_{OUT}. The results from Figure 48 indicate indicate a lower performance until grid power returns. Then the DUT recovers to normal operation without intervention.

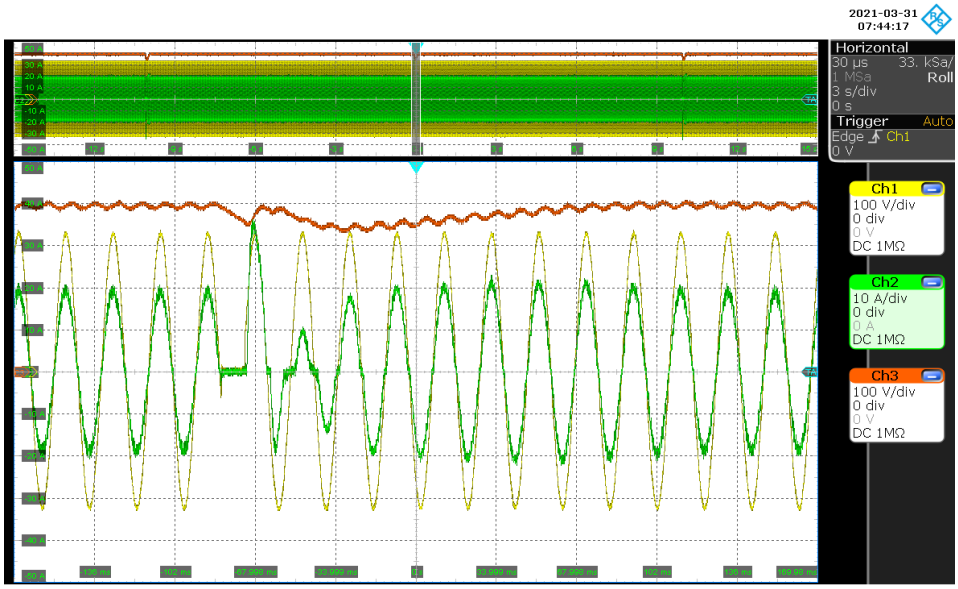


Figure 48: 0% Grid Power During Half of a Cycle

5.7. Overload and Power Derating

The converter delivers 3kW at nominal conditions, but it can deliver up to 3.35kW. When this limit is reached, the control clamps the output power by decreasing the output voltage. If the output voltage drops below the input voltage, an inrush current flows into the electrolytic capacitors and triggers an external circuit breaker (optional, can be added by the user). To avoid this scenario, output under-voltage protection (UVP) triggers an alarm that stops the converter. However, since the source-to-load current path in a boost converter is always connected, an external circuit breaker at the output is required to stop the current from flowing. A connector (J13) can be used to trigger this protection (not isolated from power).

The output voltage is constantly compared to the input voltage (with an added 15V margin that can be modified via the DOUV register). If this limit is reached, output UVP is triggered, and the converter enters a halt. Figure 49 shows what happens when the output current rises from 6.5A to 9A for about 2 seconds, where CH1 is V_{IN}, CH2 is I_L, CH3 is V_{OUT}, and CH4 is I_{OUT}. During this period, the output voltage is reduced to approximately 370V.

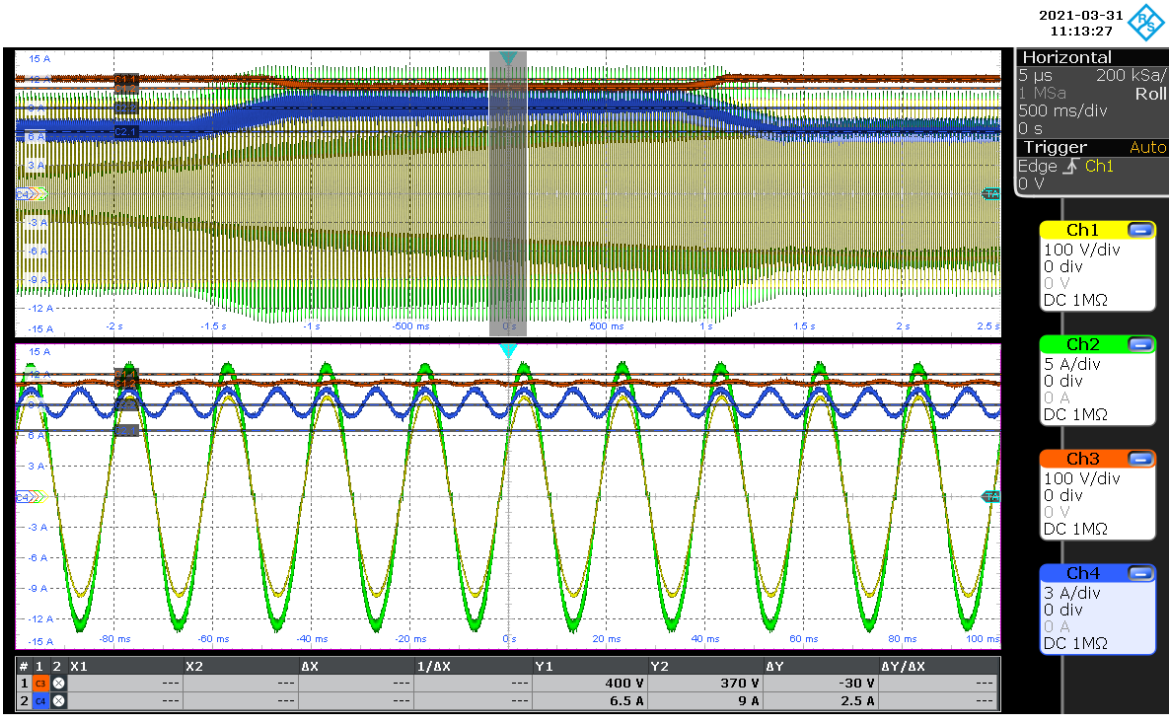


Figure 49: Overload Conditions

This output power limit drops if the input voltage drops (power derating). Figure 50 shows what happens during power derating, where CH1 is V_{IN}, CH2 is I_L, and CH3 is V_{OUT}.

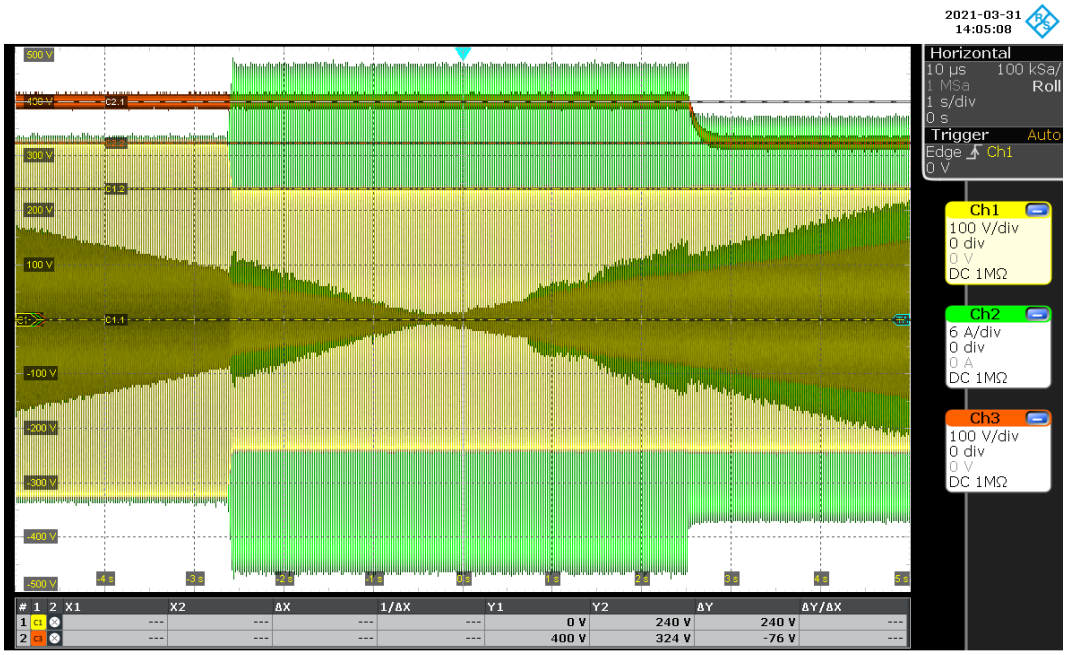


Figure 50: Power Derating

This protection is not enabled until 5 seconds after the condition is met. This is done to enable voltage sags without switching off the converter. There are four registers to tune this protection: PLIMH, PLIML, VLIMH and VLIML (3350W, 1300W, 180V and 155V are the default values, respectively). Refer to the related datasheet for more information.

5.8. Hot Switch On

A 56Ω resistive load should be connected to the output before the converter is turned on. When the PFC switches on, the coil current waveform begins to change. Figure 51 shows the typical waveforms of a rectifier bridge. Figure 52 offers a close-up view of what happens to these waveforms when the PFC is switched on. For both figures, CH1 is V_{IN}, CH2 is I_L, CH3 is V_{OUT}, and CH4 is I_{OUT}.

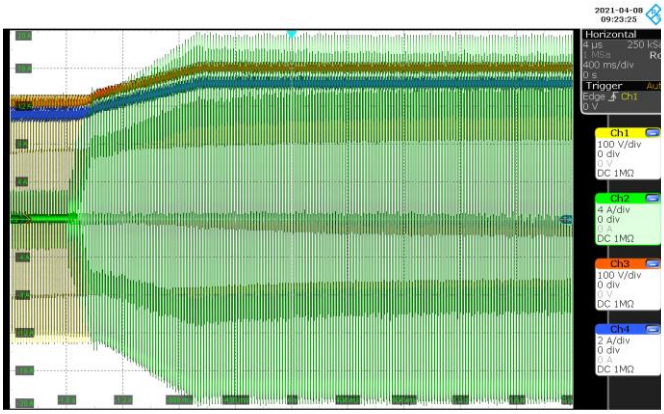


Figure 51: Hot Switch On

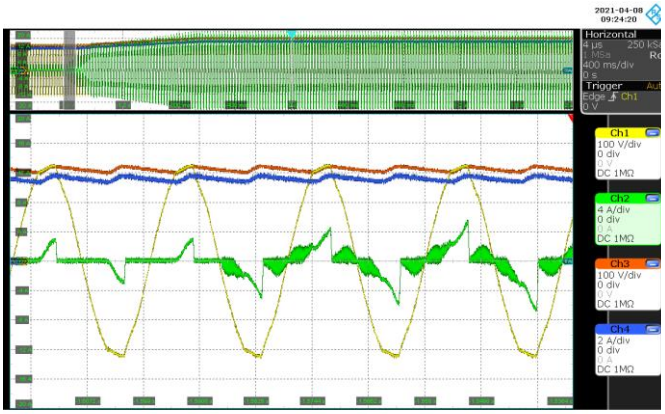


Figure 52: Zoom On Switch On

Then the coil current waveform becomes a sinusoidal wave that is in phase with input voltage. Figure 53 shows the zoom on soft start. Figure 54 shows the zoom on steady state. For both figures, CH1 is V_{IN}, CH2 is I_L, CH3 is V_{OUT}, and CH4 is I_{OUT}.

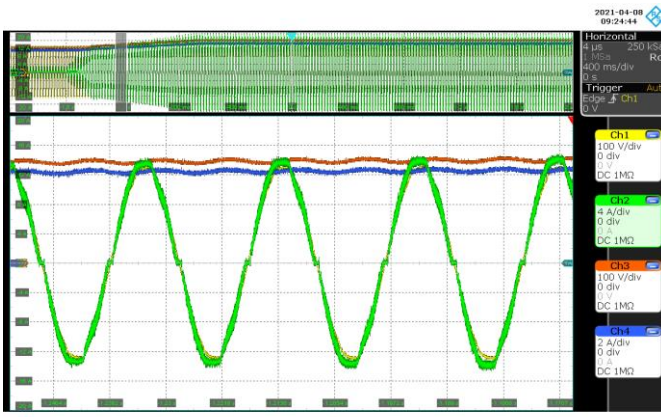


Figure 53: Zoom On Soft Start

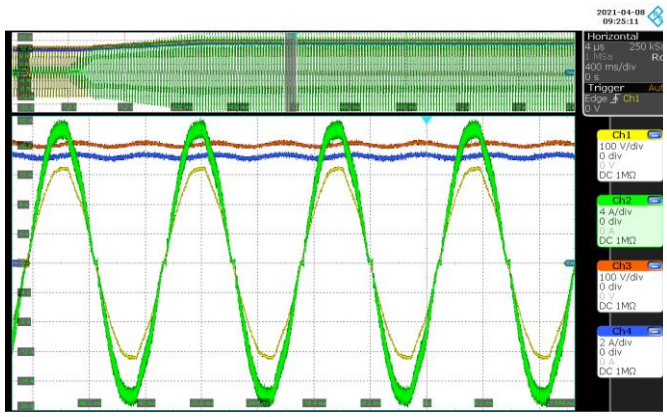


Figure 54: Zoom On Steady State

5.9. Conducted Emissions (EMC)

Standard CISPR 32:2015+AMD1 (Class A).

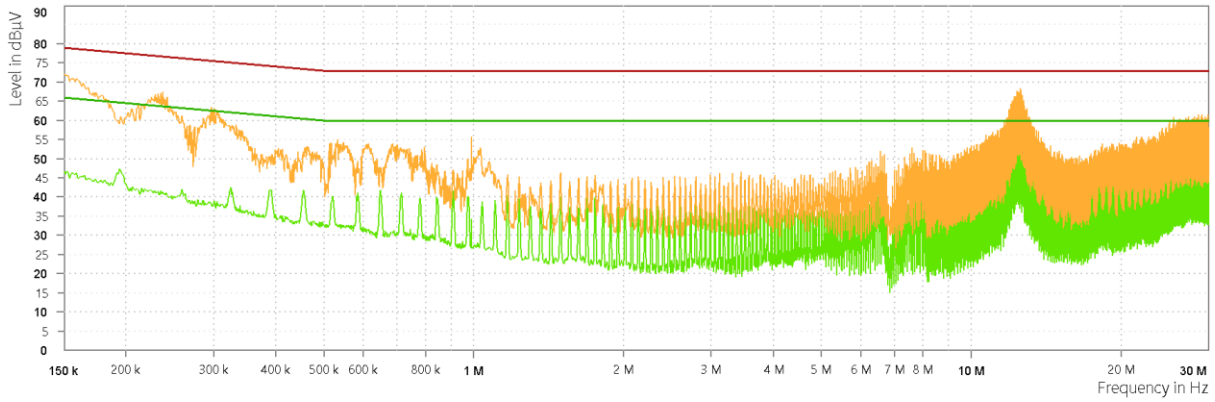


Figure 55: Line

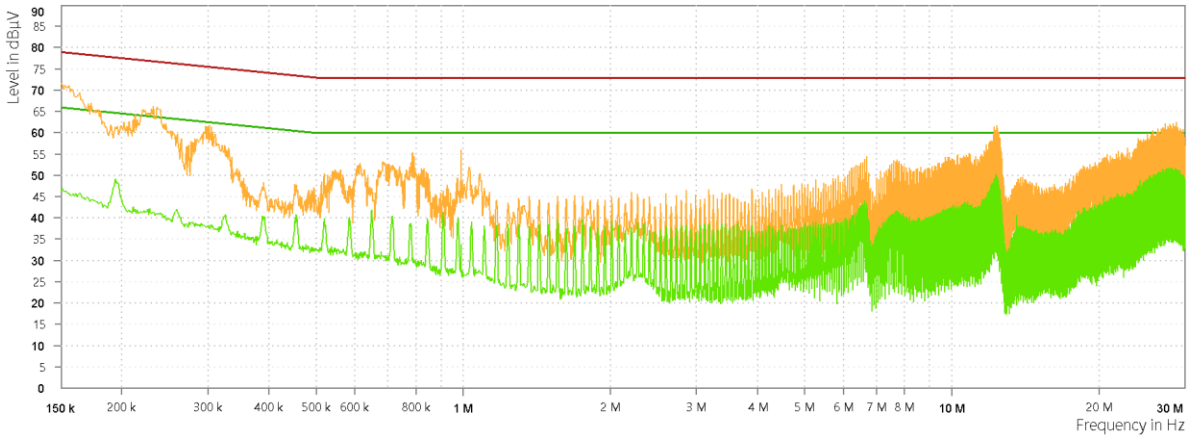


Figure 56: Neutral

5.10. Thermal Performance

There is a hot spot located on the SiC devices. Figure 57 shows the temperatures when the system's thermal performance was tested under nominal conditions at room temperature (about 23°C). Note that the fan was spinning at maximum speed.

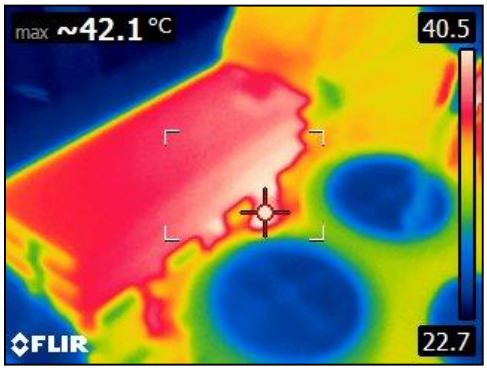


Figure 57: Hot Spot

6. Start-Up

6.1. Board Requirements

The overall reference board requires five boards total, listed below (see Figure 58).

1. EVF32010-18831-01A (main board)
2. MPF32010 CTRL BOARD v01
3. BUCK-LV-00A
4. BUCK-HV-00A
5. COMM-BOARD-01A

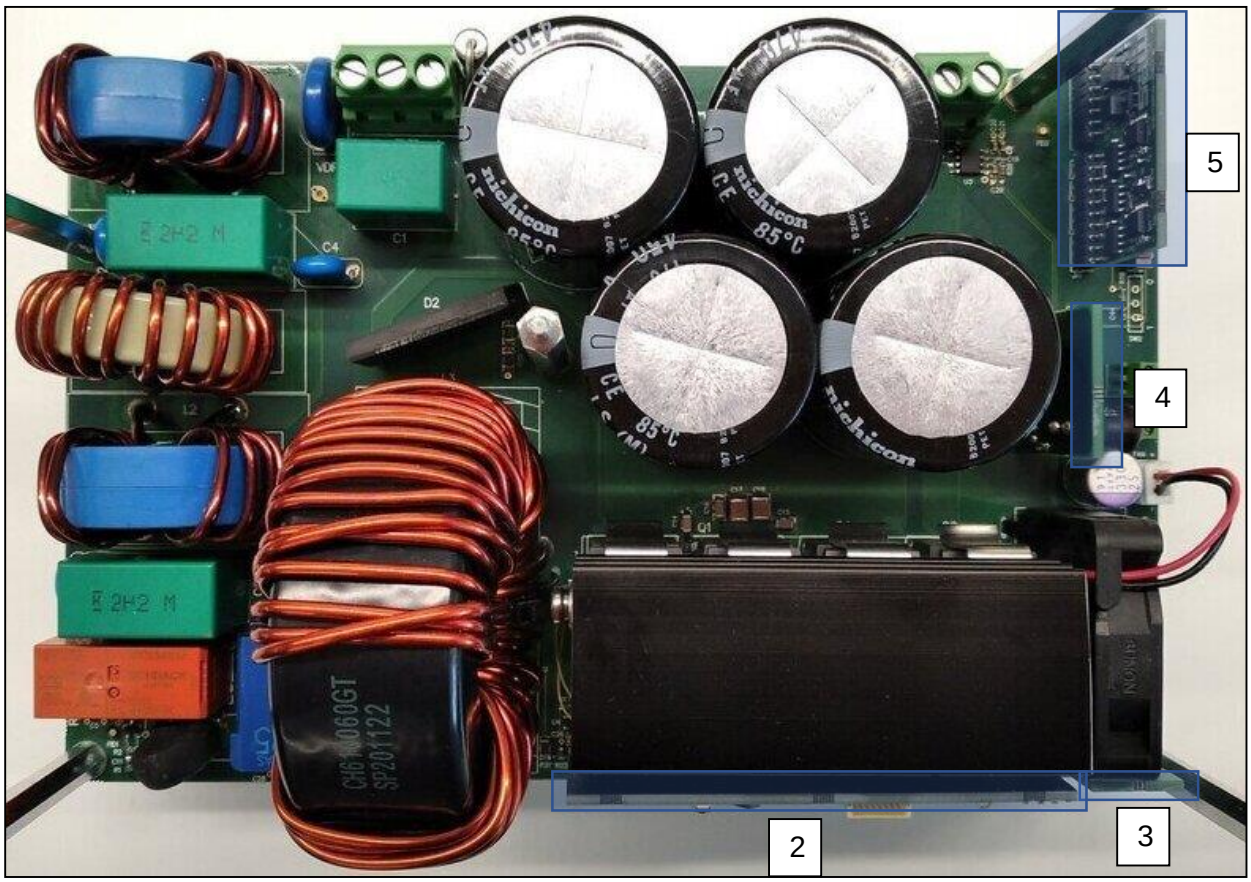


Figure 58: Totem-Pole Converter

6.2. Board Connection

1. Ensure that all daughter boards are connected (see Figure 59).
2. Connect the power cables. It is recommended to connect the circuit breaker to the input.

Figure 59: Front View

3. Connect the communications cables (optional) (see Figure 60).

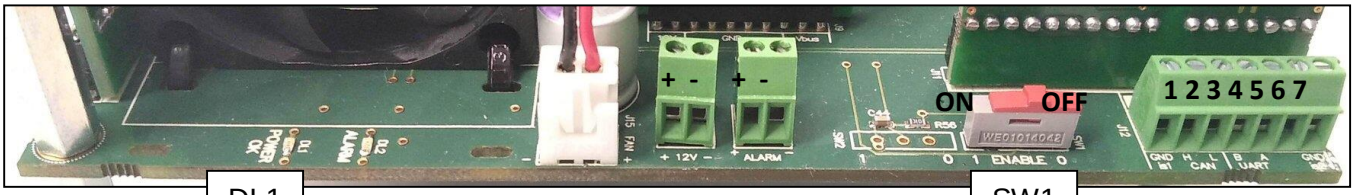


Figure 60: Lateral View

6.3. Board Start-Up

1. Apply 230V_{AC} to the input.
2. Slide SW1 to the on position. The output should reach 400V after a few seconds. The device should work in burst mode since there is no load. The Power OK LED (DL1) should be on.
3. Increase the load current.

6.4. Board Shutdown

1. Decrease the load current down to 0A.
2. Slide SW1 to the off position.
3. Remove the input voltage.
4. Discharge the bulk capacitors with the load.

Note that the evaluation board is for evaluation purposes only, and is not intended to be a finished product.

7. Schematics

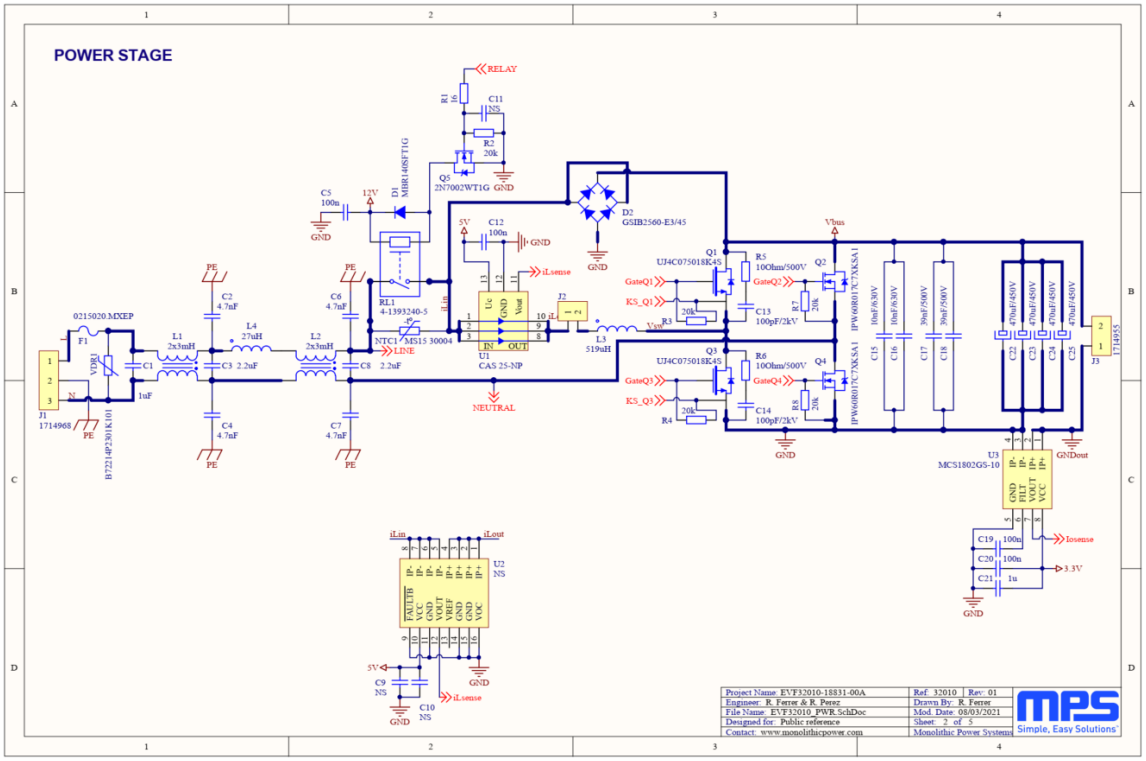


Figure 61: Main Board Schematic 1/3 (EVF32010-18831-01A)

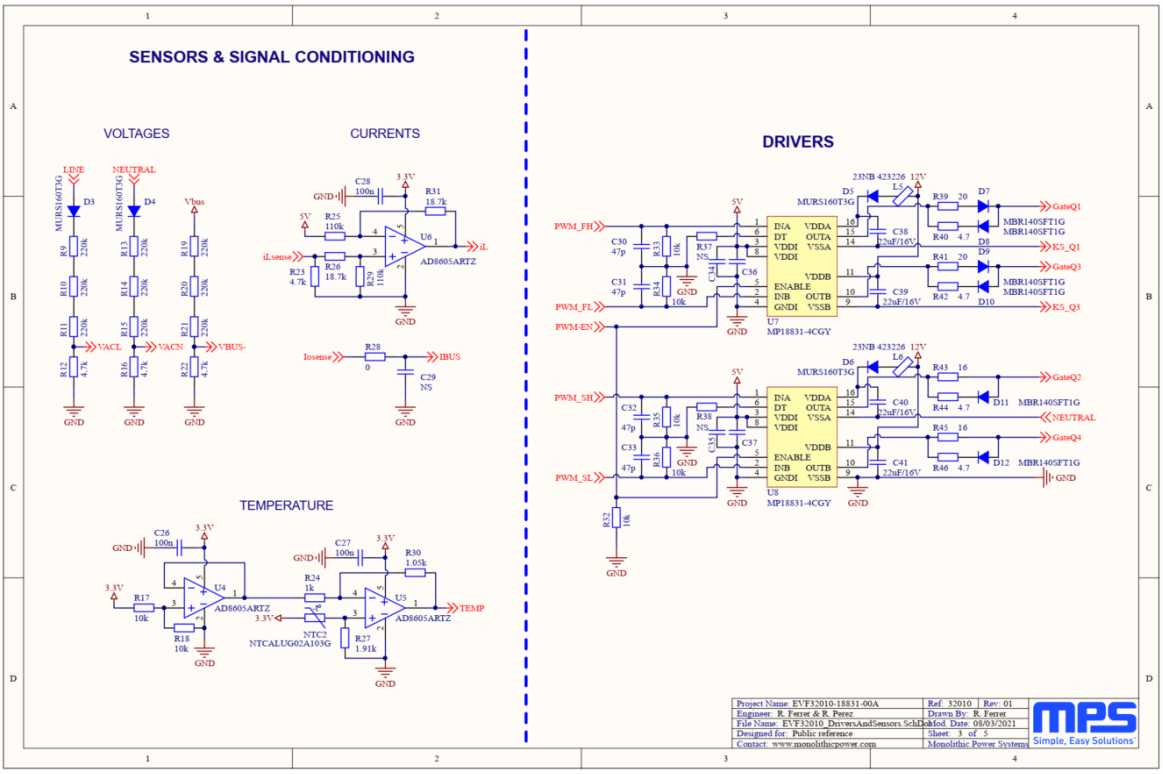


Figure 62: Main Board Schematic 2/3 (EVF32010-18831-01A)

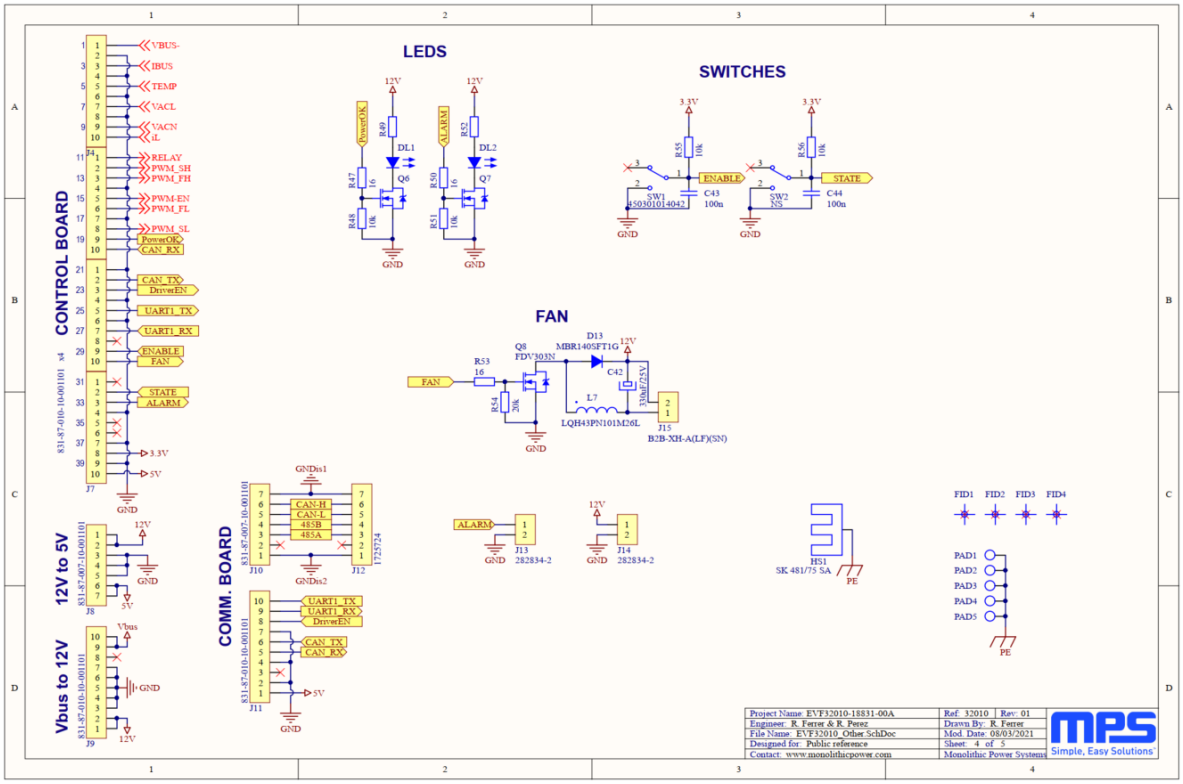


Figure 63: Main Board Schematic 3/3 (EVF32010-18831-01A)

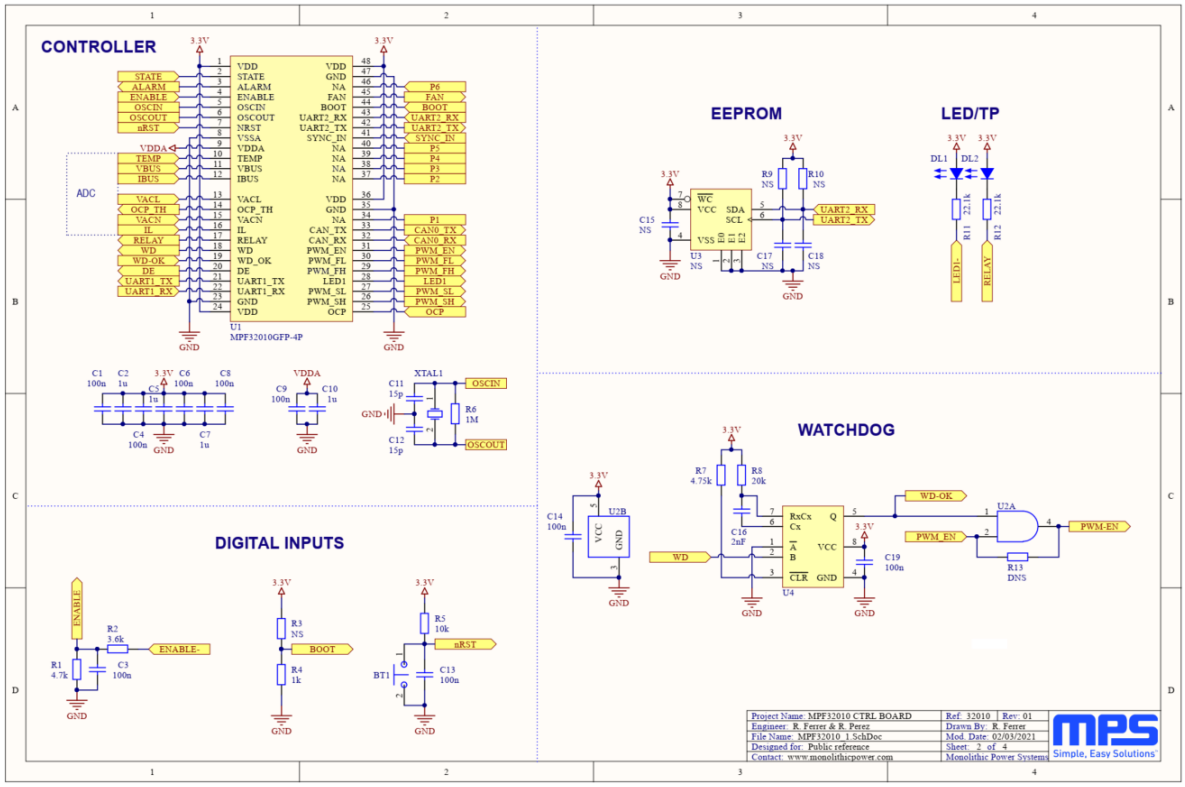


Figure 64: Control Board Schematic 1/3 (MPF32010)

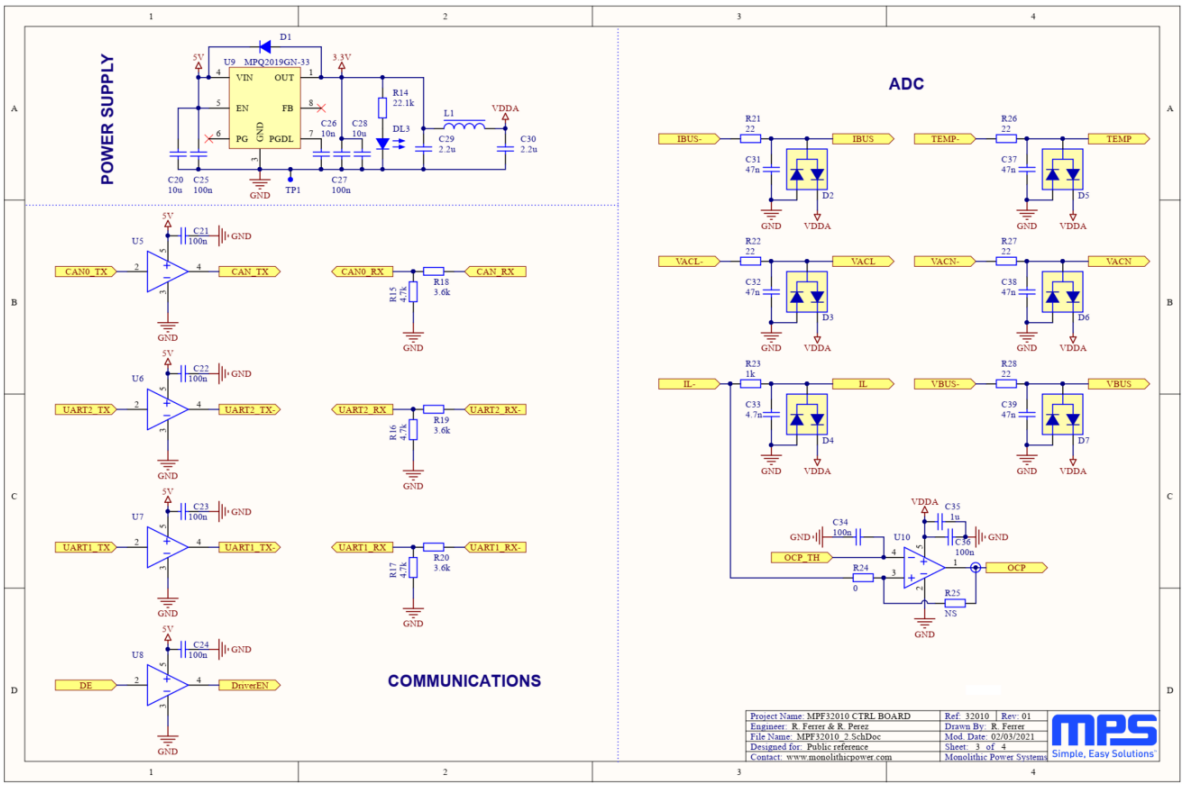


Figure 65: Control Board Schematic 2/3 (MPF32010)

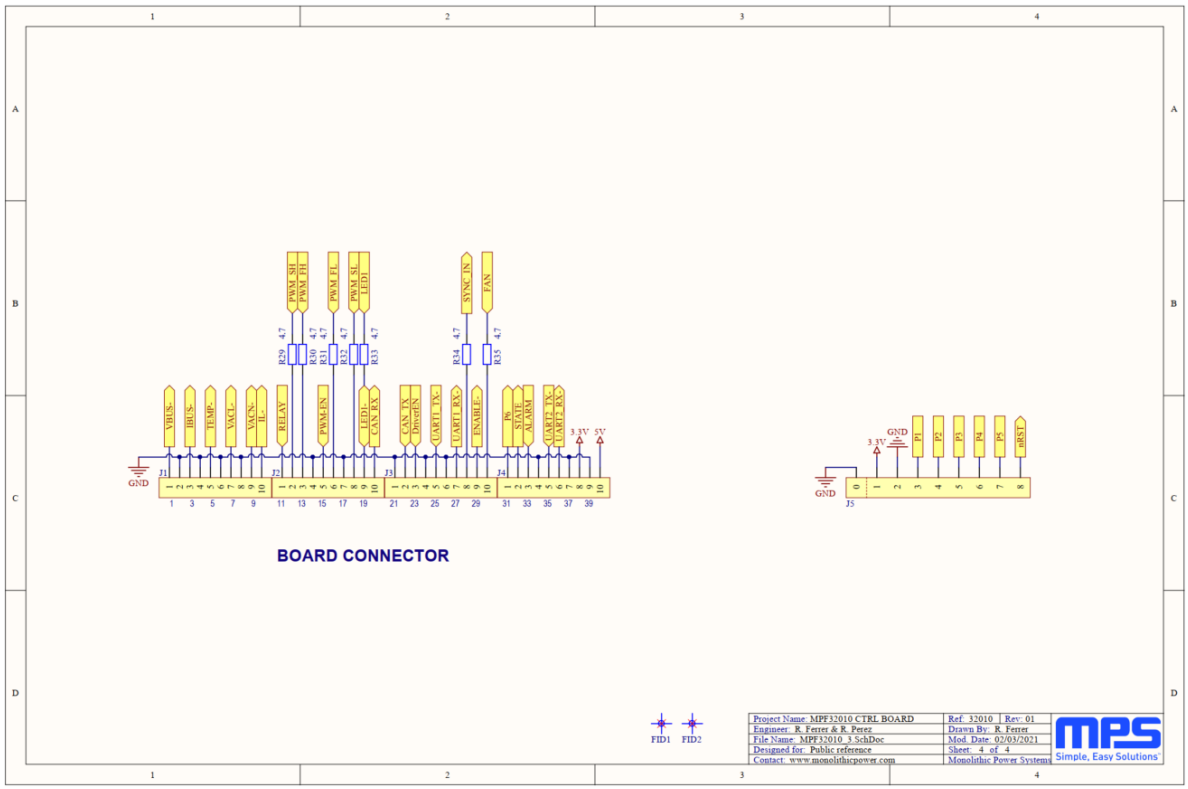


Figure 66: Control Board Schematic 3/3 (MPF32010)

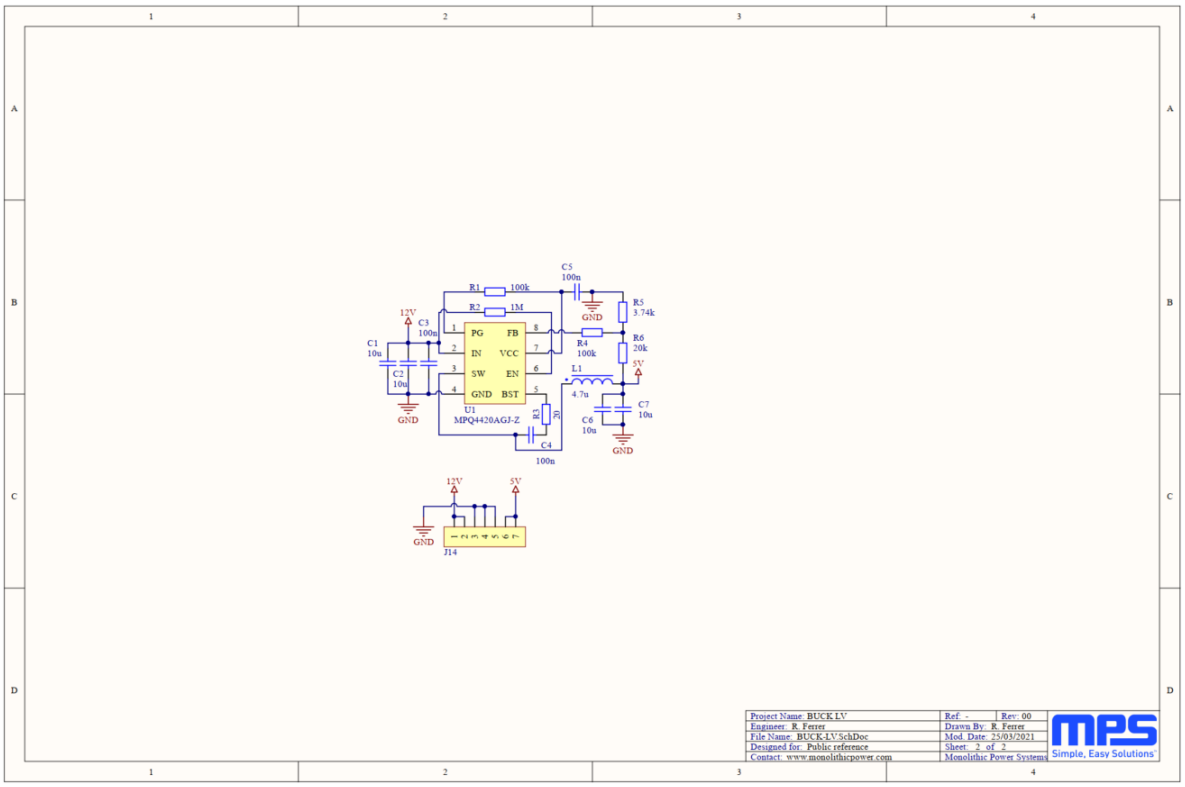


Figure 67: Low-Voltage Buck Schematic (BUCK-LV-00A)

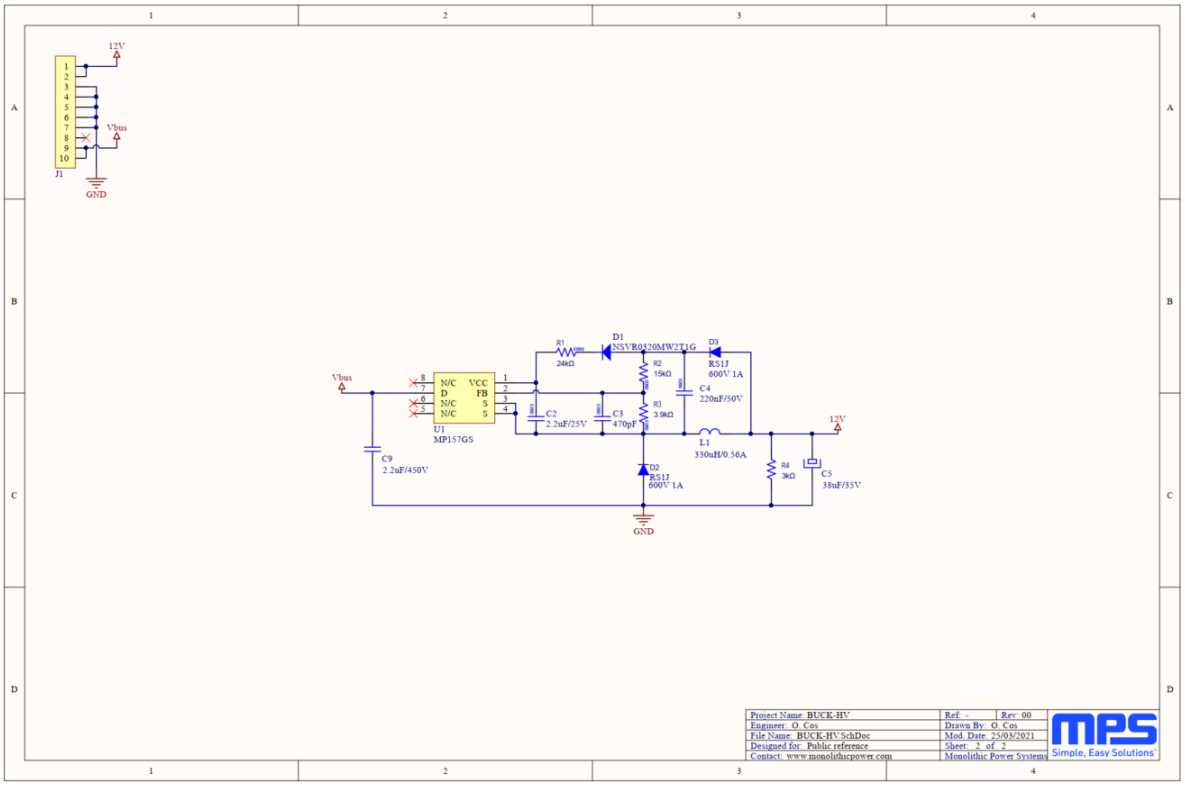


Figure 68: High-Voltage Buck Schematic (BUCK-HV-00A)

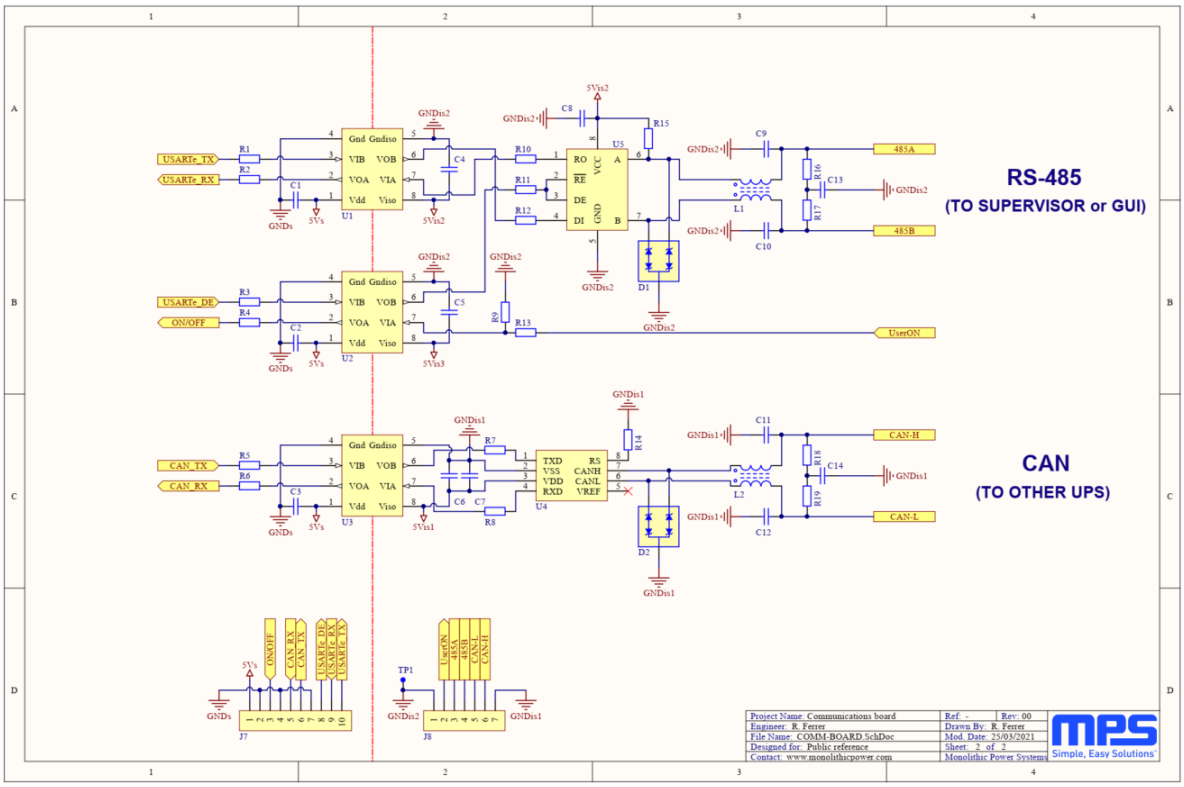
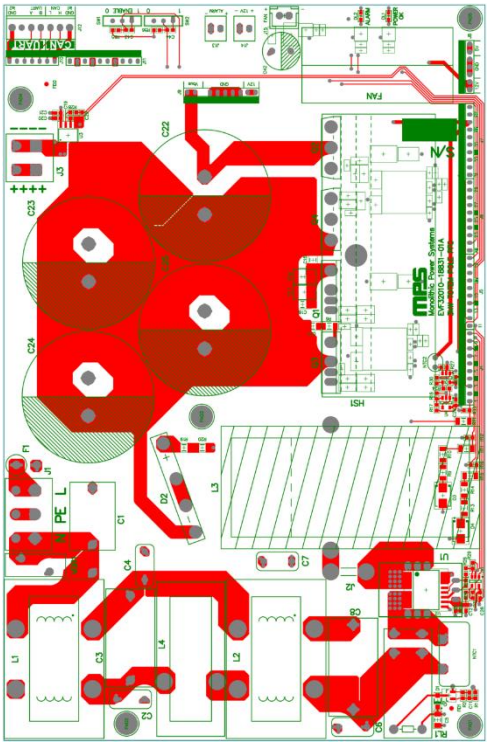
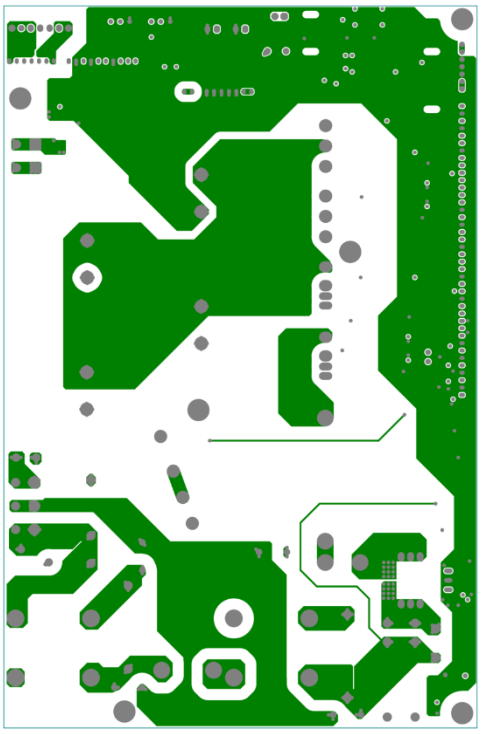


Figure 69: Communications Board Schematic (COMM-BOARD-01A)

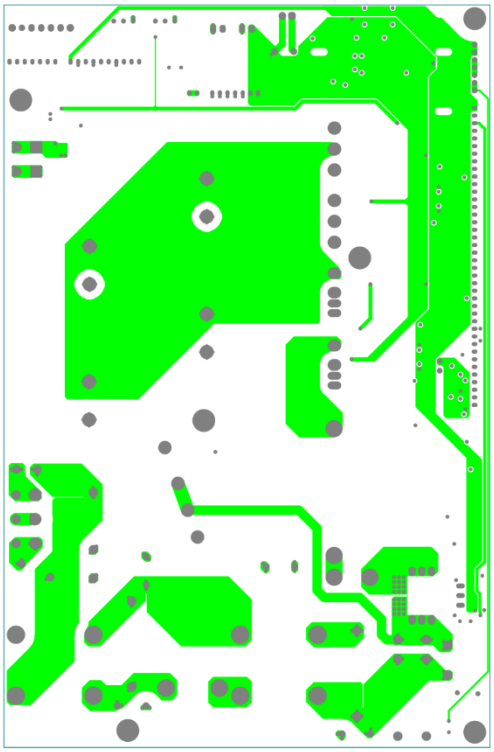
8. PCB Layout



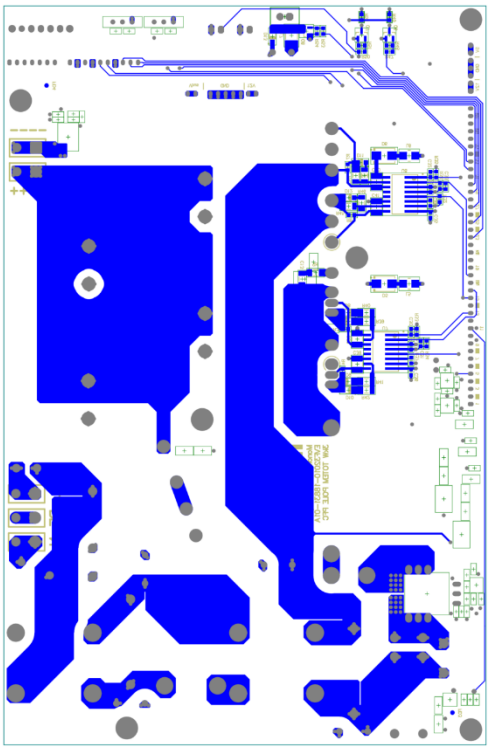
Top Layer



Mid-Layer 1

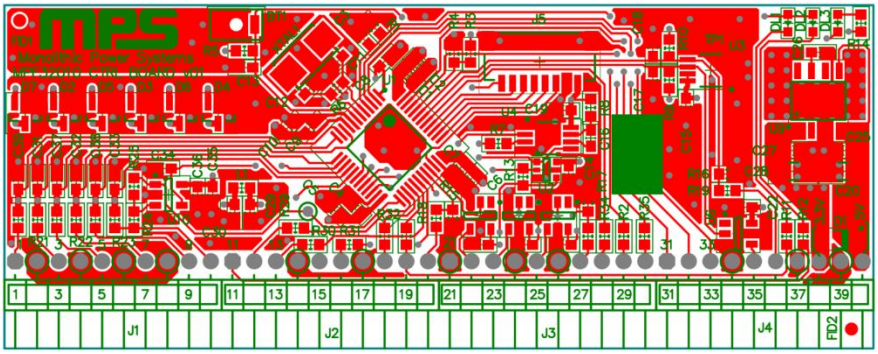


Mid-Layer 2

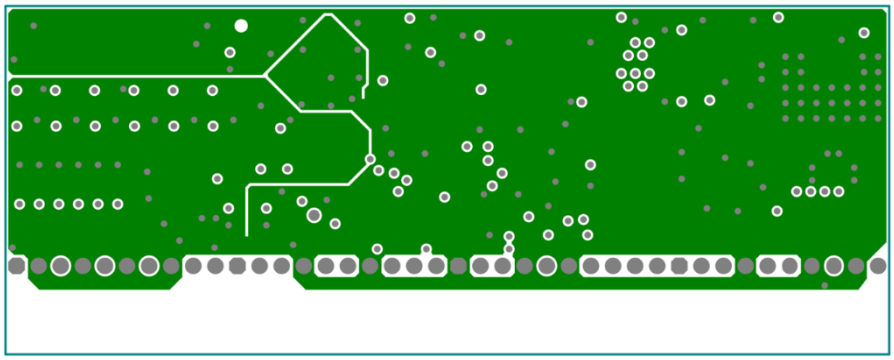


Bottom Layer

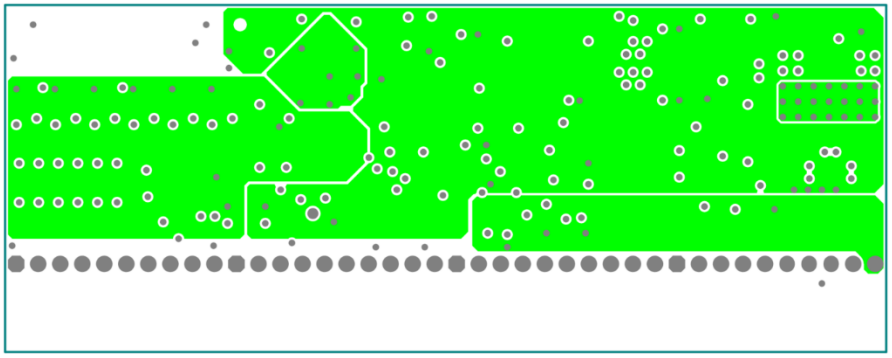
Figure 70: Main Board PCB (EVF32010-18831-01A)



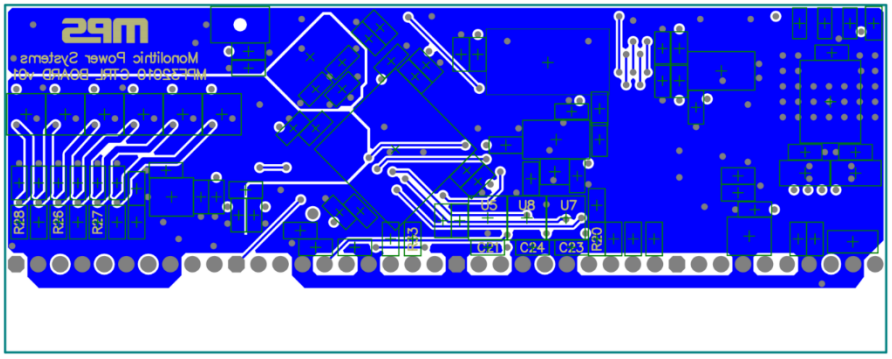
Top Layer



Mid-Layer 1

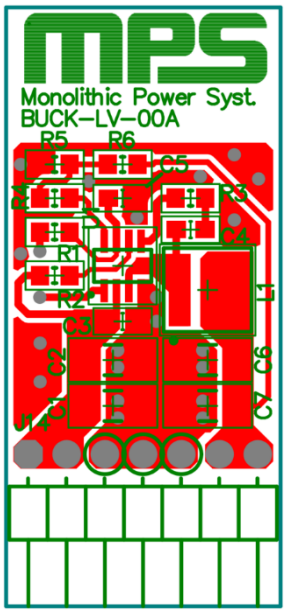


Mid-Layer 2

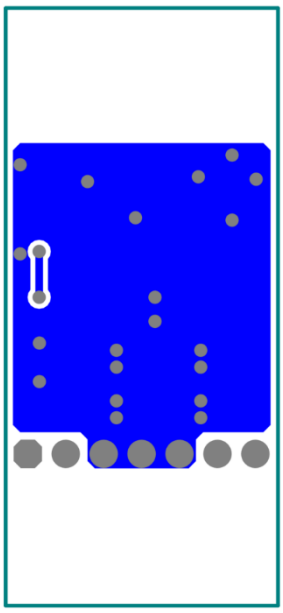


Bottom Layer

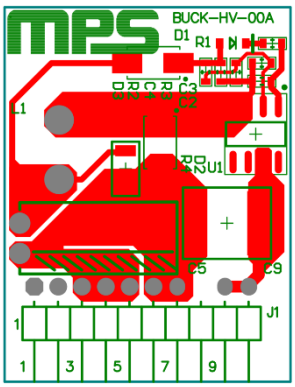
Figure 71: Control Board PCB (MPF32010)



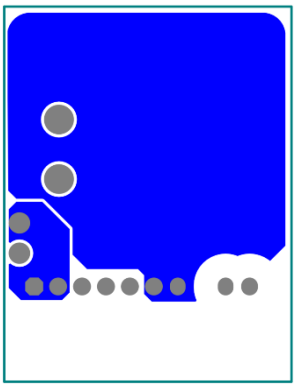
Top Layer (Low-Voltage Buck)



Bottom Layer (Low-Voltage Buck)

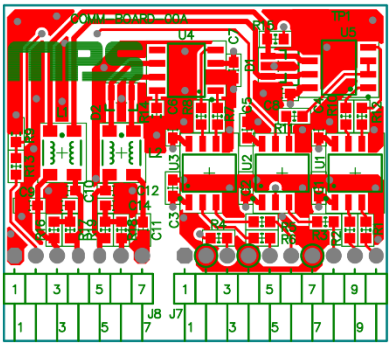


Top Layer (High-Voltage Buck)

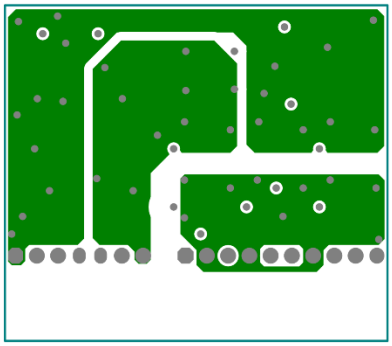


Bottom Layer (High-Voltage Buck)

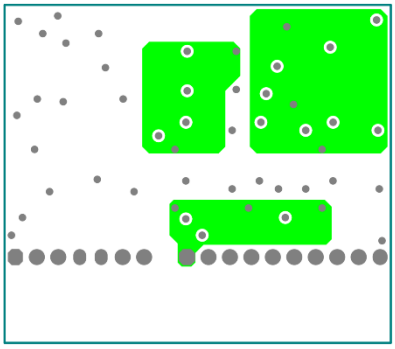
Figure 72: Low-Voltage Buck PCB (BUCK-LV-00A) and High-Voltage Buck PCB (BUCK-HV-00A)



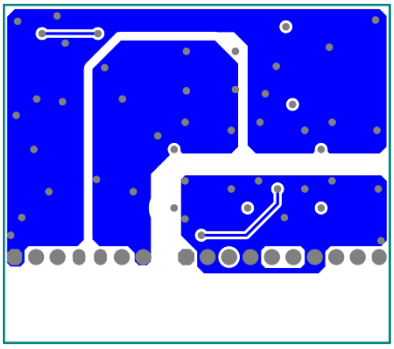
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 73: Communication Board PCB (COMM-BOARD-01A)

9. Bill of Materials

Table 22: Main Board BOM (EVF32010-18831-01A)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1	1µF	Polypropylene (PP) metallized radial film capacitor	18mmx12mm	KEMET	F861BZ105M310A
4	C2, C4, C6, C7	4.7nF	Disc ceramic capacitor	r5.5	KEMET	C947U472MZVDBA 7317
2	C3, C8	2.2µF	Polypropylene (PP) metallized radial film capacitor	26mmx13mm	KEMET	F861DU225M310L
1	C5	100nF	Surface-mount MLCC	1206	KEMET	C1206C104M5 RACTU
4	C9, C10, C11, C29	NS				
8	C12, C19, C20, C26, C27, C28, C43, C44	100nF	Surface-mount MLCC	0603	KEMET	C0603T104K5 RACTU
2	C13, C14	100pF/2kV	Surface-mount MLCC	1206	Johanson Dielectrics Inc.	202R18N101JV4E
2	C15, C16	10nF/630V	Surface-mount MLCC	1206	TDK	CGA5L4C0G2J103J 160AA
2	C17, C18	39nF/500V	Surface-mount MLCC	1812	KEMET	CKC18C393JCGAC AUTO
1	C21	1µF	Surface-mount MLCC	0603	KEMET	C0603C105K8 PACTU
4	C22, C23, C24, C25	470µF/ 450V	Aluminum electrolytic capacitors	r45 d35	Nichicon	LLS2W471MELC
4	C30, C31, C32, C33	47pF	Surface-mount MLCC	0603	Yageo	CC0603JRNPO0 BN470
4	C34, C35, C36, C37	470nF	Surface-mount MLCC	0603	TDK	C1608X7R1C474 K080AC
4	C38, C39, C40, C41	22µF/16V	Surface-mount MLCC	1210	TDK	C3225X5R1C226 M250AA
1	C42	330µF/25V	Aluminum polymer capacitor	r13 d10	Panasonic Electronic Components	25SEPF330M
4	Clip 1, Clip 2, Clip 3, Clip 4	10mmx 20.5mm	Retaining spring	N/A	Fischer Elektronik	THFU3
8	D1, D7, D8, D9, D10, D11, D12, D13	40V/1A	Schottky diode	SOD-123F	On Semiconductor	MBR140SFT1G
1	D2	600V/25A	Rectifier diode	GSIB-5S	Vishay	GSIB2560-E3/45
4	D3, D4, D5, D6	600V/2A	Fast recovery diode	DO-214AA	On Semiconductor	MURS160T3G
1	DB1	N/A	Control board	N/A	N/A	N/A

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	DB2	N/A	Communication board	N/A	N/A	N/A
1	DB3	N/A	Low-voltage buck	N/A	N/A	N/A
1	DB4	N/A	High-voltage buck	N/A	N/A	N/A
1	FAN1	8500rpm	Fan	40x40x10mm	Sunon Fans	MF40101VX-1000U-A99
1	HS1	5.7°C/W	Heatsink	75x30x45mm	Fischer	SK 481/75 SA
1	Isolator 1	1.6W/mK	Thermal insulator	Custom	Bergquist	HF300P-0.001-00-0404
1	J1	6.35mm	3-position PCB terminal block	N/A	Phoenix Contact	1714968
1	J2	N/A	Copper wire	N/A	Any	
1	J3	6.35mm	2-position PCB terminal block	N/A	Phoenix Contact	1714955
6	J4, J5, J6, J7, J9, J11	2mm	10-position socket connector	N/A	Preci-Dip	831-87-010-10-001101
2	J8, J10	2mm	7-position socket connector	N/A	Preci-Dip	831-87-007-10-001101
1	J12	2.54mm	Wire to board terminal block	N/A	Phoenix Contact	1725724
2	J13, J14	2.54mm	Terminal block header, male pins	N/A	TE Connectivity	282834-2
1	J15	2.5mm	Connector header	N/A	JST Sales America	B2B-XH-A(LF)(SN)
1	J16	2mm	Connector housing	N/A	JST Sales America	PHR-2
2	L1, L2	2 x 3mH	Common-mode choke	Custom	Custom	
1	L3	519µH	PFC Coil	Custom	Custom	
1	L4	27µH	EMC Coil	Custom	Custom	
2	L5, L6	49Ω @ 100MHz	Ferrite bead inductor	4mmx3mmx 2.55mm	Multicomp Pro	23NB423226
1	L7	100µH, 0.32A	Shielded wire wound inductor	1812	Murata	LQH43PN101M26L
1	NTC1	30Ω/135J	Inrush current limiter	d17	Ametherm	MS1530004
1	NTC2	10kΩ/3984K	NTC thermistor	Ring lug	Vishay	NTCALUG02A 103G
1	PCB1	EVF32010-18831-01A	MPF32010 EVB	PCB	MPS	EVF32010-18831-01A
2	Pin 1, Pin 2	30AWG to 24AWG	Socket contact tin	N/A	JST Sales America	SPH-002T-P0.5S
2	Q1, Q3	750V/81A	N-channel SiC FET	TO-247-4	UnitedSiC	UJ4C075018K4S
2	Q2, Q4	600V/129A	N-channel MOSFET	PG-TO247	Infineon	IPW60R017C7X KSA1
3	Q5, Q6, Q7	600V/ 340mA	N-channel MOSFET	SC70-3	On Semiconductor	2N7002WT1G

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	Q8	25V/680mA	N-channel digital FET	SOT-23-3	On Semiconductor	FDV303N
4	R1, R47, R50, R53	16Ω	Thick film resistor	0603	Yageo	RT0603FRE0716RL
6	R2, R3, R4, R7, R8, R54	20kΩ	Thick film resistor	0603	Vishay	CRCW060320K0FKEAC
2	R5, R6	10Ω/500V	Thick film resistor	1206	RoyalOhm Semiconductor	KTR18EZPF10R0
9	R9, R10, R11, R13, R14, R15, R19, R20, R21	220kΩ	Thick film resistor	1206	Panasonic	ERJ-UP8F2203V
4	R12, R16, R22, R23	4.7kΩ	Thick film resistor	0603	Vishay	CRCW06034K70JNEAC
11	R17, R18, R32, R33, R34, R35, R36, R48, R51, R55, R56	10kΩ	Thick film resistor	0603	Vishay	CRCW060310K0FKECC
1	R24	1kΩ	Thick film resistor	0603	Vishay	CRCW06031K00FKEA
2	R25, R29	110kΩ	Thick film resistor	0603	Vishay	CRCW0603110KFKEA
2	R26, R31	18.7kΩ	Thick film resistor	0603	Vishay	CRCW060318K7FKEA
1	R27	1.91kΩ	Thick film resistor	0603	Vishay	CRCW06031K91FKEA
1	R28	0Ω	Thick film resistor	0603	Vishay	CRCW06030000Z0EA
1	R30	1.05kΩ	Thick film resistor	0603	Vishay	CRCW06031K05FKEA
2	R37, R38	NS				
2	R39, R41	20Ω	Thick film resistor	1206	Vishay	CRCW120620R0FKEA
4	R40, R42, R44, R46	4.7Ω	Thick film resistor	1206	Vishay	CRCW12064R70FKEA
2	R43, R45	16Ω	Thick film resistor	1206	Vishay	CRCW120616R0FKEA
2	R49, R52	22.1kΩ	Thick film resistor	0603	Vishay	CRCW060322K1FKEA
1	RL1	16A/12V	General-purpose relay	SPST-NO	TE Connectivity	4-1393240-5
1	Screw1	M3x10	Screw	M3, 10mm	Any	
5	Spacer 1, Spacer 2, Spacer 3, Spacer 4, Spacer 5	M3x70	Steel spacer	M3, 70mm	Wurth	971700321

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
5	Spacer 6, Spacer 7, Spacer 8, Spacer 9, Spacer 10	M3x30	Steel spacer	M3, 30mm	RS	806-6617
1	Spacer 11	M3 6.3x3	Plastic spacer	M3, 30mm	Duratool	DT000286
1	SW1	12V/ 500mA	Slide switch	10mmx 6.4mmx 2.5mm	Wurth	450301014042
1	SW2	NS	Slide switch	10mmx 6.4mmx 2.5mm	Wurth	450301014042
1	U1	25A	Current sensor	N/A	LEM USA	CAS25-NP
1	U3	MCS1802	Linear Hall-effect current sensor	8-SOIC	MPS	MCS1802GS-10
3	U4, U5, U6	5.5V, 10MHz	Operational amplifier	SOT23	Analog Devices	AD8605ARTZ-REEL7
2	U7, U8	MP18831	Half-bridge gate driver	SOIC-16	MPS	MP18831-4CGY
1	VDR1	$300V_{AC}$	Varistor	r7	TDK	B72214P2301K101

Table 23: Control Board BOM (MPF32010)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	BT1	12V/ 50mA	Button	N/A	Omron	B3U-1000P
17	C1, C3, C4, C6, C8, C9, C13, C14, C19, C21, C22, C23, C24, C25, C27, C34, C36	100nF	Surface-mount MLCC	0603	KEMET	C0603T104K5 RACTU
5	C2, C5, C7, C10, C35	1µF	Surface-mount MLCC	0603	KEMET	C0603C105K8 PACTU
2	C11, C12	15pF	Surface-mount MLCC	0603	KEMET	C0603C150F5 GACTU
3	C15, C17, C18	NS				
1	C16	2nF	Surface-mount MLCC	0603	AVX	06033C202KAT2A
2	C20, C28	10µF	Surface-mount MLCC	1206	Murata	GCM31CR71C106 KA64L
1	C26	10nF	Surface-mount MLCC	0603	KEMET	C0603C103K1RA C7411
2	C29, C30	2.2µF	Surface-mount MLCC	0603	TDK	CGA3E1X7R0J225 K080AC
5	C31, C32, C37, C38, C39	47nF	Surface-mount MLCC	0603	KEMET	C0603C473K5 NAUTO
1	C33	4.7nF	Surface-mount MLCC	0603	KEMET	C0603C472K4RE CAUTO
1	D1	40V/ 350mA	Schottky diode	SOD-123	STMicro-electronics	BAT48ZFILM
6	D2, D3, D4, D5, D6, D7	30V/ 200mA	Rectifier diode	SOT-23-3	On Semiconductor	BAT54S
3	DL1, DL2, DL3	3.2V	Green LED	0603	Wurth	150060GS75000
4	J1, J2, J3, J4	2mm	Right-angle connector header	N/A	Preci-Dip	830-80-010-20-001101
1	J5	1mm	Right-angle connector header	N/A	JST Sales America	SM08B-SRSS-TB(LF)(SN)
1	L1	120Ω @ 100MHz	Ferrite bead	0603	Murata	BLM18PG121SN1D
4	R1, R15, R16, R17	4.7kΩ	Thick film resistor	0603	Vishay	CRCW06034K70 FKEA
4	R2, R18, R19, R20	3.6kΩ	Thick film resistor	0603	Vishay	CRCW06033K60 FKEA
5	R3, R9, R10, R13, R25	NS	Thick film resistor			
2	R4, R23	1kΩ	Thick film resistor	0603	Vishay	CRCW06031K00 FKEA
1	R5	10kΩ	Thick film resistor	0603	Vishay	CRCW060310K0 FKEA
1	R6	1MΩ	Thick film resistor	0603	Vishay	CRCW06031M00 FKEA
1	R7	4.75kΩ	Thick film resistor	0603	Vishay	CRCW06034K75 FKEA

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	R8	20kΩ	Thick film resistor	0603	Vishay	CRCW060320K0FKEA
3	R11, R12, R14	22.1kΩ	Thick film resistor	0603	Vishay	CRCW060322K1FKEA
5	R21, R22, R26, R27, R28	22Ω	Thick film resistor	0603	Vishay	CRCW060322K0FKEA
1	R24	0Ω	Thick film resistor	0603	Vishay	CRCW06030000Z0EA
7	R29, R30, R31, R32, R33, R34, R35	4.7Ω	Thick film resistor	0603	Vishay	CRCW06034R70FKEA
1	TP1	1.5mm	Test point	N/A	Keystone	5015
1	U1	MPF32010	Totem-pole PFC controller	LQFP48	MPS	MPF32010GFP-4P
1	U2	CMOS/LVTTL	AND gate IC	5-TSSOP	Nexperia	74LVC1G08GW125
1	U3	NS	EEPROM	8-TSSOP	STMicroelectronics	M24128-BRDW6TP
1	U4	CMOS/LVTTL	Multivibrator	8-TSSOP	Nexperia	74LVC1G123DP125
4	U5, U6, U7, U8	TTL	Non-inverting buffer	5-TSSOP	On Semiconductor	M74VHC1GT50DTT1G
1	U9	MPQ2019	Linear voltage regulator	SOIC-8	MPS	MPQ2019GN-33
1	U10	5V, 470μA	Comparator	SOT23-5	STMicroelectronics	TS3011ILT
1	XTAL1	8MHz	Crystal	2-SMD	Abracon	ABM7-8.000MHZ-D2Y-T

Table 24: Low-Voltage Buck BOM (BUCK-LV-00A)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	C1, C2, C6, C7	10μF	Surface-mount MLCC	1206	Murata	GCM31CR71C106KA64L
3	C3, C4, C5	100nF	Surface-mount MLCC	0603	KEMET	C0603T104K5RACTU
1	J14	2mm	Right-angle connector header	N/A	Preci-Dip	830-80-007-20-001101
1	L1	4.7μF	Unshielded molded Inductor	2-SMD	MPS	MPL-AL4020-4R7
2	R1, R4	100kΩ	Thick film resistor	0603	Vishay	CRCW0603100KFKEA
1	R2	1MΩ	Thick film resistor	0603	Vishay	CRCW06031M00FKEA
1	R3	20Ω	Thick film resistor	0603	Vishay	CRCW060320R0FKEA
1	R5	3.74kΩ	Thick film resistor	0603	Vishay	CRCW06033K74FKEA
1	R6	20kΩ	Thick film resistor	0603	Vishay	CRCW060320K0FKEA
1	U1	MPQ4420A	Synchronous step-down converter	TSOT23-8	MPS	MPQ4420AGJ-Z

Table 25: High-Voltage Buck BOM (BUCK-HV-00A)

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C2	2.2µF/25V	Surface-mount MLCC	0603	TDK	C1608X5R1E225K080AE
1	C3	470pF	Surface-mount MLCC	0603	KEMET	C0603C471J5GAC7411
1	C4	220nF/50V	Surface-mount MLCC	0603	Murata	GCM188R71H224KA64J
1	C5	68µF/35V	Aluminum electrolytic capacitors	r2.54 d6.3	Panasonic	EEU-FM1V680B
1	C9	2.2µF/450V	MLCC	2220	TDK	C5750X6S2W225K250KA
1	D1	23V, 1A	Schottky diode	SOD-323	onsemi	NSVR0320MW2T1G
2	D2, D3	600V, 1A	Standard diode	DO-214AC	Diodes, Inc.	RS1J-13-F
1	J1	N/A	Right-angle connector header	N/A	Preci-Dip	830-80-010-20-001101
1	L1	330µH/ 0.56A	Unshielded wire wound inductor	r4.25	Bourns, Inc.	RLB0913-331K
1	R1	24kΩ	Thick film resistor	0603	Vishay	CRCW060324K0FKEA
1	R2	15kΩ	Thick film resistor	0603	Vishay	CRCW060315K0FKEA
1	R3	3.9kΩ	Thick film resistor	0603	Vishay	CRCW06033K90FKEA
1	R4	3kΩ	Thick film resistor	1206	Vishay	CRCW12063K00FKEA
1	U1	MP157	Offline primary-side regulator	SOIC-8	MPS	MP157GS

10. Inductive Components

INDUCTIVE COMPONENT

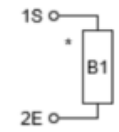
CODE	EVF32010-L3v7
DESIGNER	R. Ferrer

MATERIALS LIST

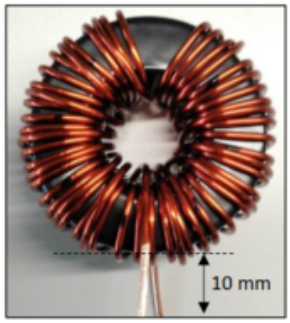
Quantity	Units	Description
1	-	Toroidal core 61x32x25mm. Chang Sung CH610060GT (Titanium).
4.7	m	Copper wire Ø = 2mm

WINDINGS			Turns	WIRE			PINOUT		TUBE		INSULATORS		ELECTRIC	
#	Start	End		Ø	Class	Color	Start	End	Start	End	Layers	Mater.	mΩ	µH
B1	1S	2E	52	2	F	-	-	-	No	No	No	No	31	519

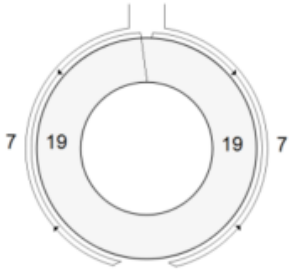
ELECTRIC SCHEME



ASSEMBLY DETAILS



ASSEMBLY DETAILS



MANUFACTURING NOTES

The winding occupies two layers, the inner one which has 38 turns and the outer one with 14.

VERIFICATION

Inductance	B1 = 519 uH (±10%)		
DCR	B1 = 31 mΩ (±10%)		
Turns ratio	-		
Dielectric strength	Connect pins	Voltage	Connect pins
	-	-	-

EDITION	DATE	MODIFICATION
7	Mar.4, 2021	---
8		
9		

Figure 74: PFC Coil (L3)

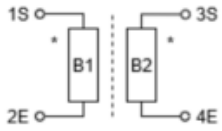
	INDUCTIVE COMPONENT	CODE	EVF32010-L1L2
		DESIGNER	R. Ferrer

MATERIALS LIST

Quantity	Units	Description
1	-	Toroidal core 30x20x10mm. Magnetec M-1016.
47 x2	mm	Copper wire Ø = 2mm
1	-	Separator (18x12x1.6mm)

WINDINGS			Turns	WIRE			PINOUT		TUBE		INSULATORS		ELECTRIC	
#	Start	End		Ø	Class	Color	Start	End	Start	End	Layers	Mater.	mΩ	mH
B1	1S	2E	8	2	F	-	-	-	No	No	No	No	7	3
B2	3S	4E	8	2	F	-	-	-	No	No	No	No	7	3

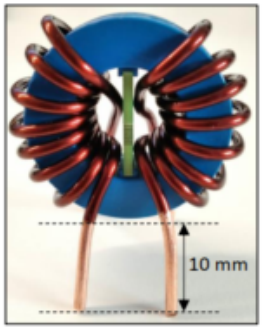
ELECTRIC SCHEME



ASSEMBLY DETAILS

MANUFACTURING NOTES

ASSEMBLY DETAILS



VERIFICATION

Inductance	B1 = B2 = 3 mH (±10%)		
DCR	B1 = B2 = 7 mΩ (±10%)		
Turns ratio	-		
Dielectric strength	Connect pins	Voltage	Connect pins
	-	-	-

EDITION	DATE	MODIFICATION
1	Jul.28, 2020	---
2		
3		

Figure 75: Common Mode Choke (L1 and L2)

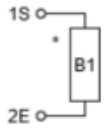
INDUCTIVE COMPONENT	CODE	EVF32010-L9v0
	DESIGNER	R. Ferrer

MATERIALS LIST

Quantity	Units	Description
1	-	Toroidal core 33x20x10mm. Chang Sung CH330060.
1	m	Copper wire Ø = 2mm

WINDINGS			Turns	WIRE			PINOUT		TUBE		INSULATORS		ELECTRIC	
#	Start	End		Ø	Class	Color	Start	End	Start	End	Layers	Mater.	mΩ	µH
B1	1S	2E	21	2	F	-	-	-	No	No	No	No	9	27

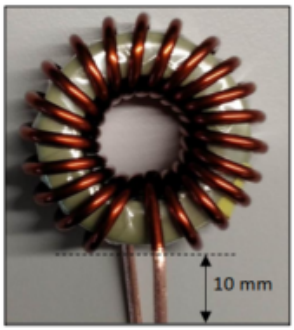
ELECTRIC SCHEME



ASSEMBLY DETAILS

MANUFACTURING NOTES

ASSEMBLY DETAILS



VERIFICATION

Inductance	B1 = 27 uH (±10%)		
Turns ratio	-		
Dielectric strength	Connect pins	Voltage	Connect pins
	-	-	-

EDITION	DATE	MODIFICATION
1	Jan.25, 2021	---
2		
3		

Figure 76: EMC Coil (L4)

11. Heatsink

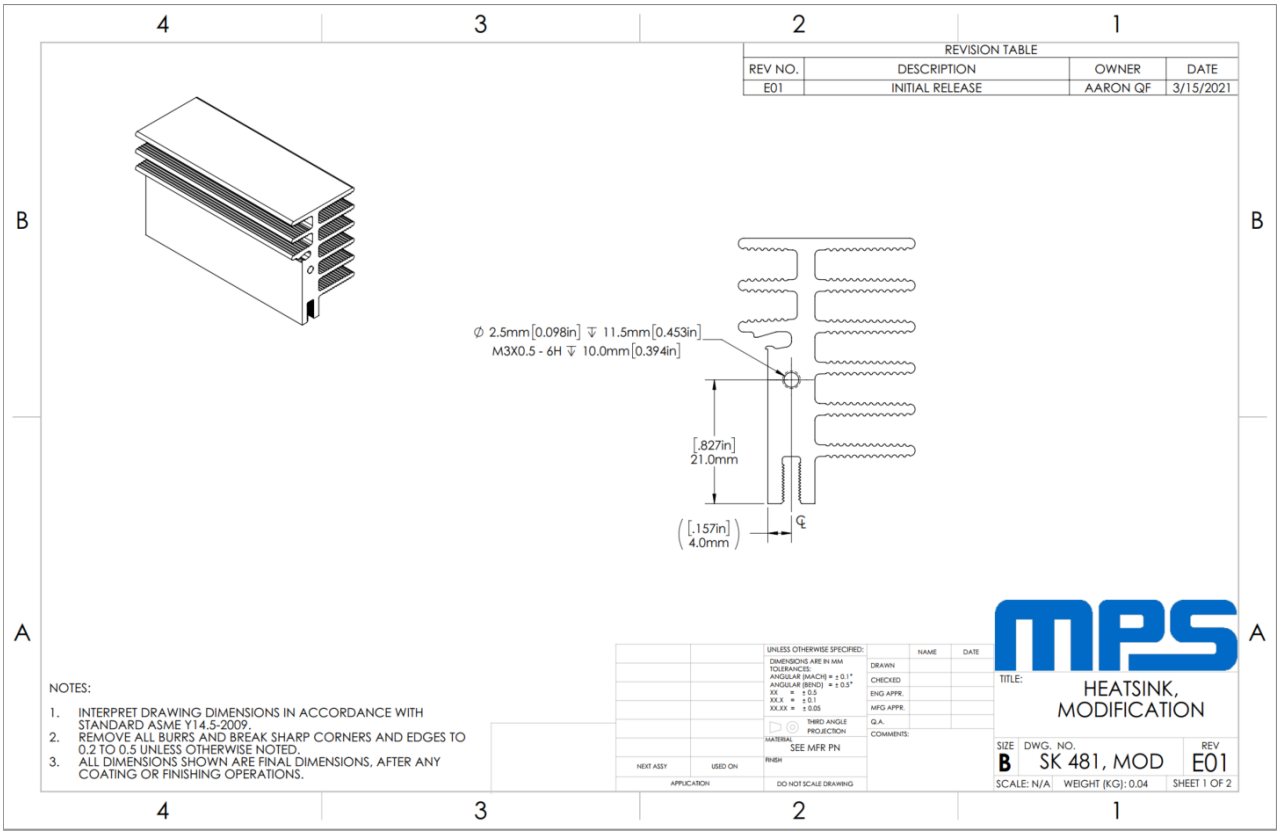


Figure 77: Heatsink Drilling (HS1)

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/14/2021	Initial Release	-
1.01	5/12/2022	Updated the efficiency min value from “985%” to “0.985” in Table 2	6
		Updated table numbers; updated figure numbers; updated pagination; grammar and formatting updates	All