Computing / Server Roadmap

Qian Ouyang

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Confidential – Subject to Confidentiality Agreement/NDA

Controller Families Supporting High Performance Computing

	Released to Production				Sampling				2019/20			
									Q3	Q4	Q1	Q2
Intel Xeon Processor	**MP2955A** 7-ph/ 2-rail VR13	**MP2965** 7-ph/ 2-rail VR13.HC			**MP2975** 8-ph/ 2-rail VR13.HC	**MP2972** 12-ph/ 2-rail VR13.HC	**MP2971** 8-ph/ 2-rail VR14			**MP2985** 9-ph/ 2-rail VR14		
Intel IMVP	**MP2949A** 6-ph/ 3-rail IMVP8				**MP2940A** 3-ph/ 1-rail IMVP9	**MP2950A** 6-ph/ 1-rail IMVP9	**MP2943** 7-ph/ 2-rail IMVP9					
AMD Gaming SoC	**MP2853** 5-ph/ 2-rail SVI2				**MP2855** 9-ph/ 2-rail SVI2	**MP2926** 6-ph/ 3-rail AVS						
AMD Server Processor	**MP2853** 5-ph/ 2-rail SVI2				**MP2855** 9-ph/ 2-rail SVI2	**MP2852** 13-ph/ 2-rail SVI2				**MP2856** 8-ph/ 2-rail SVI3	**MP2857** 12-ph/ 2-rail SVI3	
Nvidia GPU	**MP2888A** 10-ph/ 1-rail OVR4+	**MP2886A** 6-ph/ 1-rail OVR4+	**MP2884A** 4-ph/ 1-rail OVR4+		**MP2988** 3-ph/ 1-rail OVR3i							
AI Processor	**MP2965** 7-ph/ 2-rail AVS				**MP2975** 8-ph/ 2-rail AVS	**MP2852** 13-ph/ 2-rail AVS	**MP2927** 9-ph/ 3-rail AVS			**MP2882** 16-ph/ 2-rail AVS	**MP2883** 20-ph/ 2-rail AVS	
48V Data Center					**MP2981** LLC Prim/Sec Controller							

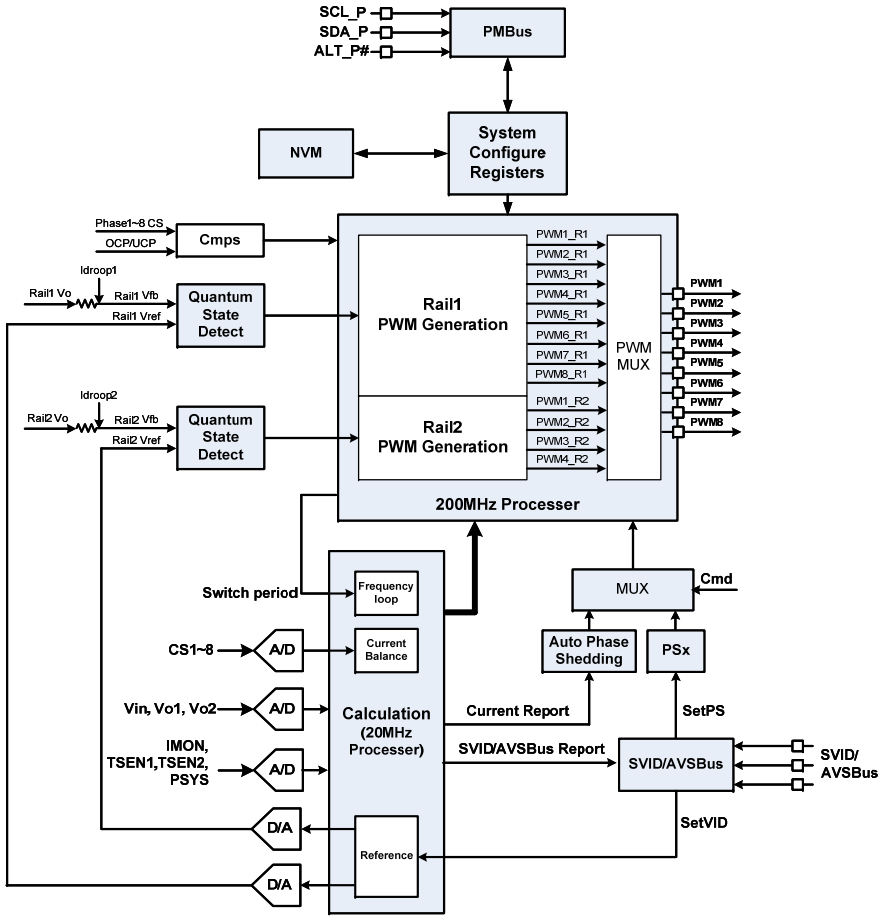
Released

Sampling

In Design

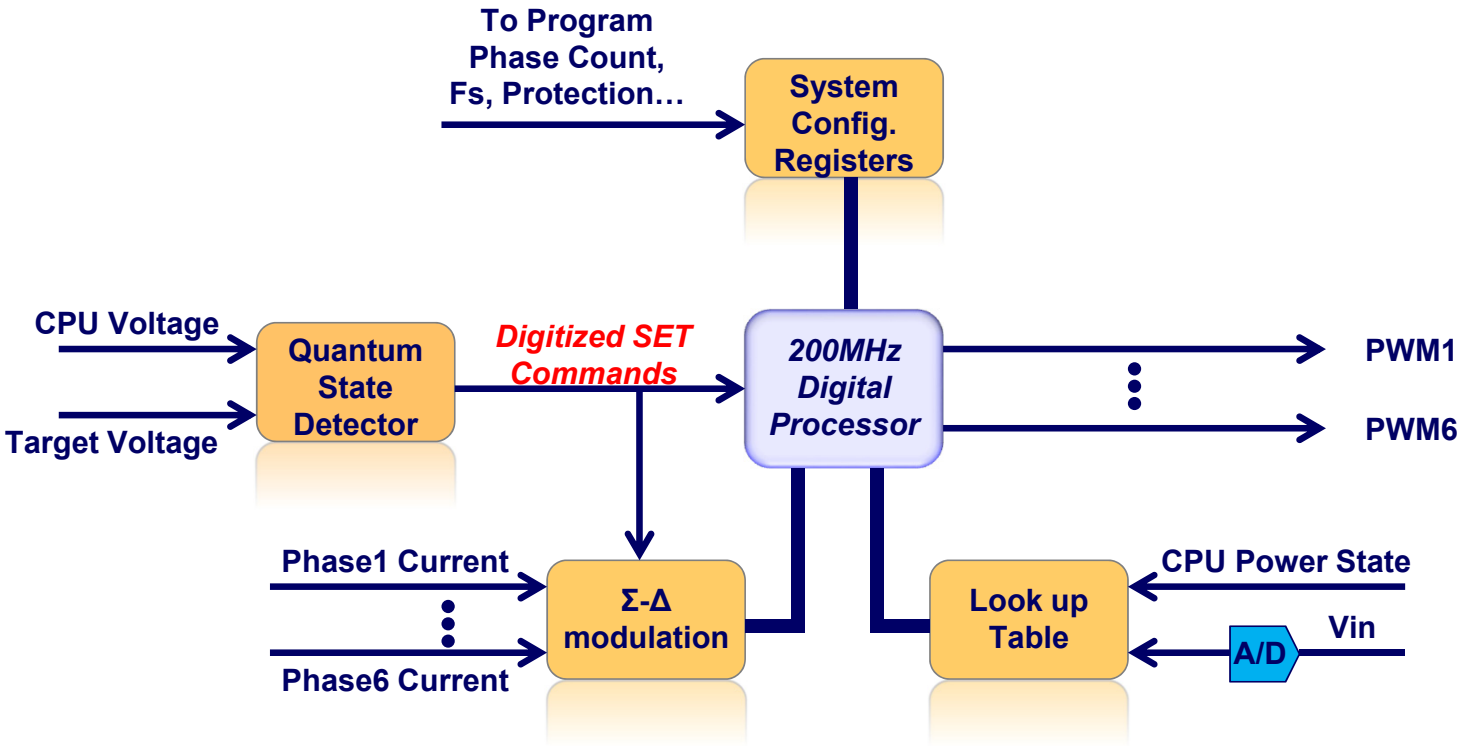
Digital Multi-phase Controller for VR13HC

- Dual Loop, Flexible Phase Assignment
- Patented Constant on-time Control: Best Transient in the Market
- All Digital Control via PMBUS
- Common-Foot Print (CFP)
- Minimal External Components
- Telemetry
  - Vin, Vo, Iin, Iout, Pin, Pout
  - Peak Current Detection
  - Temperature
- Advanced Fault Handling
  - OCP, OVP, UVP, OTP
  - Cycle-by-cycle OC/UC
  - Catastrophic Failure Protection
  - Black Box
- Enhanced PMBUS Security
  - Required by Intel VR13HC/VR14



MPS Digital Control Highlights

MPS Digital Control

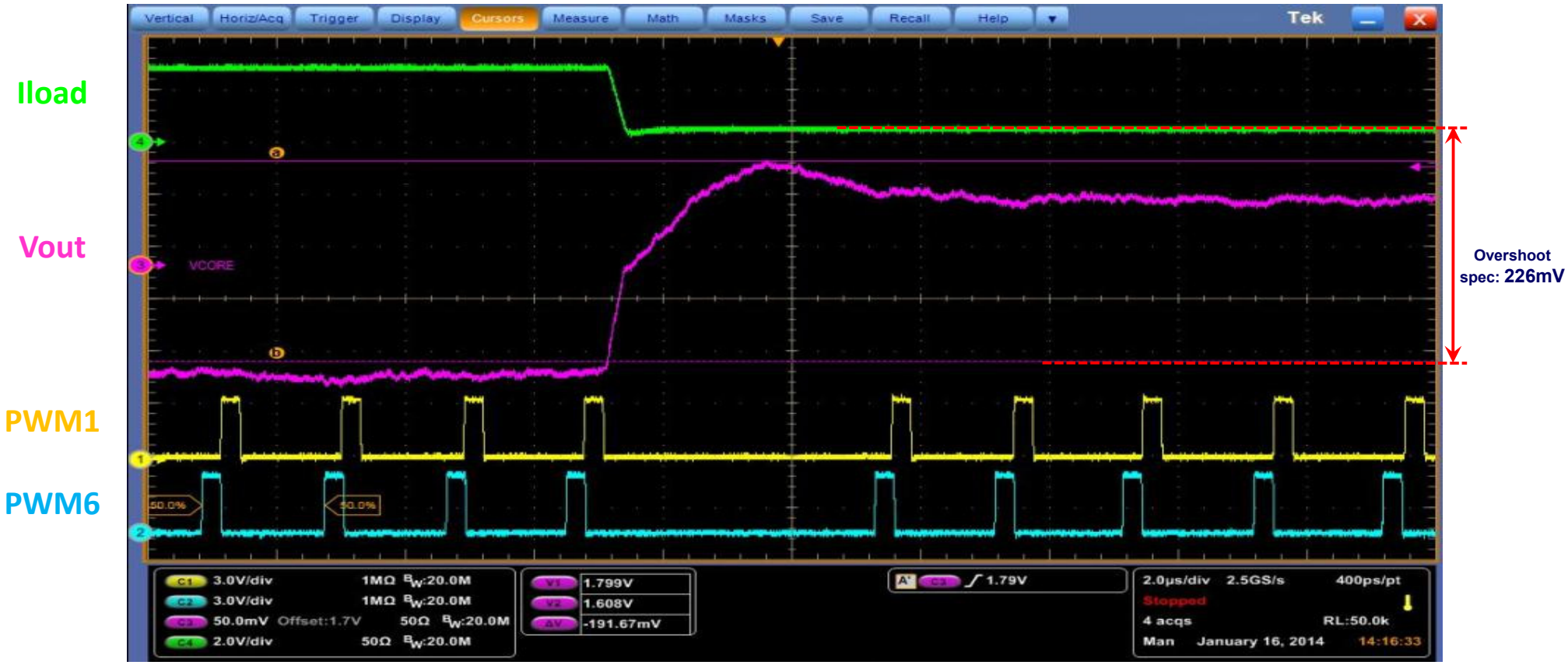


MPS Digital COT Modulation-Load Step Up



No Ring back when load step up.

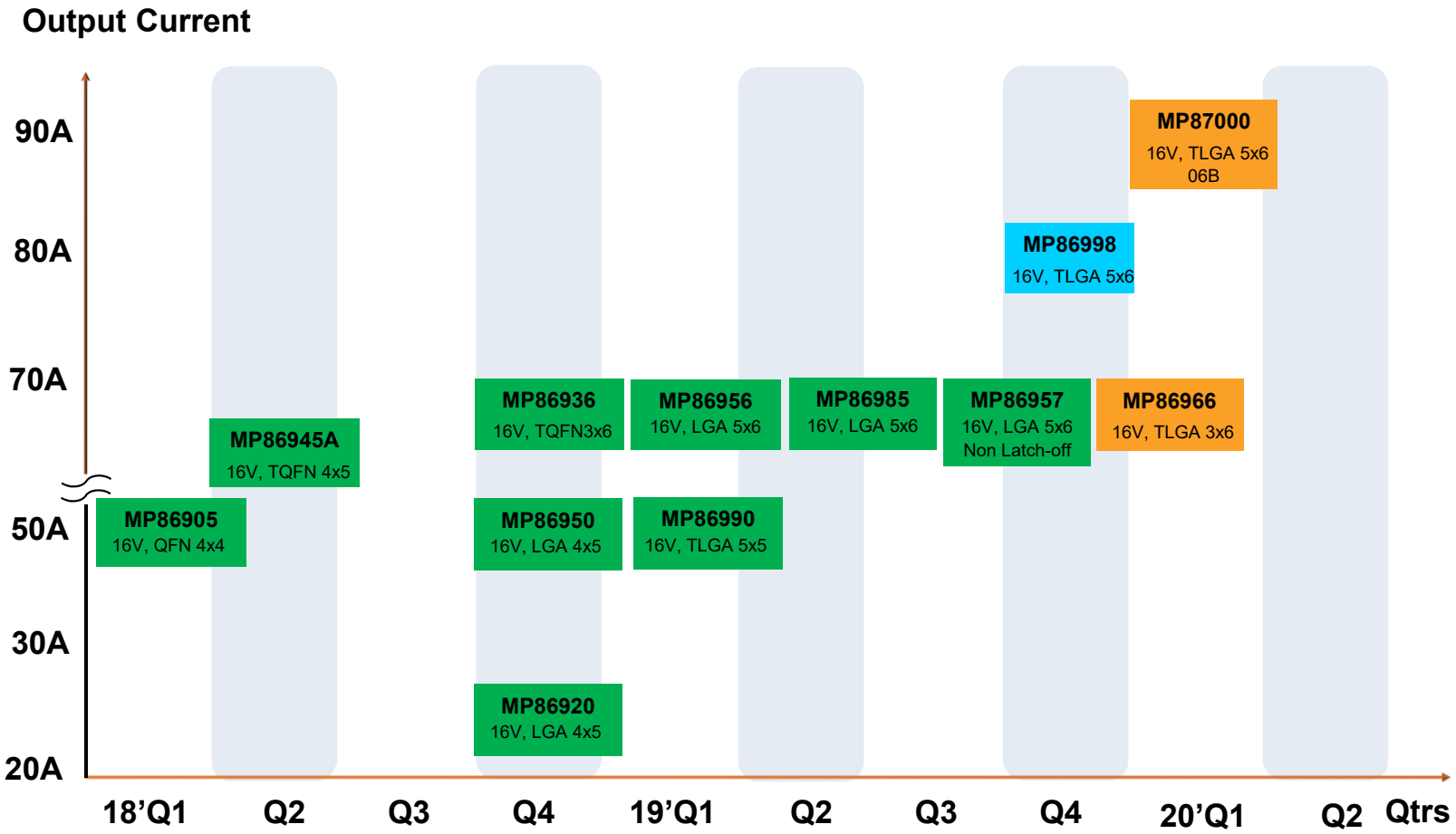
MPS Digital COT Modulation-Load Step Down



Overshoot is reduce by Non-linear digital control.

Intelli-Phase Roadmap--HV

LGA5x6 is 5x6 Common Footprint
LGA4x5 is 4x5 Common Footprint



RoHS COMPLIANT

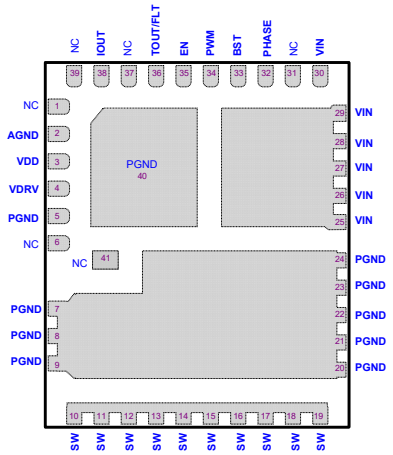
Released

Sampling

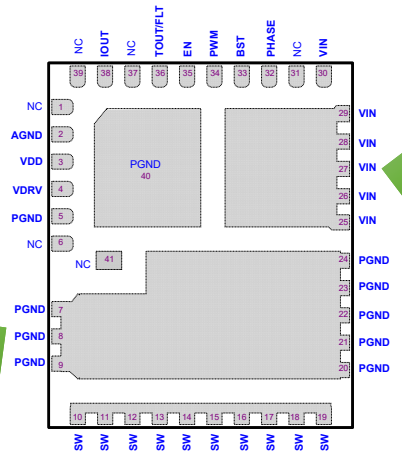
In Design

80A/90A Intelli-phase in 5x6 Common Footprint

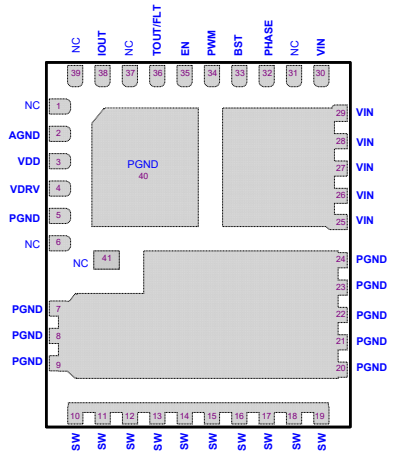
- Continuous Current up to 80A/90A
- Peak Current up to 110A
- Supports up to 3MHz Fsw
- Built-In ZCD, OCP, NOCP, OTP, SCP
- Current Sense Tolerance ±2%
- 5x6 Common Foot-print
- P2P with MP86956



MP86956, 70A

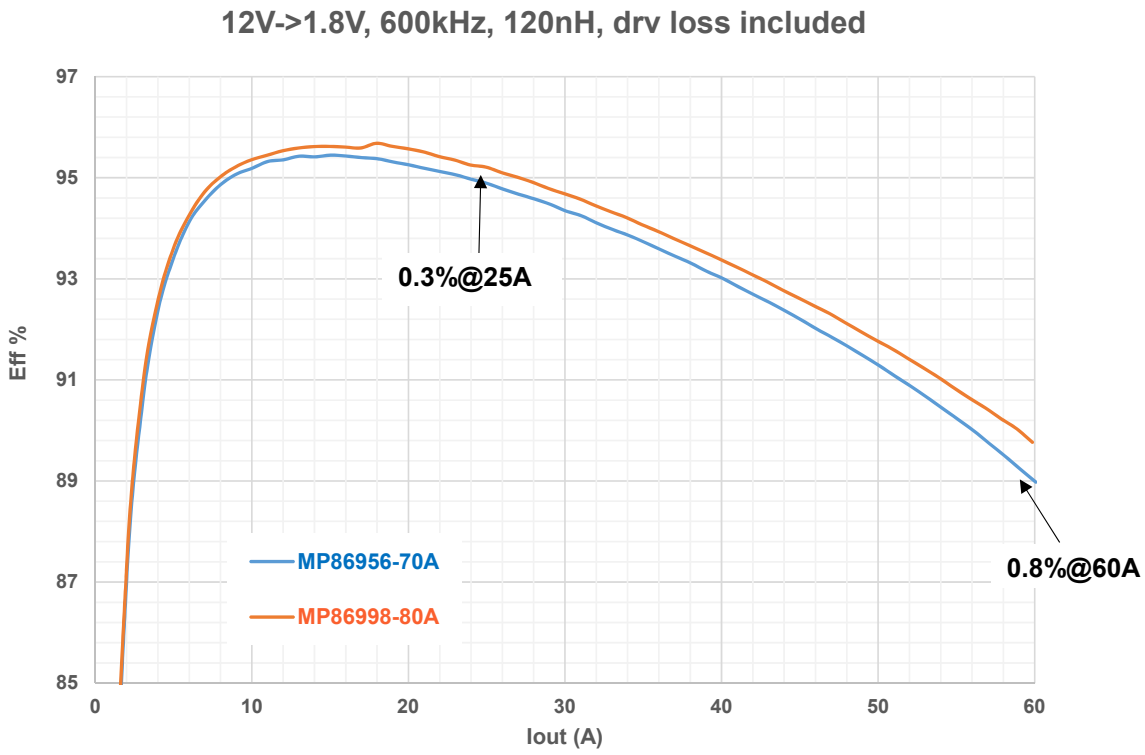


MP86988, 80A



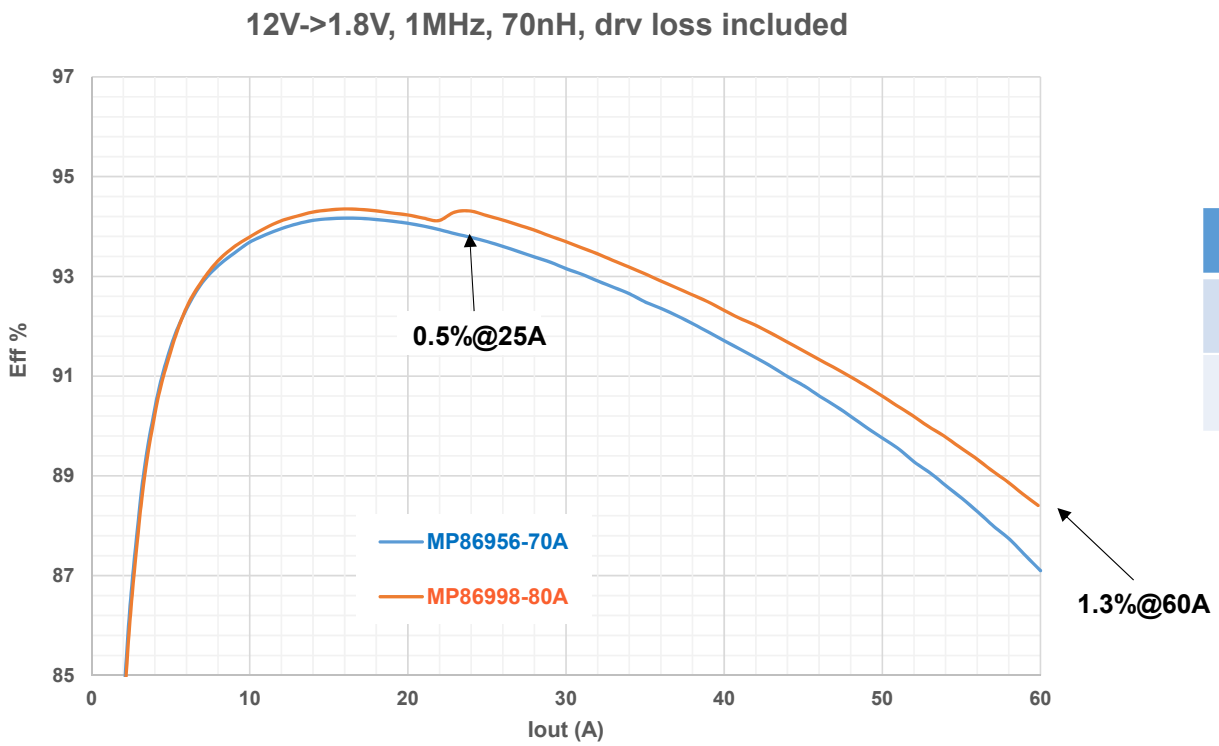
MP87000, 90A

Efficiency – 1.8V 600kHz



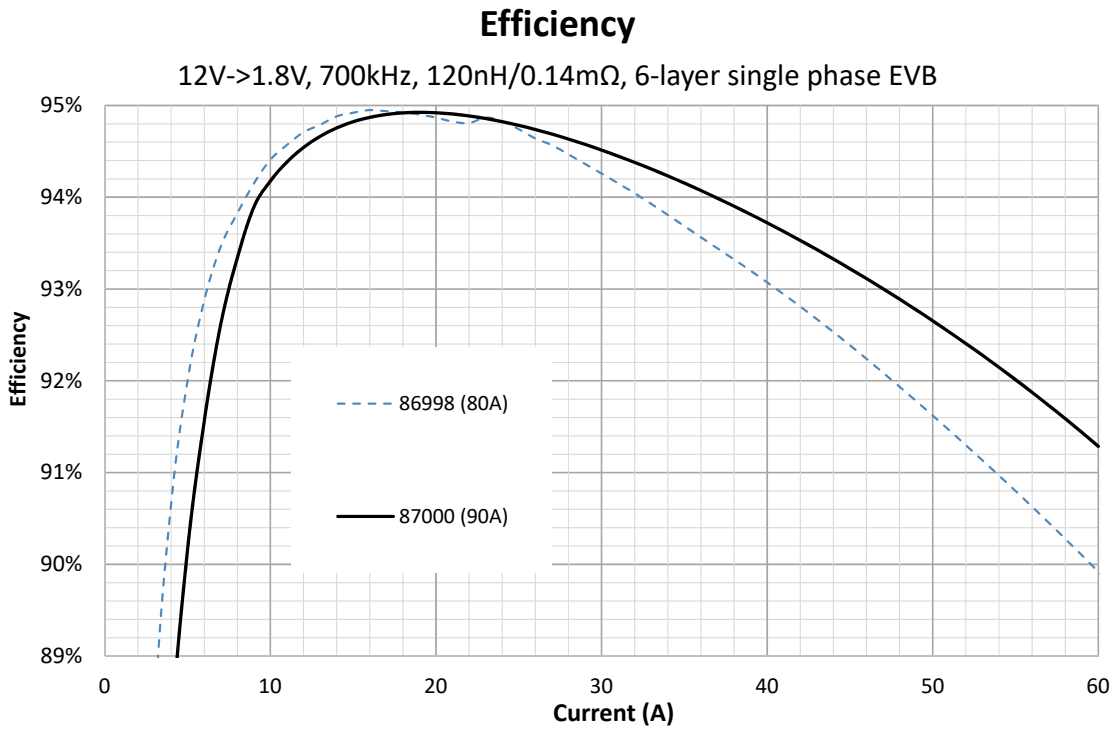
	25A	60A
MP86956	94.89%	88.98%
MP86998	95.21%	89.77%

Efficiency – 1.8V 1MHz



	25A	60A
MP86956	93.70%	87.10%
MP86998	94.22%	88.41%

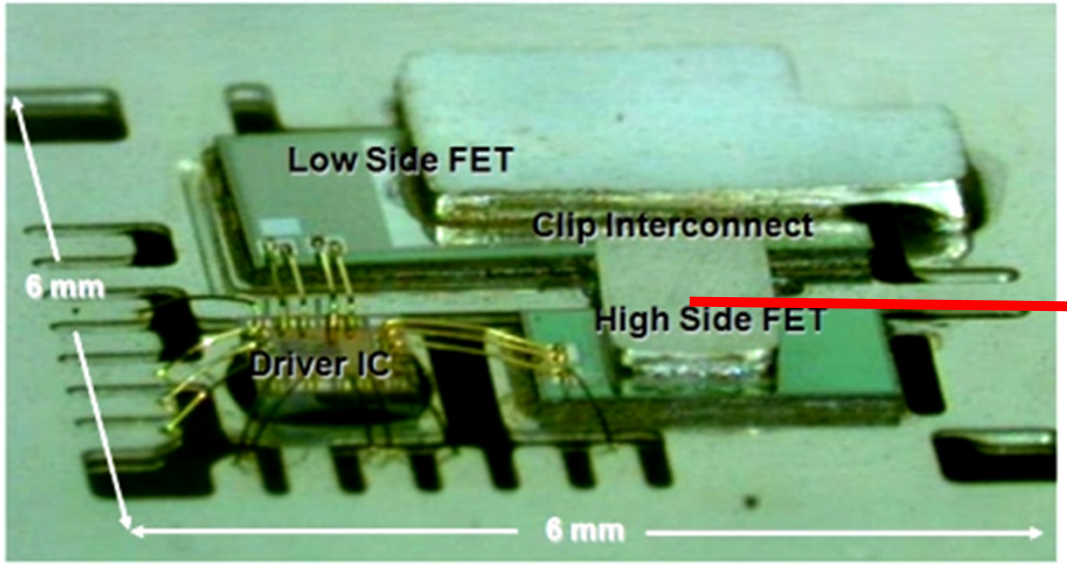
MP87000 90A DrMOS



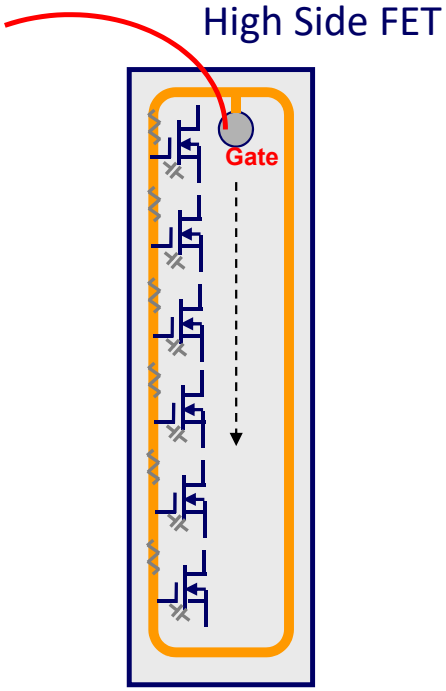
	P_loss (W)	Tcase (C)
MP86998	6.498	105
MP87000	5.6	94

MPS DrMOS Highlights

Competitors Multi-Chip-Module(MCM) DrMOS



From Driver

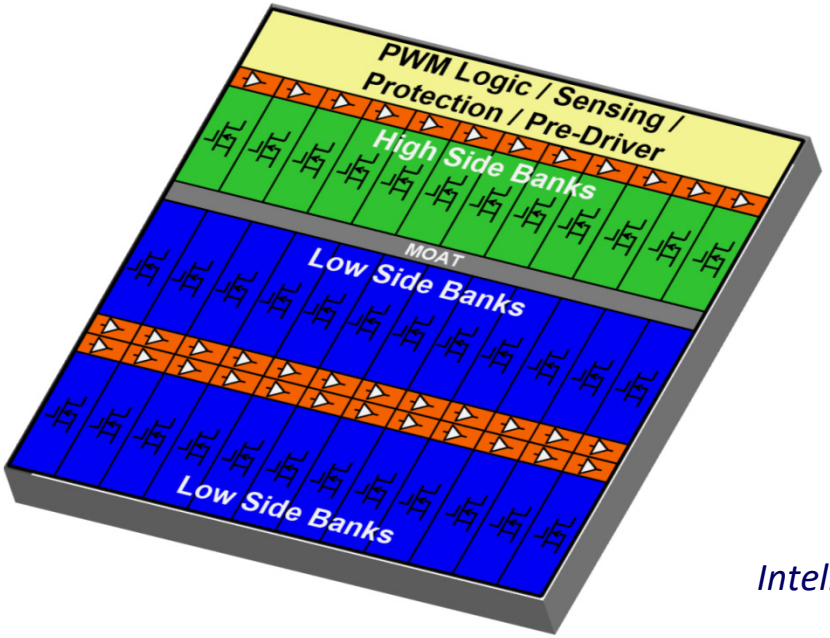


- Reduced power stage parasitic L compare to discrete solution.
- Separate Driver IC can not provide simultaneous on/off across the entire FET due to the gate delay.
- Need large dead time to ensure no shoot-through.

Photo Courtesy http://www.automotive-eetimes.com

"Next-generation power electronics - the quest for increased energy efficiency", November 04, 2010 | Marnix Tack, Peter J Zdebel, | 222901185

MPS Proprietary Monolithic DrMOS

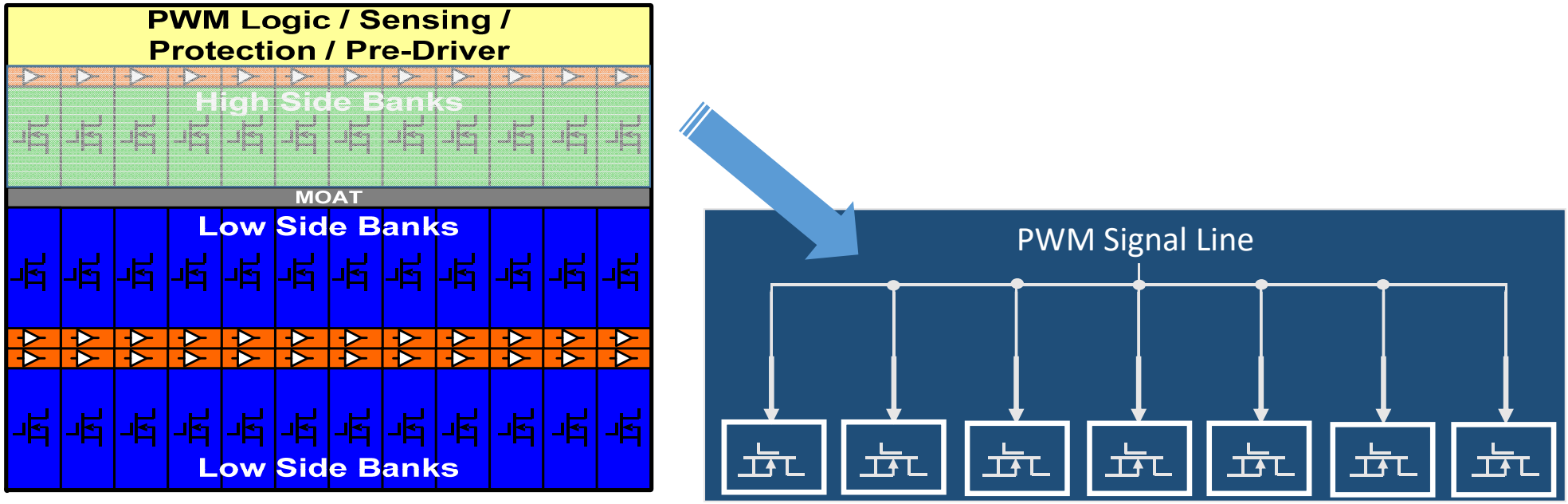


Intelli-Phase™

A Monolithic DrMOS integrates drivers, FETs, PWM Logic, Sensing and Protection circuits into one piece of silicon and operates seamlessly.

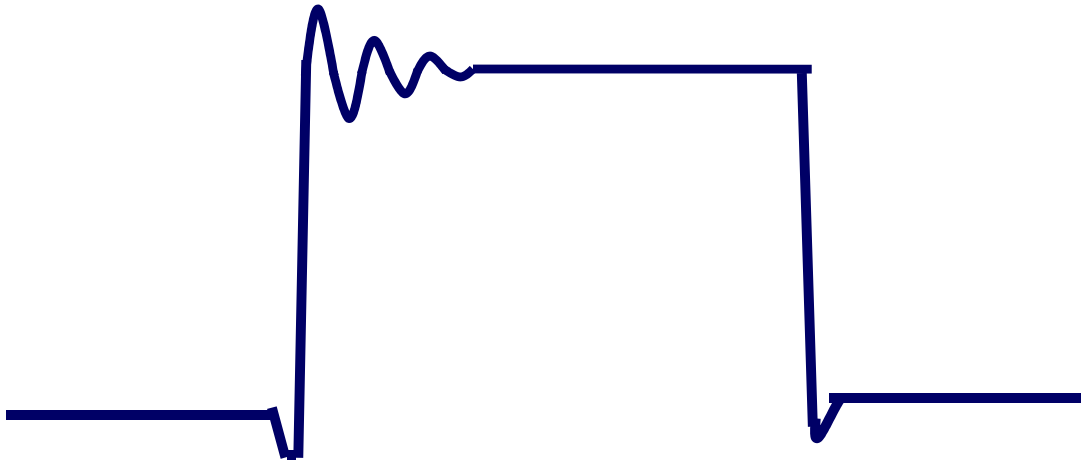
Minimized Gate Drive Delay of Intelli-Phase™

Intelli-Phase®



Distributed Gate Driver (*DGD*) minimizes the Gate Delay, therefore ensures even current distribution among cells

Benefits of Minimized Dead Time



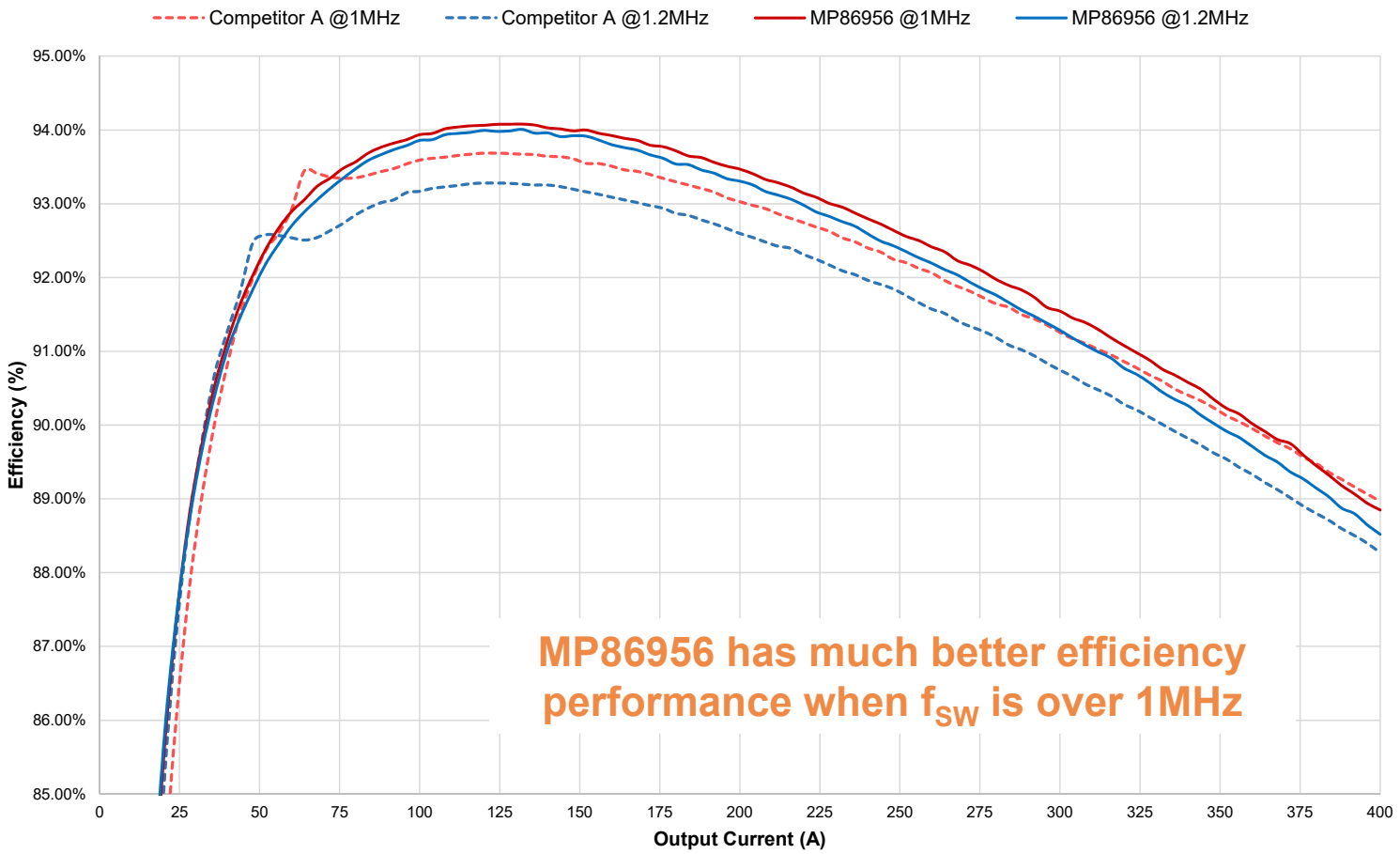
Body Diode Reverse Recovery Loss



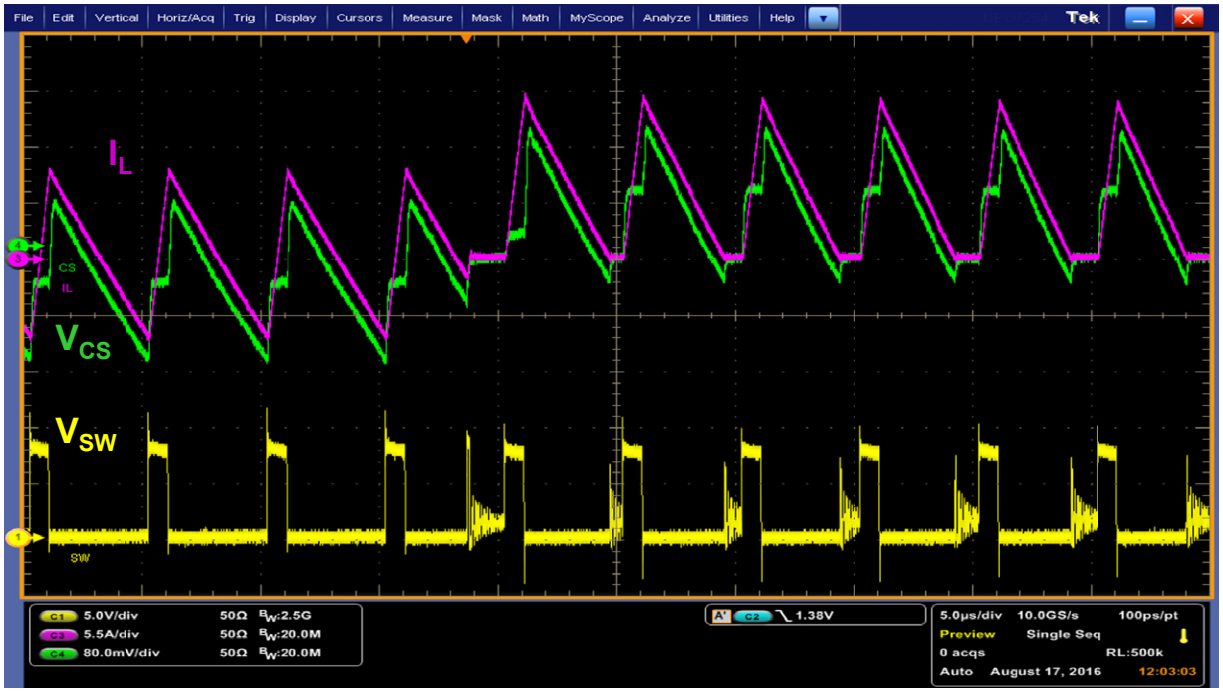
0W

Efficiency: MPS vs. Competitor

V_{IN}=12V, V_{OUT}=1.83V, R_{LL}=0.6mΩ, L=70nH, 7-phase and APS Disable (including driving loss)



MPS Patent Technology to Accurately Sense MHz Cycle-by Cycle Current



CS output matches inductor current very well

Challenges for making monolithic DrMOS

1. MOSFET FOM (Ron*A, Ron*Q)
2. How to make sure DMOS is robust
3. How to make current evenly distributed
4. How to minimize parasitic R & L

MPS BCD Process

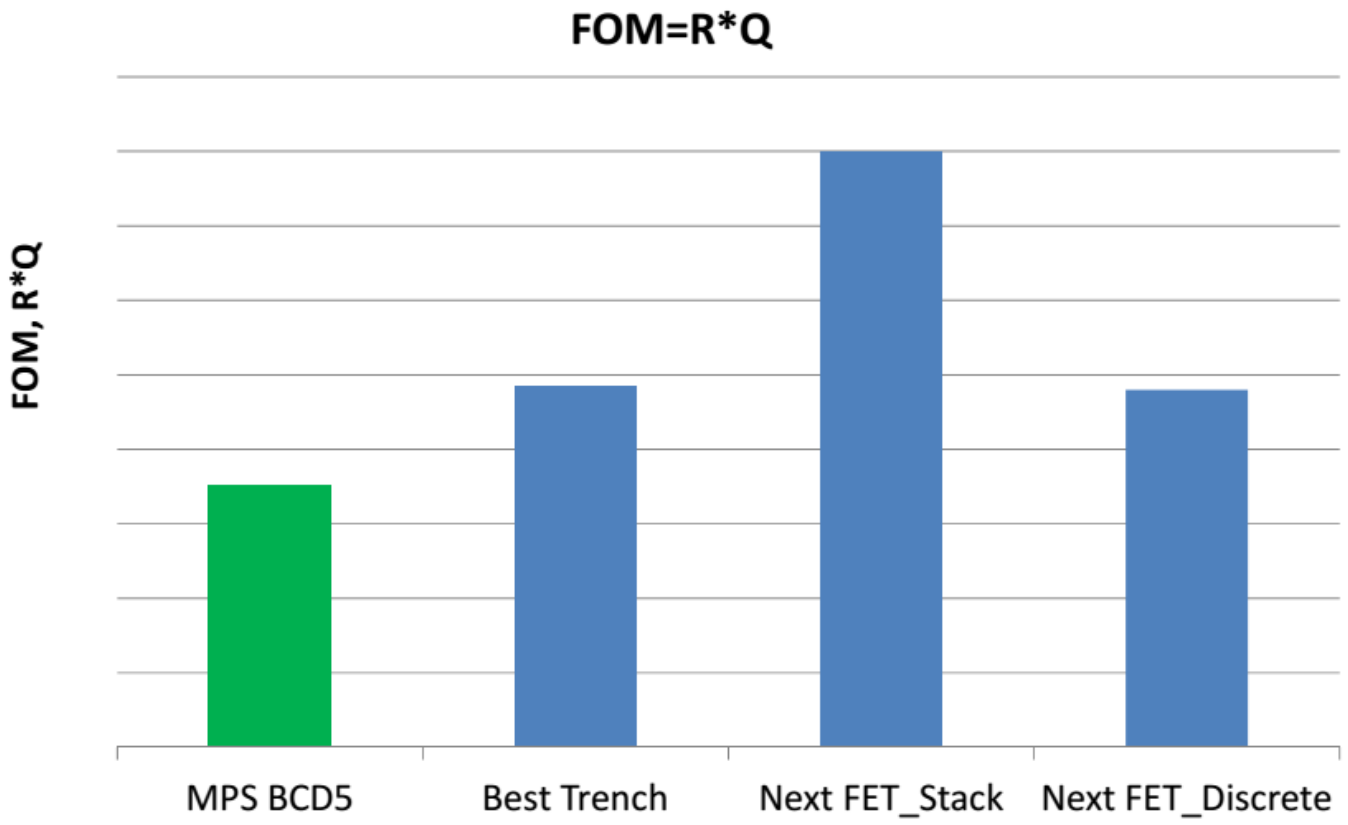
- DMOS R*A aggressively shrunk in every generation

	BCD+	BCD3	BCD4	BCD5
BCD+	1.00			
BCD3 (2011)	0.45	1.00		
BCD4 (2012)	0.35	0.75	1.00	
BCD5 (2014)	0.20	0.40	0.55	1.00

- R*A is not our only consideration:
  - Maximize avalanche current (robustness/reliability)
  - Minimize switching power loss
  - Minimize die cost
  - Zero-cost OTP memory

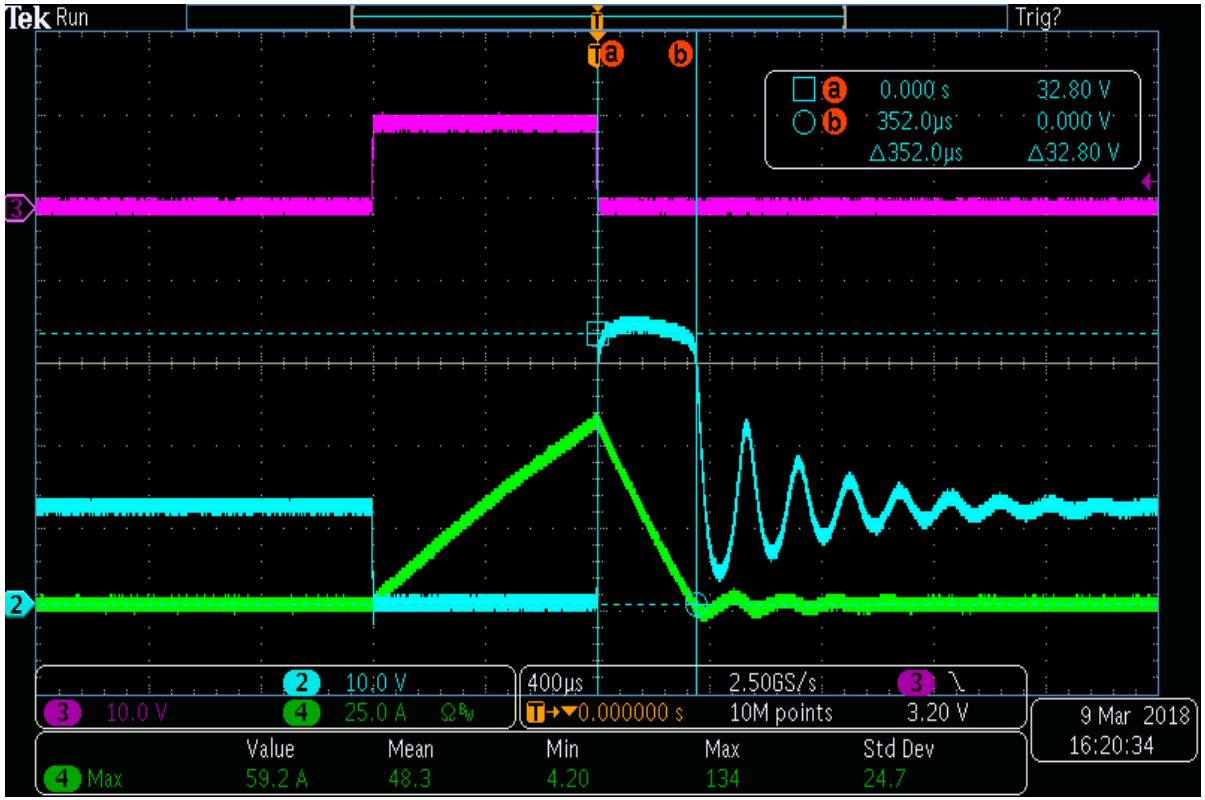
DMOS FOM

RON*Q



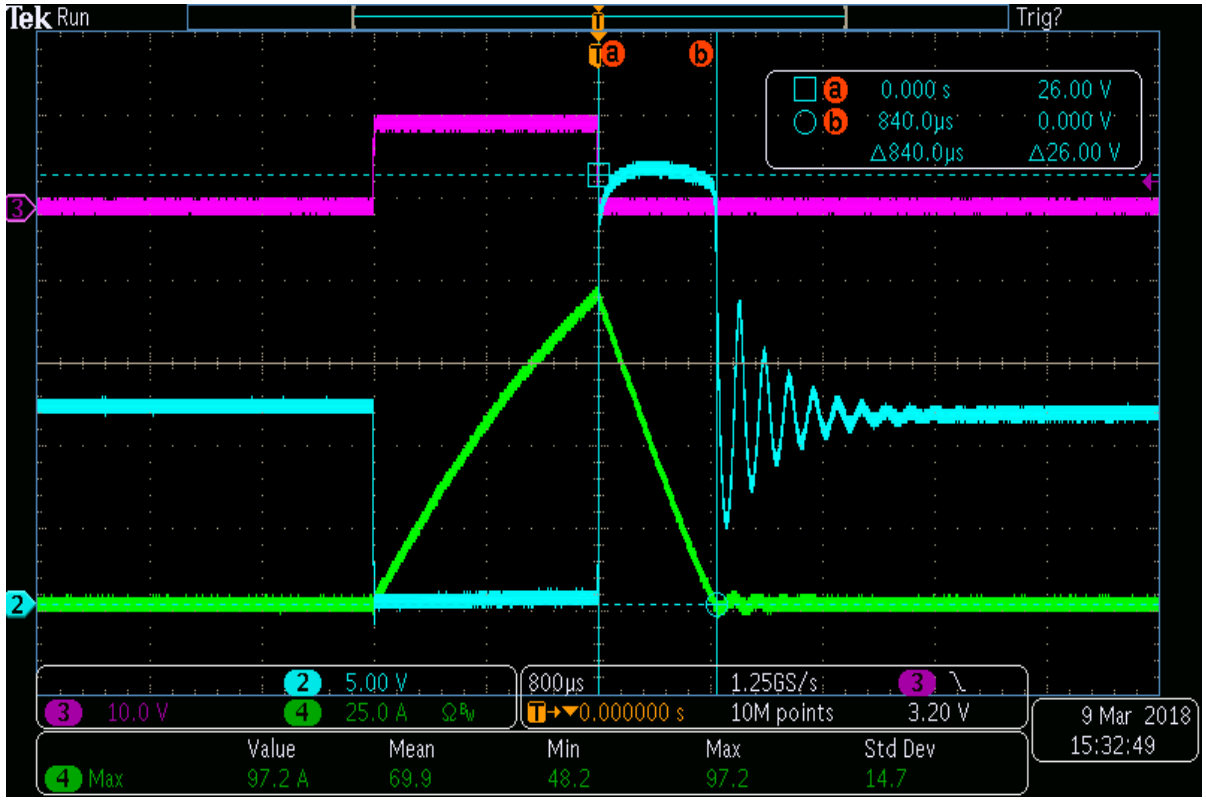
UIS Test Result---MP86956 HS

L	120	uH
Iav	59.2	A
BV	32.8	V
Tav	352	us
LS Eav=	**0.34175**	J



UIS Test Result---MP86956 LS

L	120	uH
Iav	97.2	A
BV	26	V
Tav	840	us
LS Eav=	1.061424	J



UIS Test Result---MP86956

UIS: MPS vs. Competitors

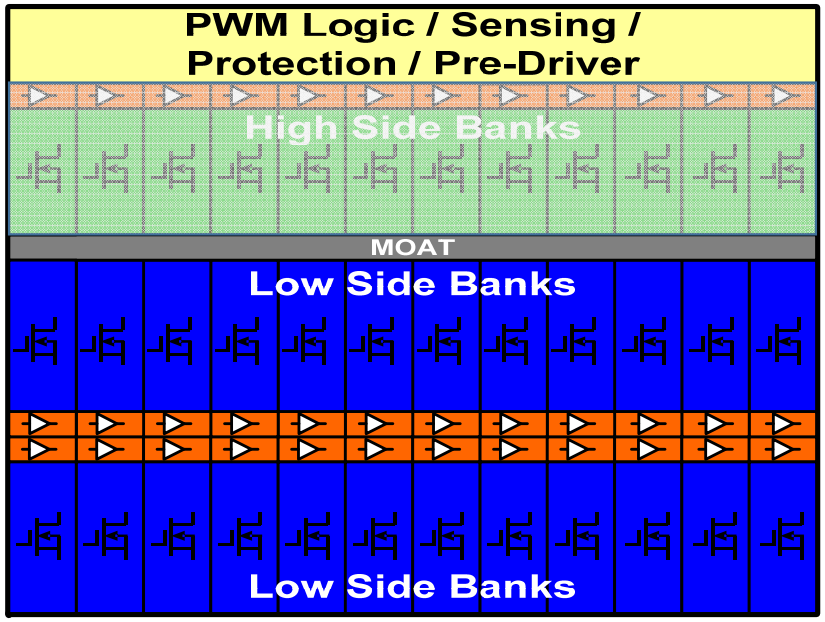
Single Pulse UIS, L=120uH, tested at room temp

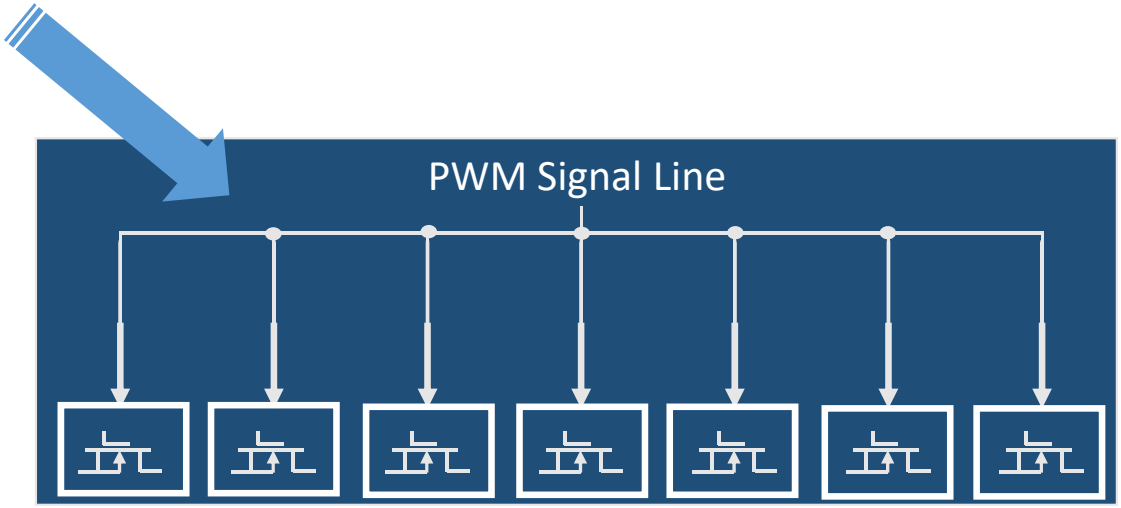
Vendor	HS (mJ)	LS (mJ)
MPS MP86956	320.83	1117.75
Competitor-1	109.98	495.89
Competitor-2	88.42	538.01

MP86956 has much bigger avalanche capabilities

How to make current evenly distributed

Intelli-Phase®

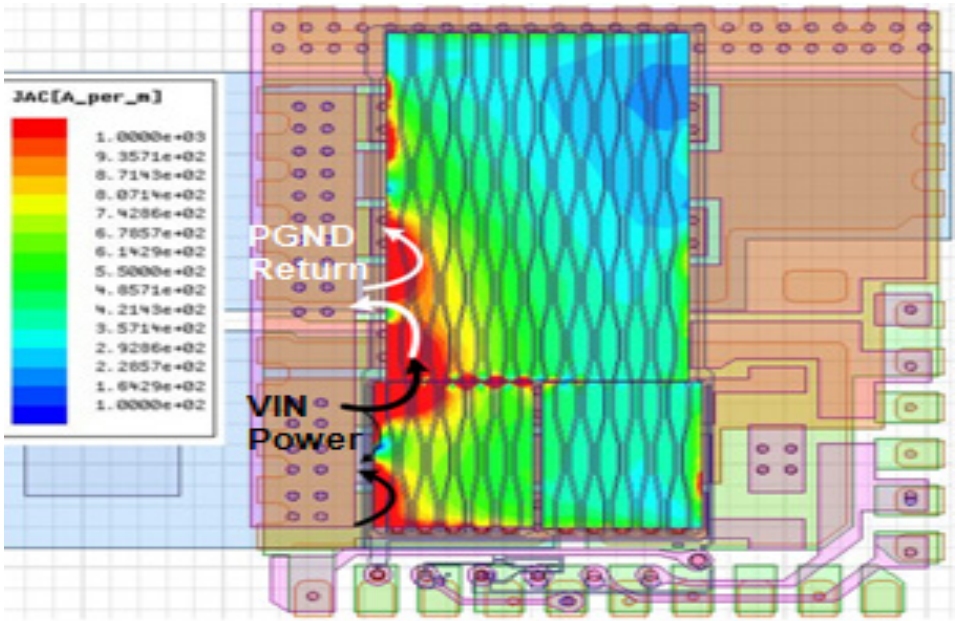


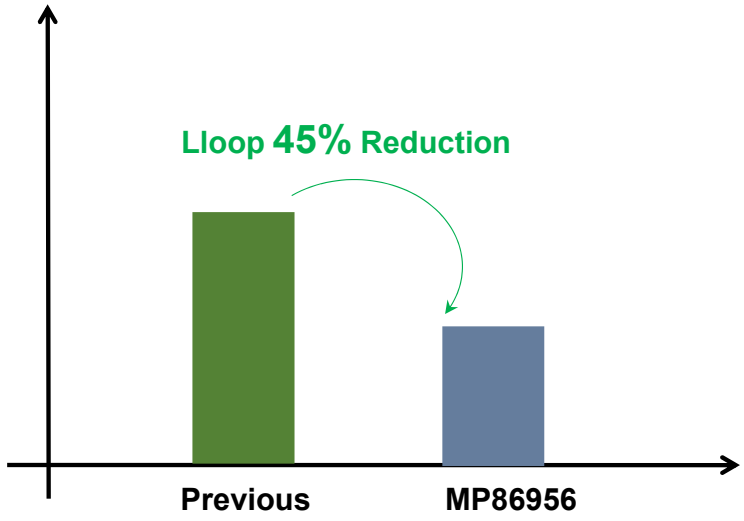


Distributed Gate Driver (*DGD*) minimizes the Gate Delay, therefore ensures even current distribution among cells

How to reduce parasitic R & L

- Patent Metal interconnection to minimize parasitic loop inductance
- Patent PKG re-distribution to minimize parasitic loop inductance
- Internal Cin caps further reduce the parasitic inductance





Thank u very much

mpssupport@monolithicpower.com