Mythbusting EMC Techniques in Power Converter Design

November 2021

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Introduction

In many seminars, we are presented with a suite of techniques to improve the electromagnetic compatibility (EMC) of our designs.

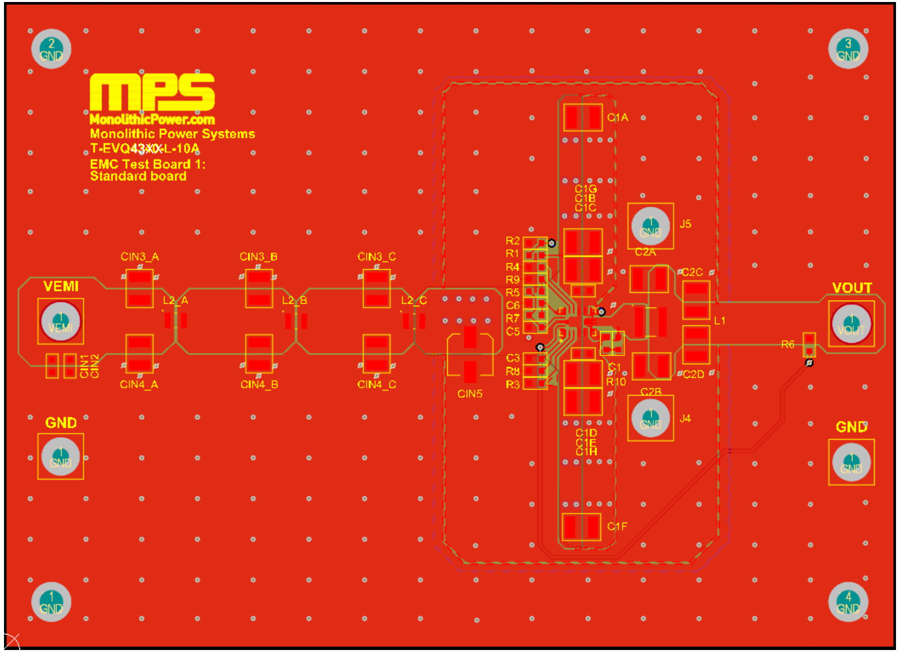
However, these techniques often don't come with accurate A-to-B comparisons to evaluate if they are true, or quantify the impact of a particular implementation.

EMC is a very design-specific topic. There are general physics laws that always apply, but things that are good for a particular design may not be optimal for a different one.

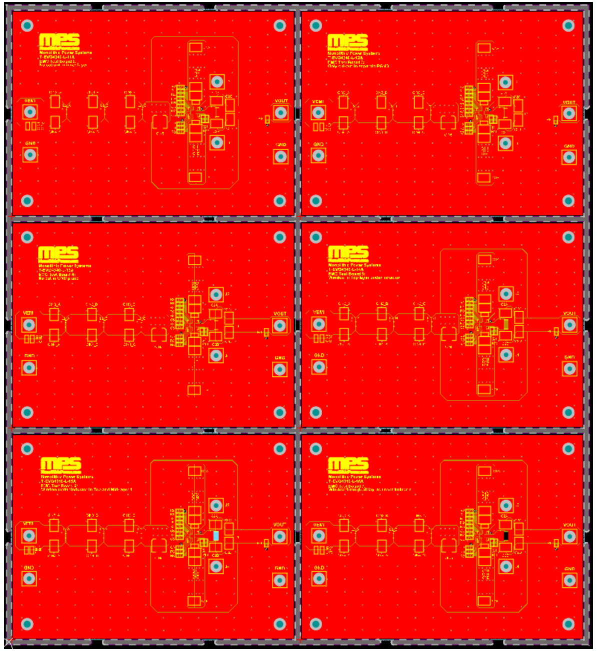
This presentation shows our efforts at trying to "mythbust" some of the most common EMC tips given in seminars.

Methodology

In order to accurately study the effect of each individual design technique, we have designed a set of PCBs that share a similar layout but each feature a specific change.

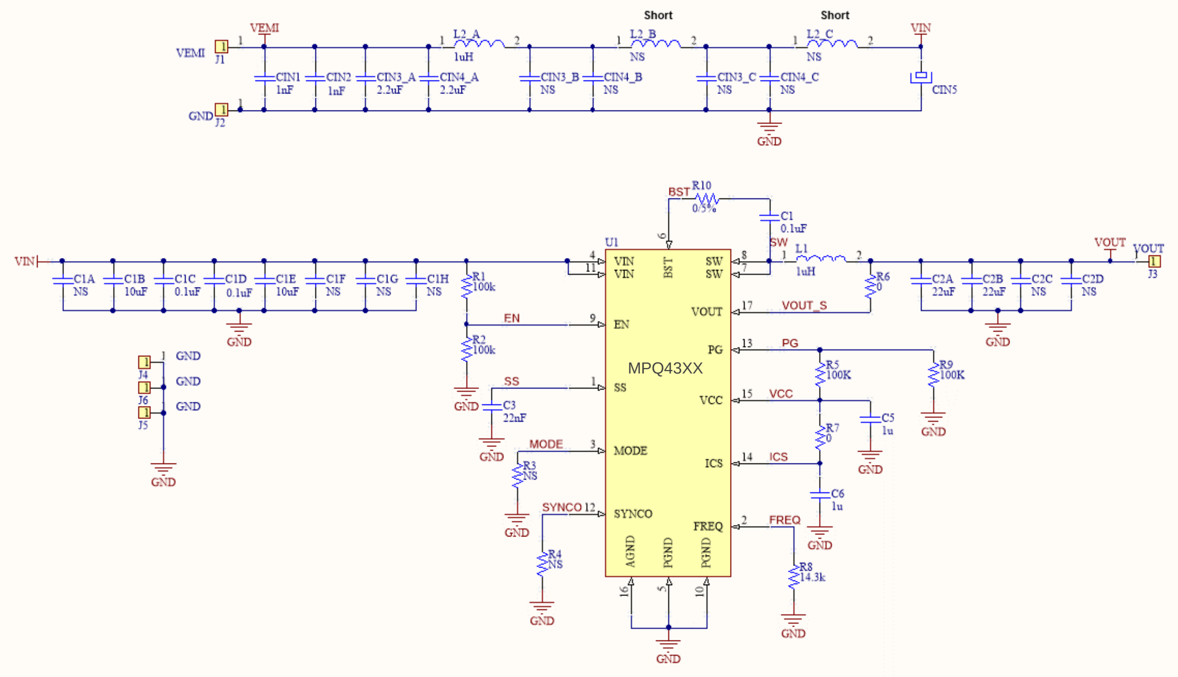


Standard Reference PCB



Methodology

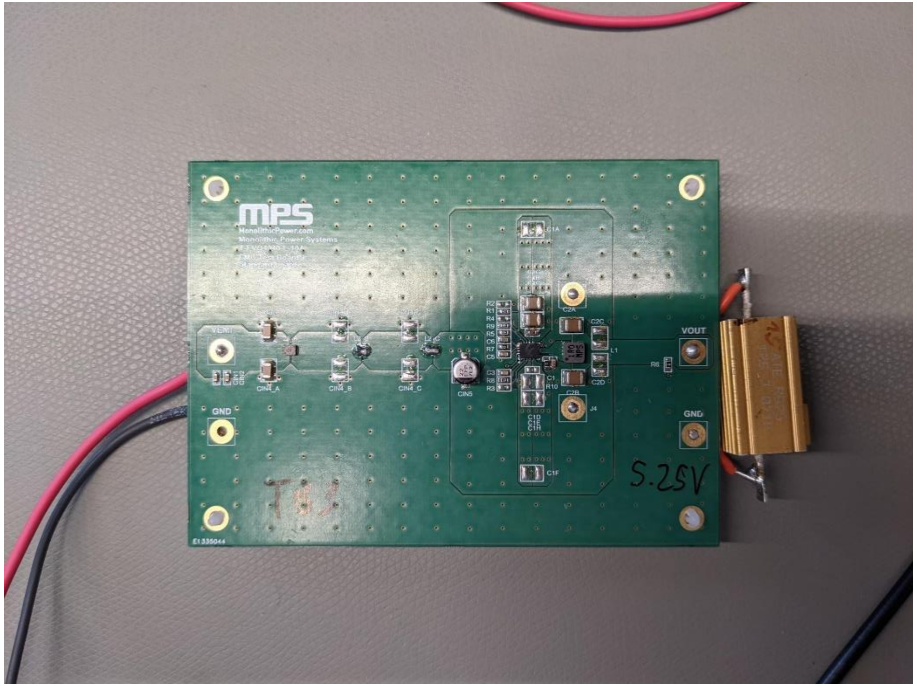
All PCBs share the same schematics, but in some cases the components were populated in different footprints.



Standard Reference Schematics

Methodology

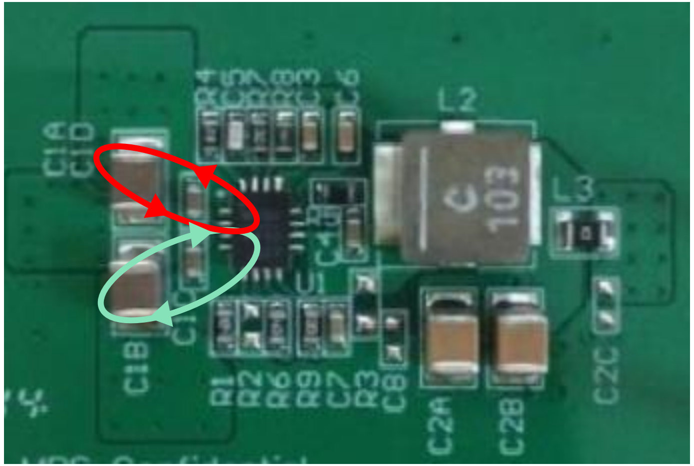
The input harness follows CISPR25 standards. The output resistor is connected to the PCB with short cables.

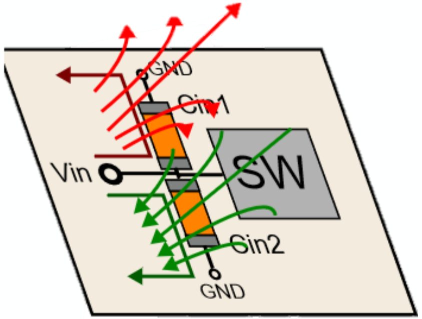


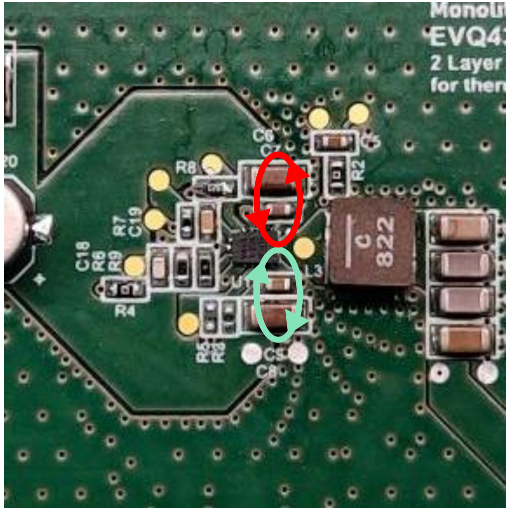
Test Set-Up

Symmetric Input Capacitors: What Is the Myth about?

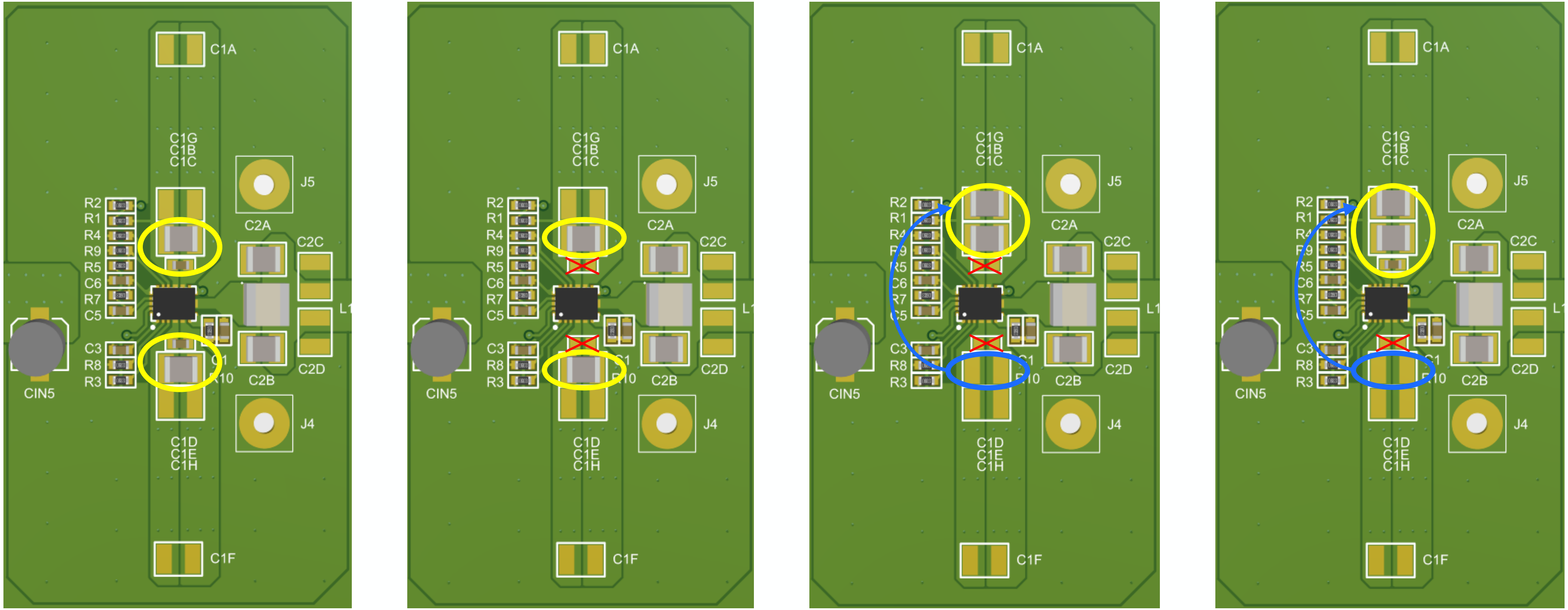
When placing the input capacitors symmetrically, creating two opposing current loops, the magnetic fields created by the dI/dt cancel each other out, as they have opposite directions.







Symmetric Input Capacitors: How Was It Tested?



Symmetric C_{IN}	Symmetric C_{IN} without HF Capacitor	Asymmetric C_{IN} without HF Capacitor	Asymmetric C_{IN} with HF Capacitor
TB6	TB6'	TB3'	TB3

MPS

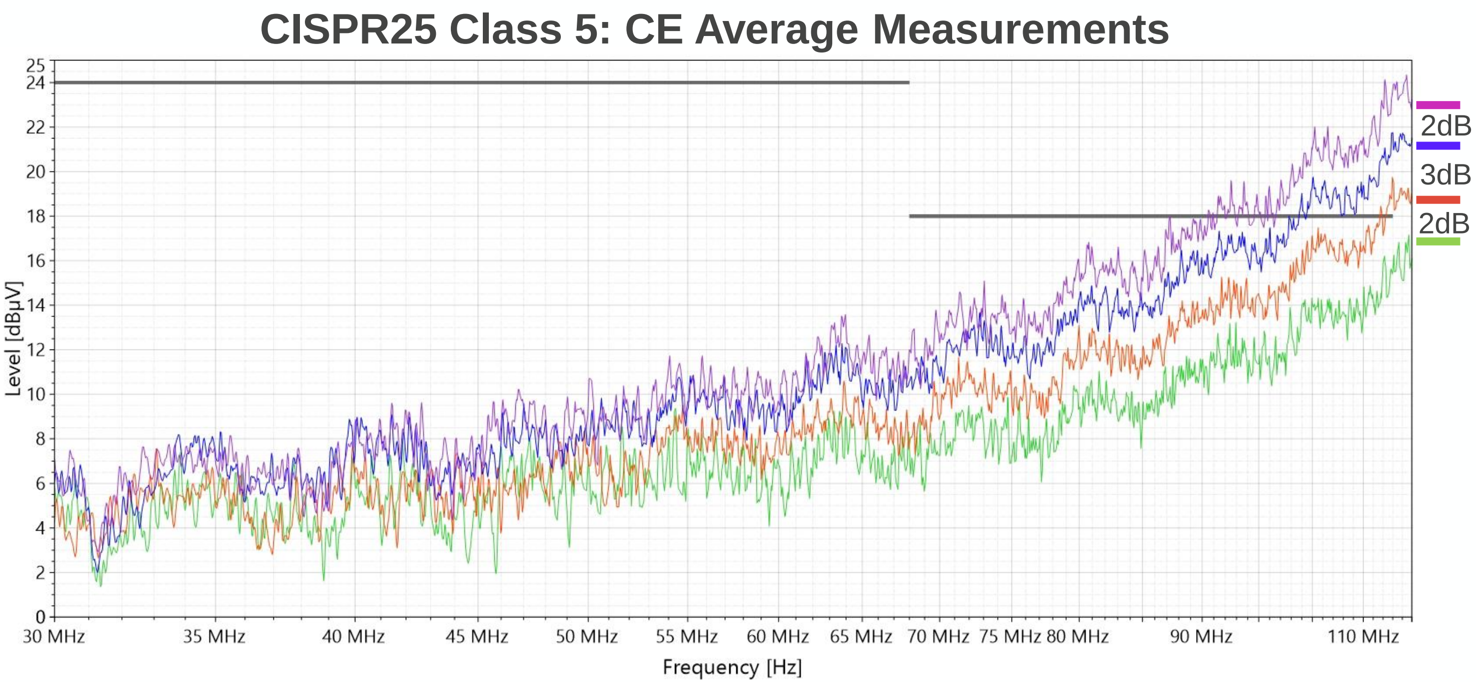
Symmetric Input Capacitors: Test Results

TB6: Symmetric C_{IN} with 100nF

TB6': Symmetric C_{IN} removing 100nF

TB3': Asymmetric C_{IN} removing 100nF

TB3: Asymmetric C_{IN} with 100nF



In the FM band, symmetric C_{IN} and having a 100nF capacitor are always better.

No difference at low frequencies

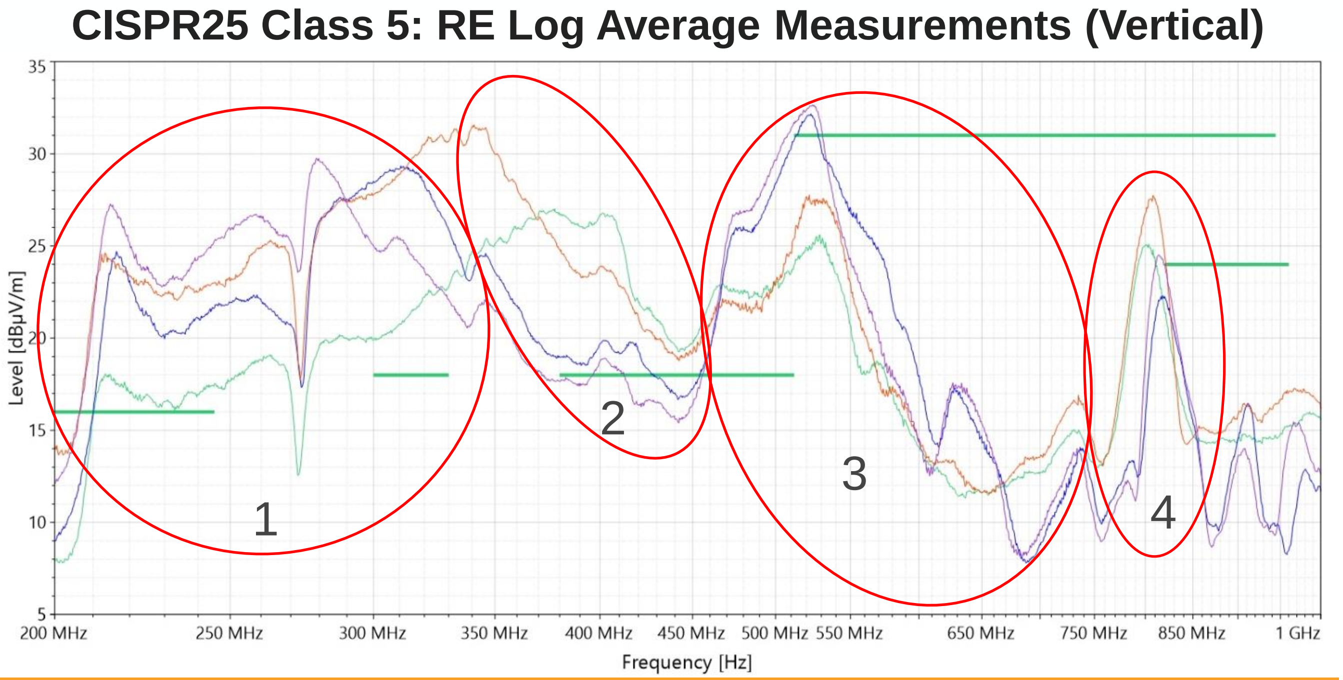
Symmetric Input Capacitors: Test Results

TB6: Symmetric C_{IN} with 100nF

TB6': Symmetric C_{IN} removing 100nF

TB3': Asymmetric C_{IN} removing 100nF

TB3: Asymmetric C_{IN} with 100nF

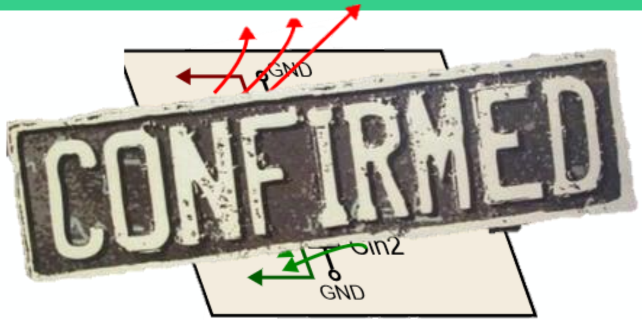


In 1 and 3, the symmetric C_{IN} is ~8dB better.
In 2, the symmetric C_{IN} is ~8dB worse. In 4, it is ~3dB worse.

The 100nF capacitor is always better.

Symmetric Input Capacitors: Mythbusting

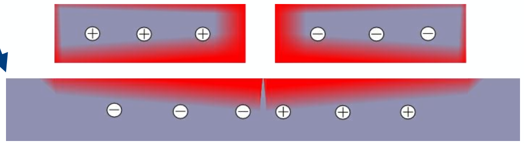
- The symmetrical input capacitors help improve EMI in the critical FM band for conducted emissions testing.
- In radiated emissions testing, they improve emissions in most bands, while in others they degrade the performance. This is probably due to the decrease of the parasitic L, which moves the resonance at higher frequencies.
- The 100nF capacitors are helpful at almost all frequencies.
- The more problematic bands for the symmetrical capacitors can be improved by other methods, such as using a ferrite bead or following topics.

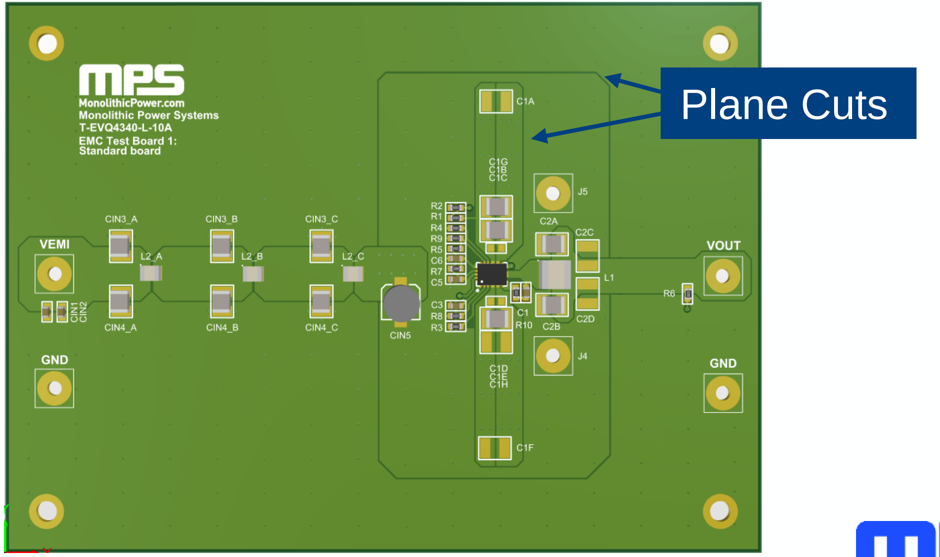


Ground Plane Splitting: What Is the Myth about?

Return currents in the GND plane are mostly concentrated next to their source conductor, but some of them are spread across a wider surface of the plane. These larger current loops form a magnetic antenna and will radiate. By cutting the GND portion of the hot loop from the rest of the board's GND, these current loops are forced to be smaller, thus lowering emissions.

The current density is low, but not 0

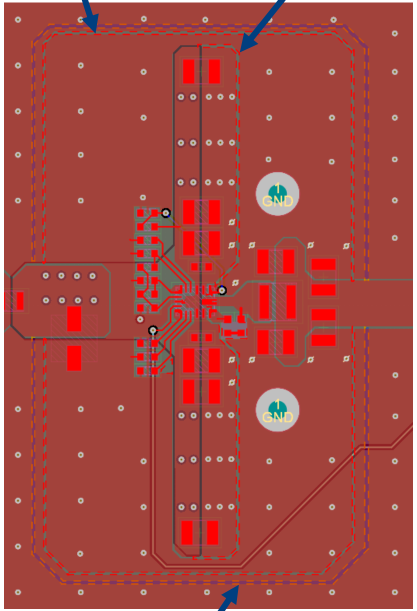




Ground Plane Splitting: How Was It Tested?

Top-Layer GND Cut

PGND Cut

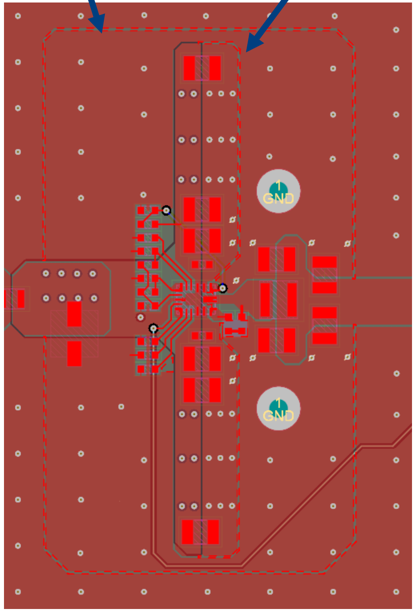


Internal Layer GND Cut

TB6

Top-Layer GND Cut

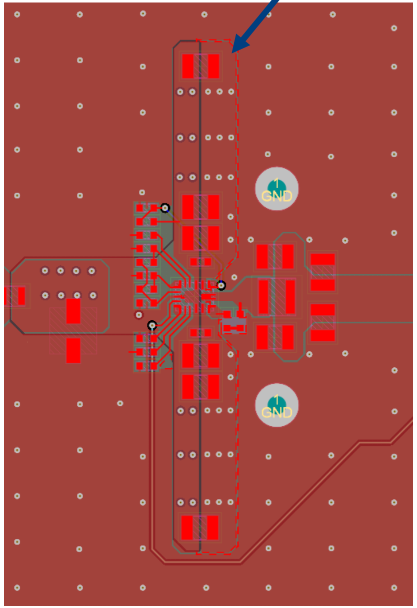
PGND Cut



Solid Internal Layer GND

TB11

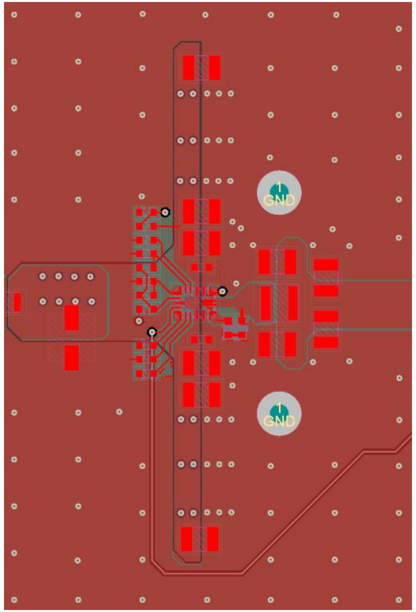
PGND Cut



Solid Internal Layer GND

TB12

No Cut on Top Layer



Solid Internal Layer GND

TB13

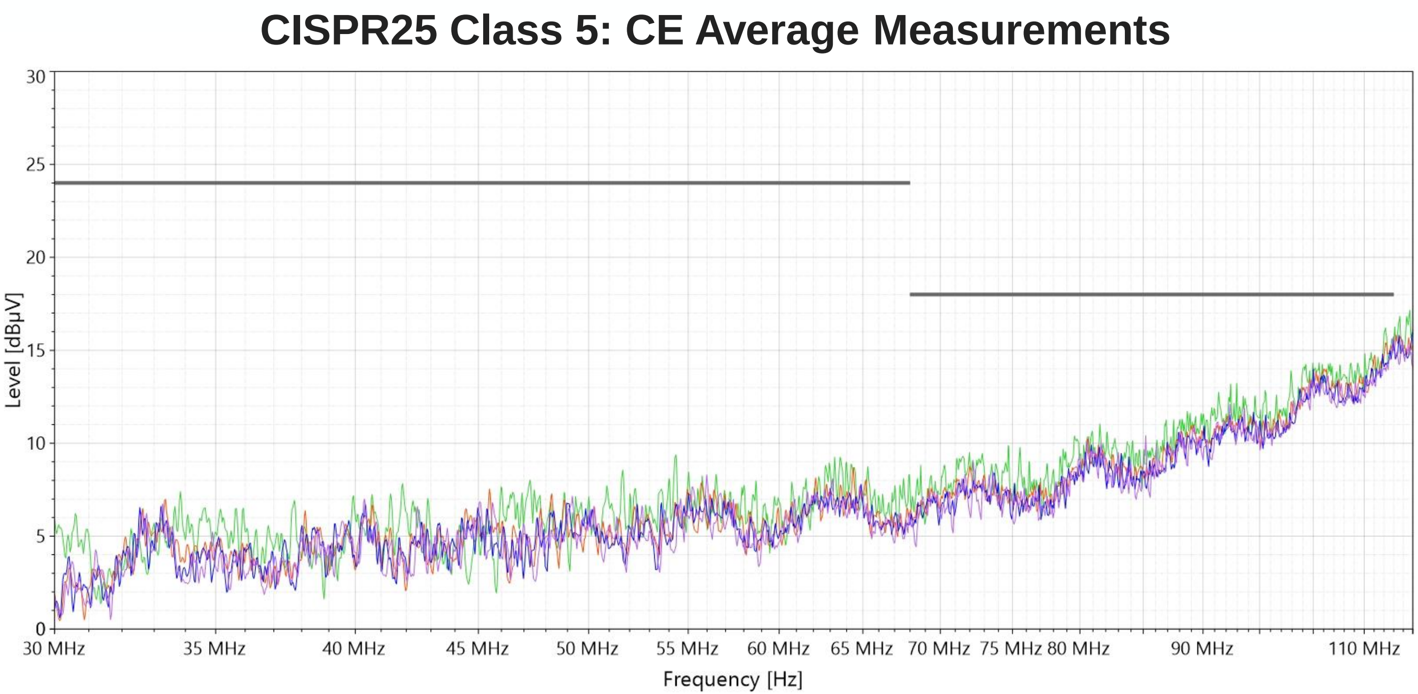
Ground Plane Splitting: Test Results

TB6: All GND cuts

TB11: Removing Internal GND Cut

TB12: Removing Internal and Top GND Cut

TB13: Removing All Cuts



No Difference!

Lower frequency also looks the same, but that was expected.

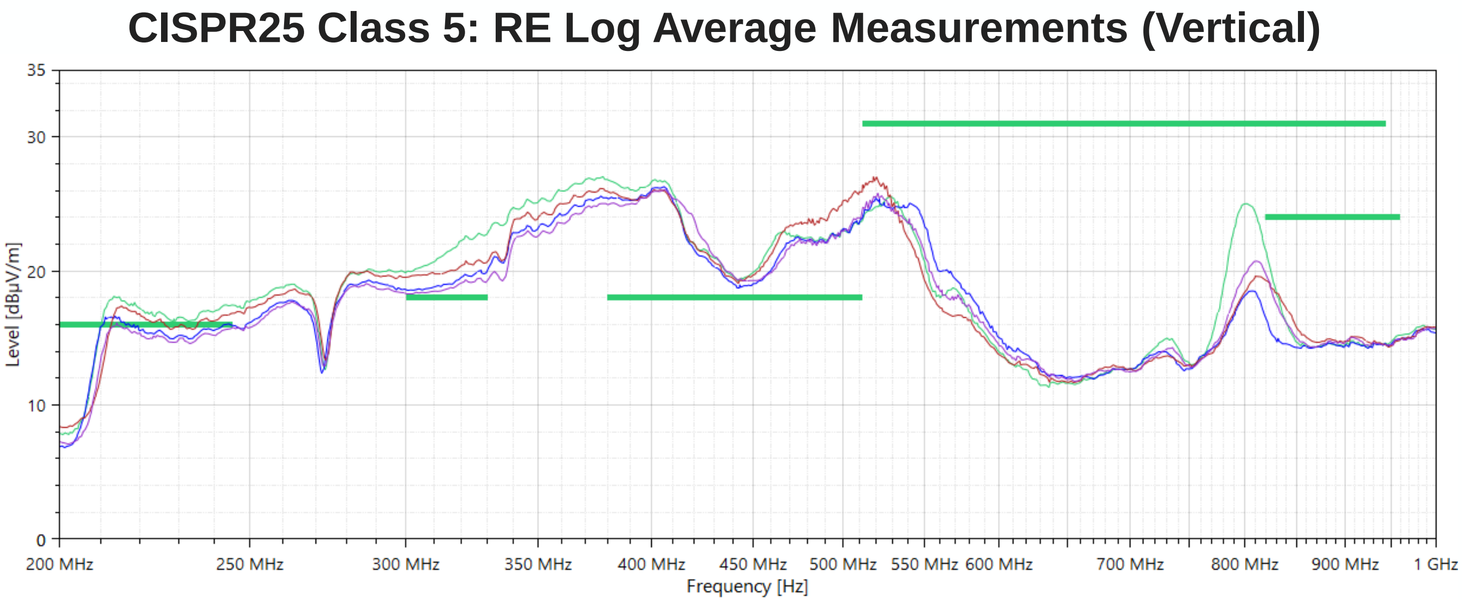
Ground Plane Splitting: Test Results

TB6: All GND cuts

TB11: Removing Internal GND Cut

TB12: Removing Internal and Top GND Cut

TB13: Removing All Cuts



Cutting the GND plane in several locations makes things worse. The best case is when making a local cut to PGND.

The difference between cutting PGND or not is minimal in most bands.

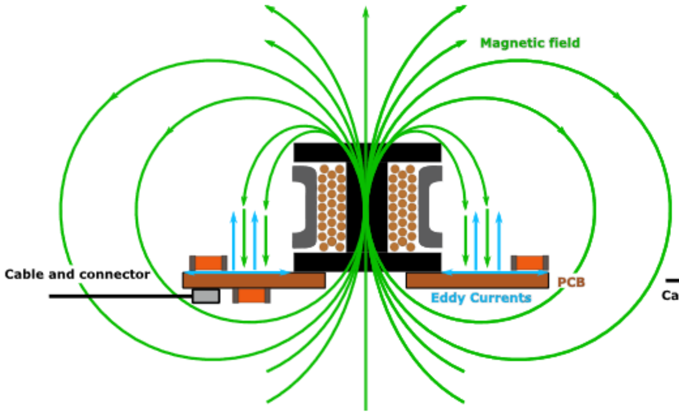
Ground Plane Splitting: Mythbusting

- Splitting the GND plane in the power converter circuit does not have a significant impact on EMI (<1dBµV/m).
- Cutting the GND plane in multiple areas degrades the GND impedance, making the board worse.
- Cutting PGND close to the IC increases the thermal $R_{J\text{-}A}$.

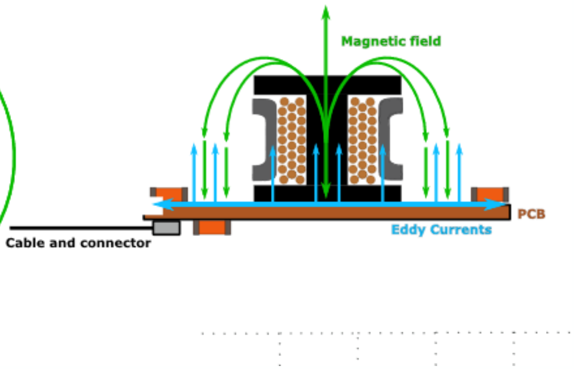
Copper under the Inductor: What Is the Myth about?

The magnetic fields emitted by the inductor create eddy currents when they hit perpendicular to a conductor. These eddy currents create losses in the form of heat, and reduce the effective inductance. However, they also generate magnetic fields that oppose the inductor's magnetic field. By placing copper under the inductor, most of the magnetic field is captured and converted to eddy currents, lowering the total emissions.

PCB with window in Cu under coil

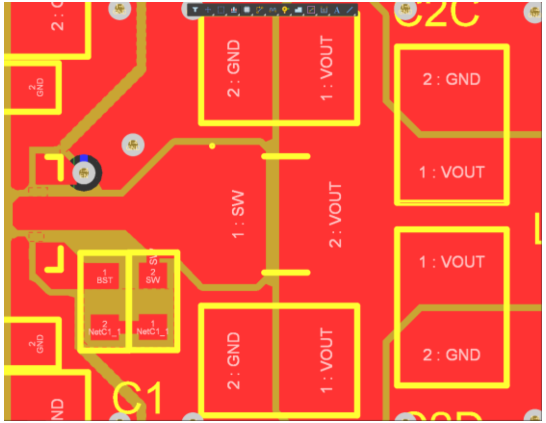


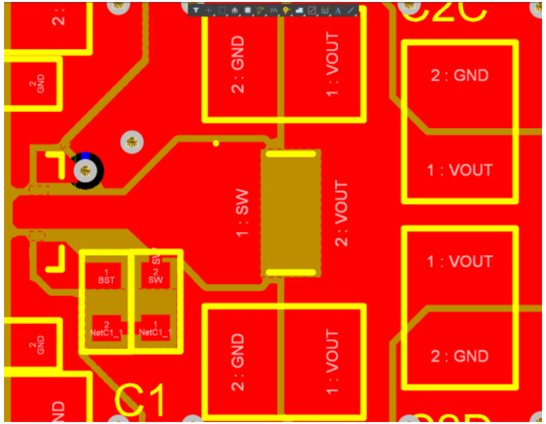
PCB with no window in Cu under coil



Copper under the Inductor: How Was It Tested?

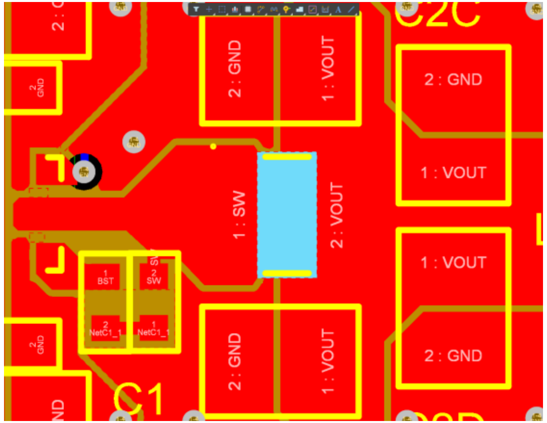
TB6

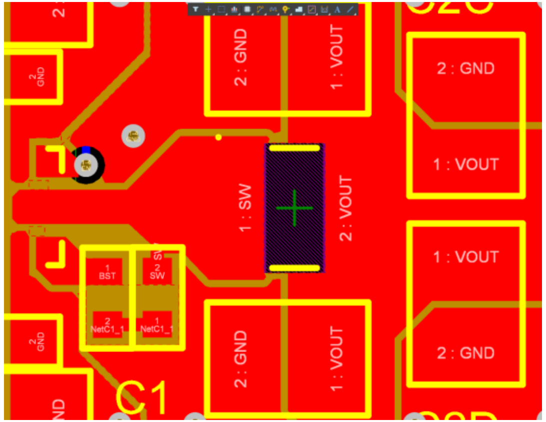




TB8

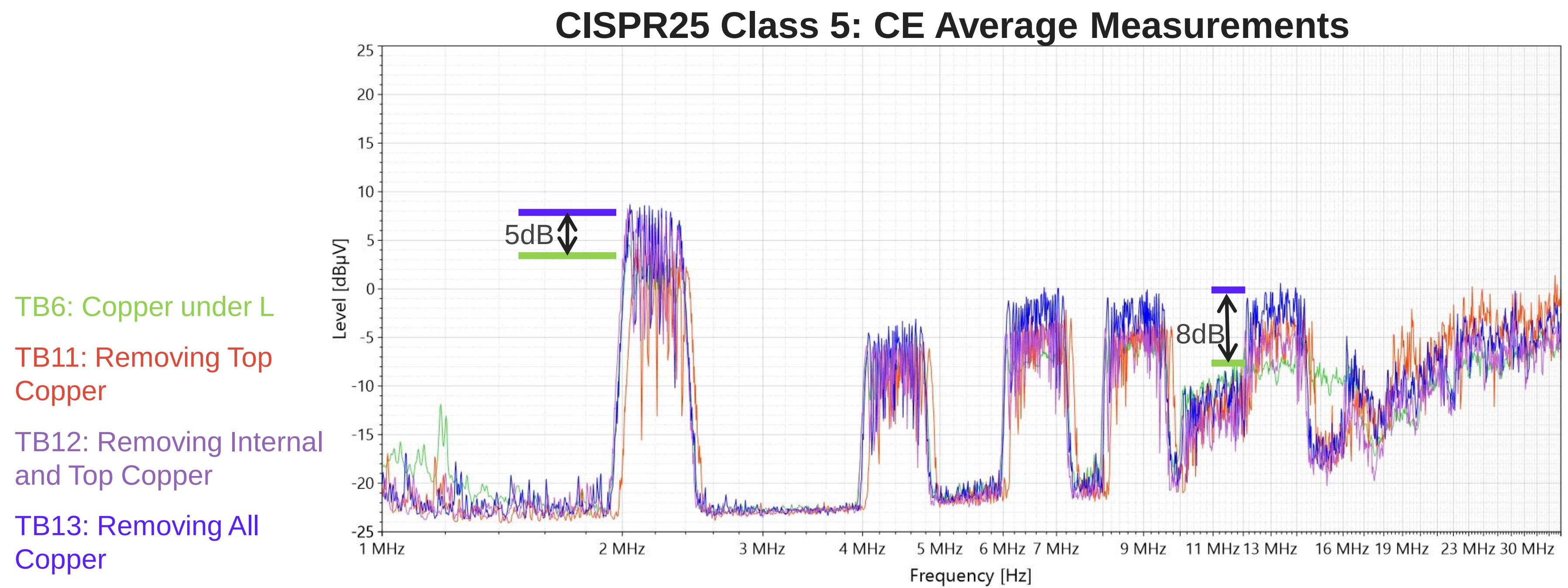
TB9





TB10

Copper under the Inductor: Test Results



The board with top copper under the inductor is better in the fundamental and following harmonics.

Copper under the Inductor: Test Results

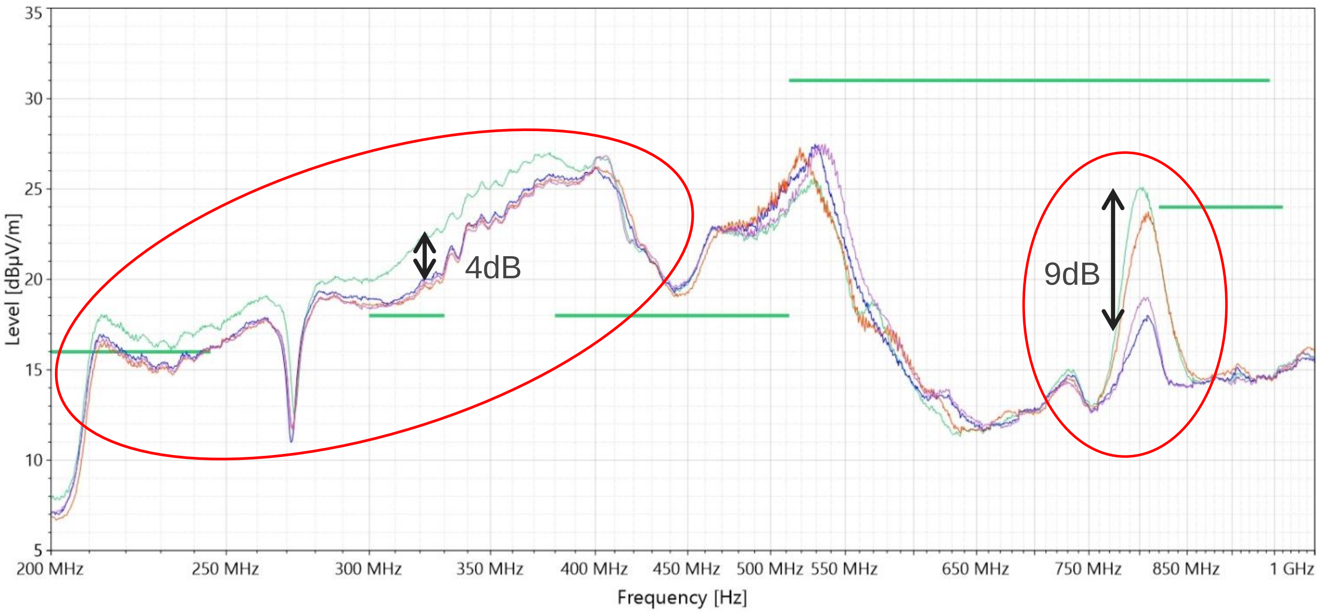
CISPR25 Class 5: RE Log Average Measurements (Vertical)

TB6: Copper under L

TB11: Removing Top Copper

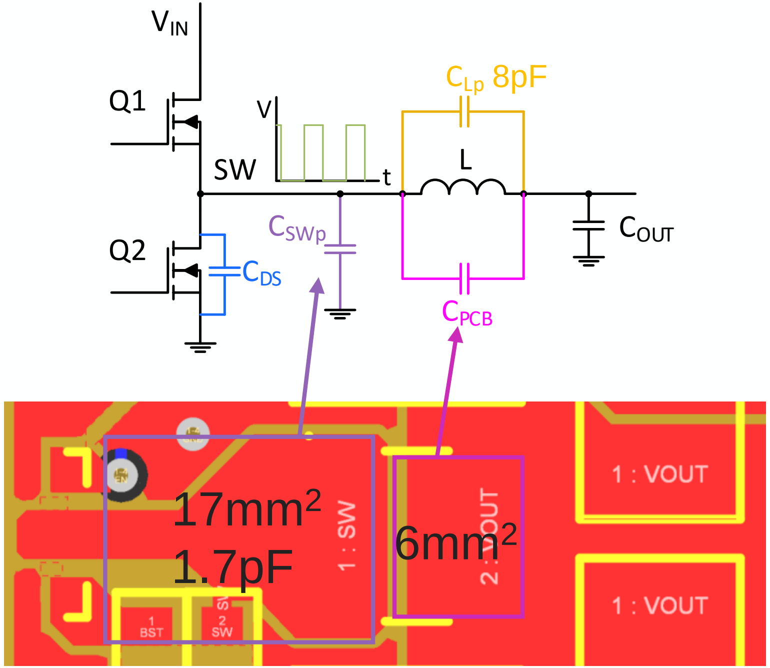
TB12: Removing Internal 1 and Top Copper

TB13: Removing All Copper



The board with top copper under the inductor is worse in most high-frequency bands.

Copper under the Inductor: Analysis

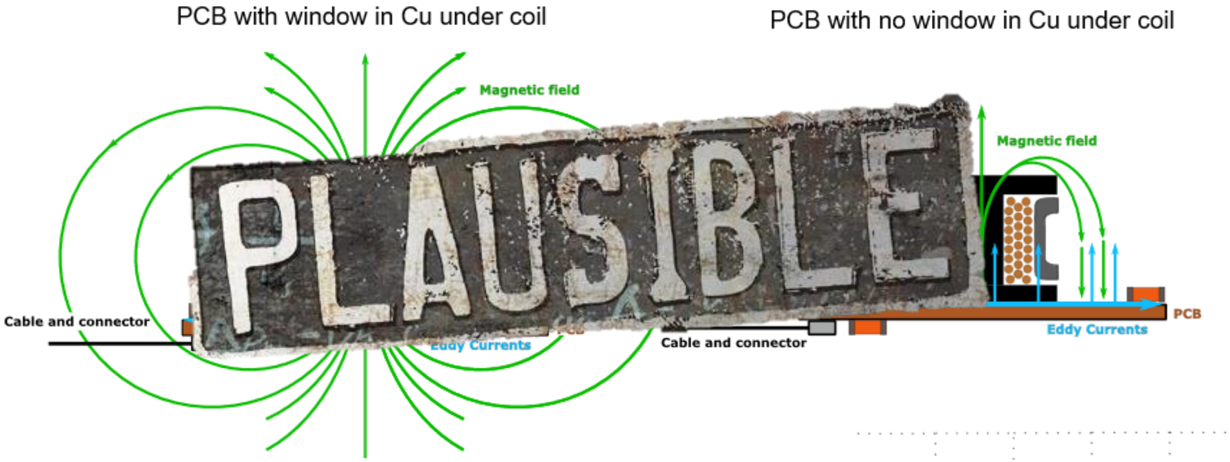


The copper area under the inductor in the top layer is V_{OUT}. The eddy currents are induced there. The parasitic capacitance between SW and V_{OUT} is increased by this additional area.

Copper under the Inductor: Mythbusting

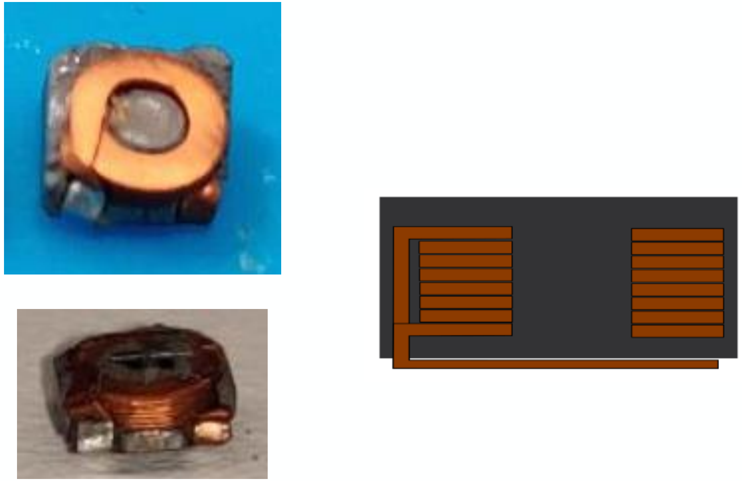
The test results in CE show a reduction in the emitted noise when there is copper directly under the inductor.

The test results in RE show an increase in the emitted noise when copper there is directly under the inductor. This may be caused by the copper being V_{OUT} instead of GND.

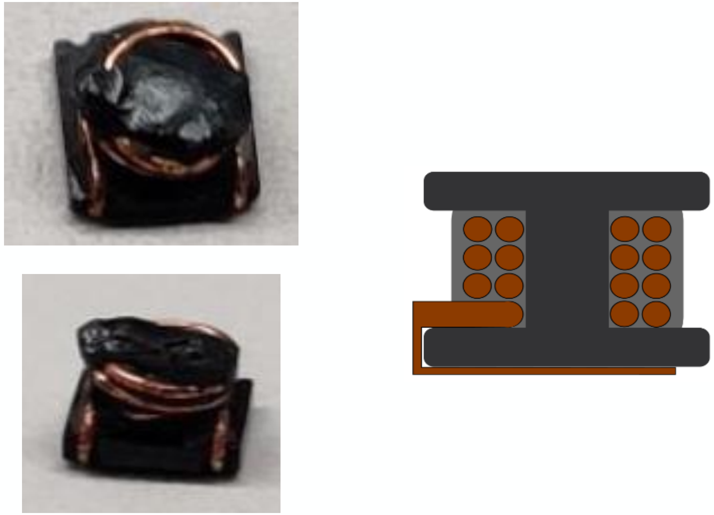


Shielded Inductors: What Is the Myth about?

Shielded inductors are regarded as always having better EMC performance compared to non-shielded and semi-shielded inductors.



Shielded (Molded)



Semi-Shielded (Epoxy Coating)

Shielded Inductors: How Was It Tested?

Changed the standard molded inductor used in all other tests (the MPL-AY4020-1R0) to a semi-shielded inductor (the MPL-SE4030-1R0).

APPLICATIONS

- Battery-powered devices
- Embedded computing
- High-current SMPS
- High-frequency SMPS
- POL converters
- FPGA

FEATURES

- Size 4.1mmx4.1mmx1.9mm
- Low DCR
- Low AC Losses
- Low Audible Noise
- Molded Construction
- Soft Saturation
- Stable Over High Temperatures
- Max Operating Temp +155°C
- RoHS/REACH-Compliant, Halogen-Free

ELECTRICAL CHARACTERISTICS

Parameter			Value	Unit
Inductance [1]	L	±20%	1.0	μH
Resistance	R_{DC}	typ	10.1	mΩ
Resistance $_{MAX}$	$R_{DC\ MAX}$	max	11.8	mΩ
Rated Current [2]	I_R	typ	7.9	A
Saturation Current $_{25°C}$ [3]	$I_{SAT\ 25°C}$	typ	8.6	A
Saturation Current $_{100°C}$ [4]	$I_{SAT\ 100°C}$	typ	8.6	A
Resonance Frequency	f_r	typ	56	MHz

$C_P = 8pF$

APPLICATIONS

- Battery-powered devices
- High-efficiency SMPS
- Embedded computing
- Input filters

FEATURES

- Size 4mmx4mmx3mm
- Semi-Shielded Construction
- Low DCR
- Low Stray Field
- Max Operating Temp +125°C
- RoHS/REACH-Compliant, Halogen-Free

ELECTRICAL CHARACTERISTICS

Parameter			Value	Unit
Inductance [1]	L	±20%	1.0	μH
Resistance	R_{DC}	typ	12.5	mΩ
Resistance $_{MAX}$	$R_{DC\ MAX}$	max	15	mΩ
Rated Current [2]	I_R	typ	6.3	A
Saturation Current $_{25°C}$ [3]	$I_{SAT\ 25°C}$	typ	7.5	A
Saturation Current $_{100°C}$ [4]	$I_{SAT\ 100°C}$	typ	7.2	A
Resonance Frequency	f_r	typ	90	MHz

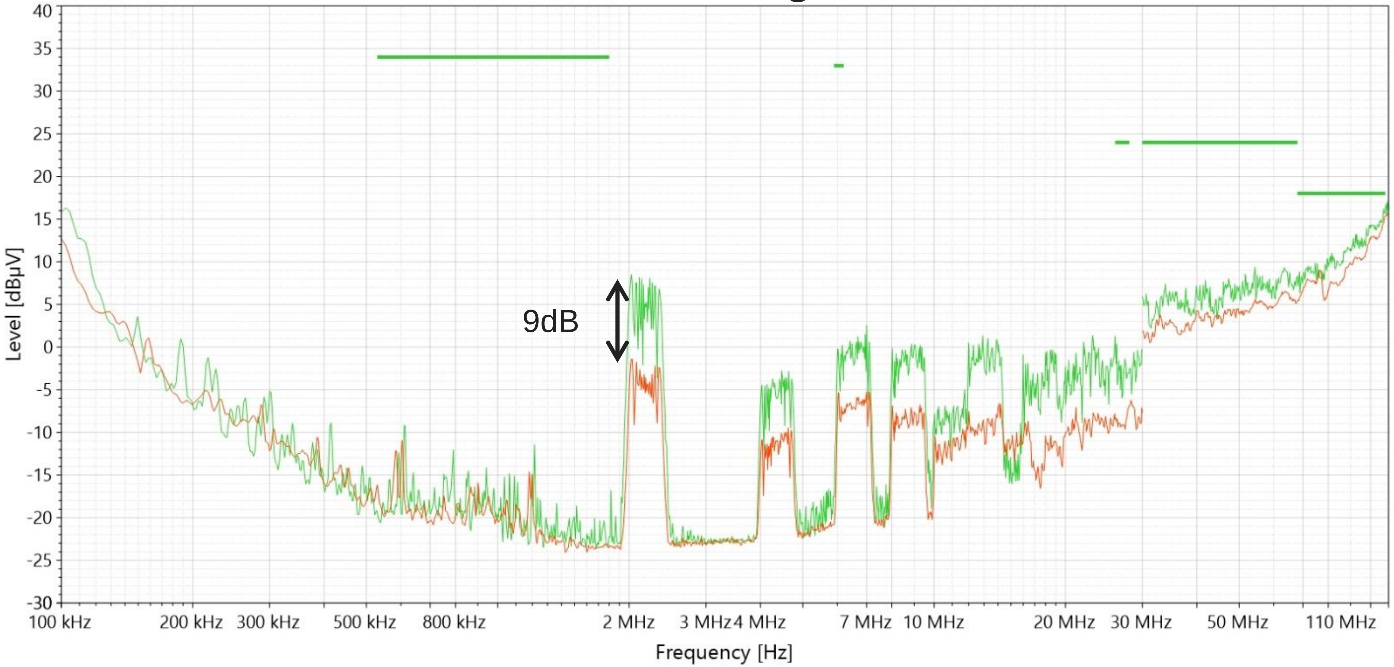
$C_P = 3pF$

Shielded Inductors: Test Results

TB6: Molded Inductor

TB15: Semi-Shielded Inductor

CISPR25 Class 5: CE Average Measurements



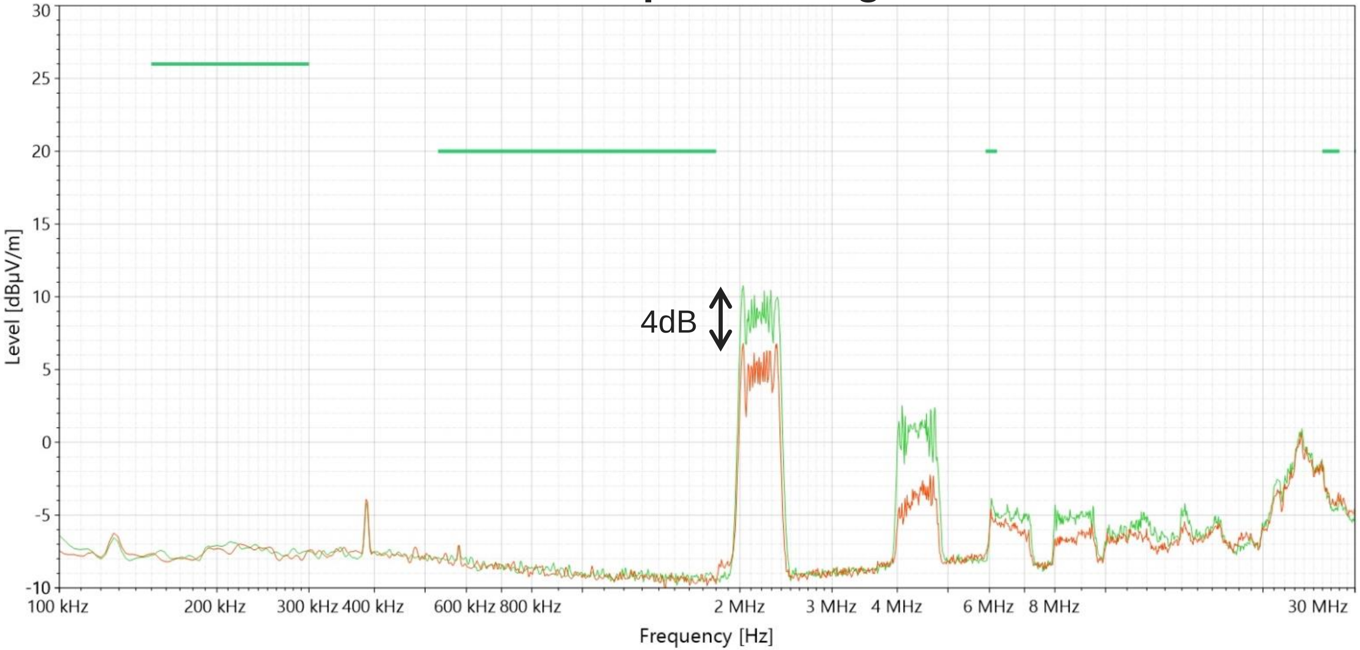
The semi-shielded inductor is much better at low frequencies, and helps at the FM band.

Shielded Inductors: Test Results

TB6: Molded Inductor

TB15: Semi-Shielded Inductor

CISPR25 Class 5: Monopole Average Measurements



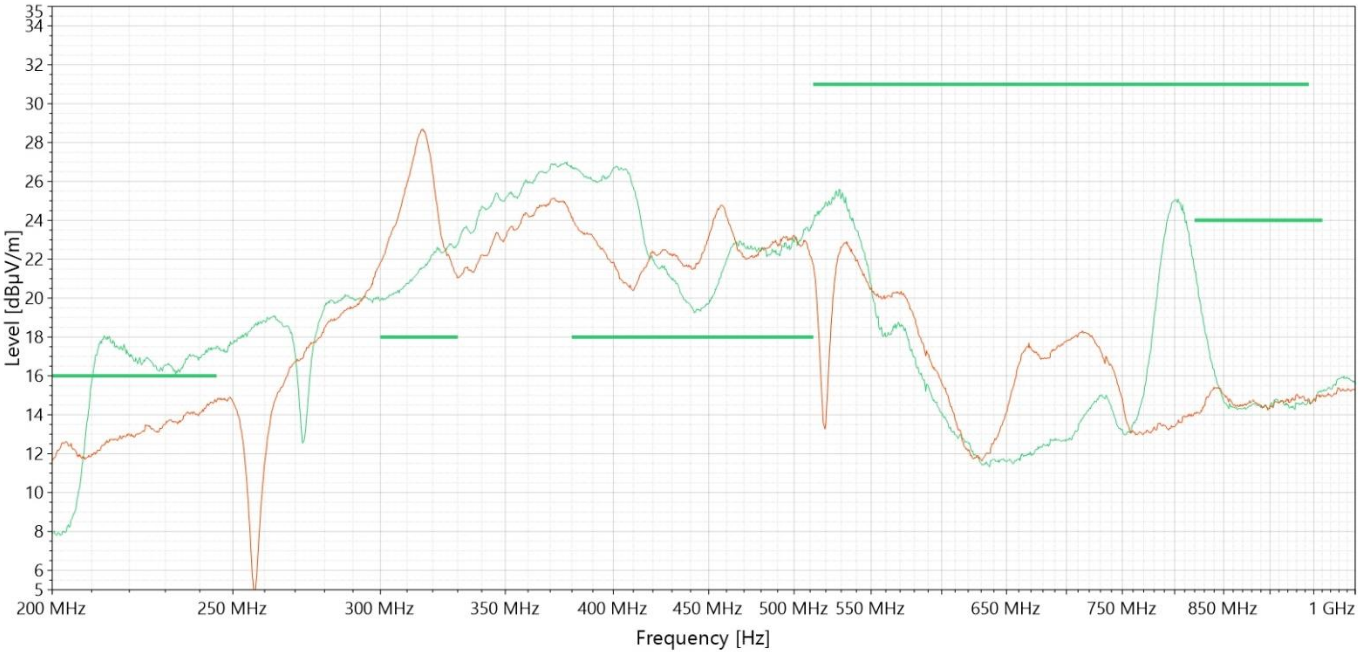
The semi-shielded inductor emits less E-field.

Shielded Inductors: Test Results

TB6: Molded Inductor

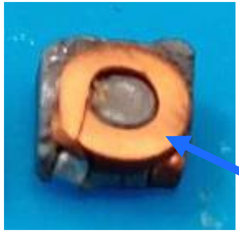
TB15: Semi-Shielded Inductor

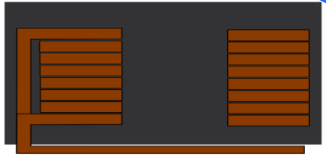
CISPR25 Class 5: RE Log Average Measurements (Vertical)



Overall, the semi-shielded looks better except for the resonance at 320MHz.

Shielded Inductors: Analysis

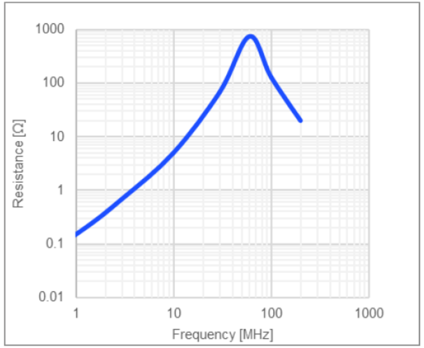




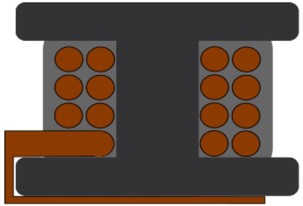
Larger Area for E-field Radiation

Shielded (Molded)

ACR

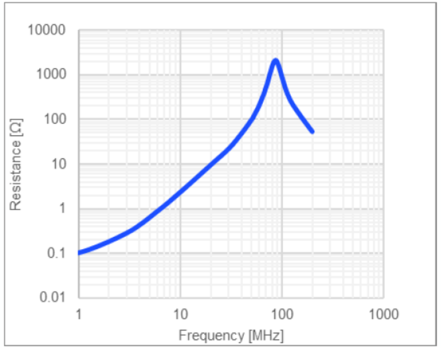


C_P = 8pF



Semi-Shielded (Epoxy Coating)

ACR



C_P = 3pF

Shielded Inductors: Mythbusting

From previous experience, it is true that in some cases shielded inductors improve EMC results.

In this particular test, the shielded inductor exhibits worse EMI than the semi-shielded inductor, due to the construction of the inductor.

Each design is unique, which is why it is important to test in the early stages to evaluate which components are best. Not all inductors are built equal.

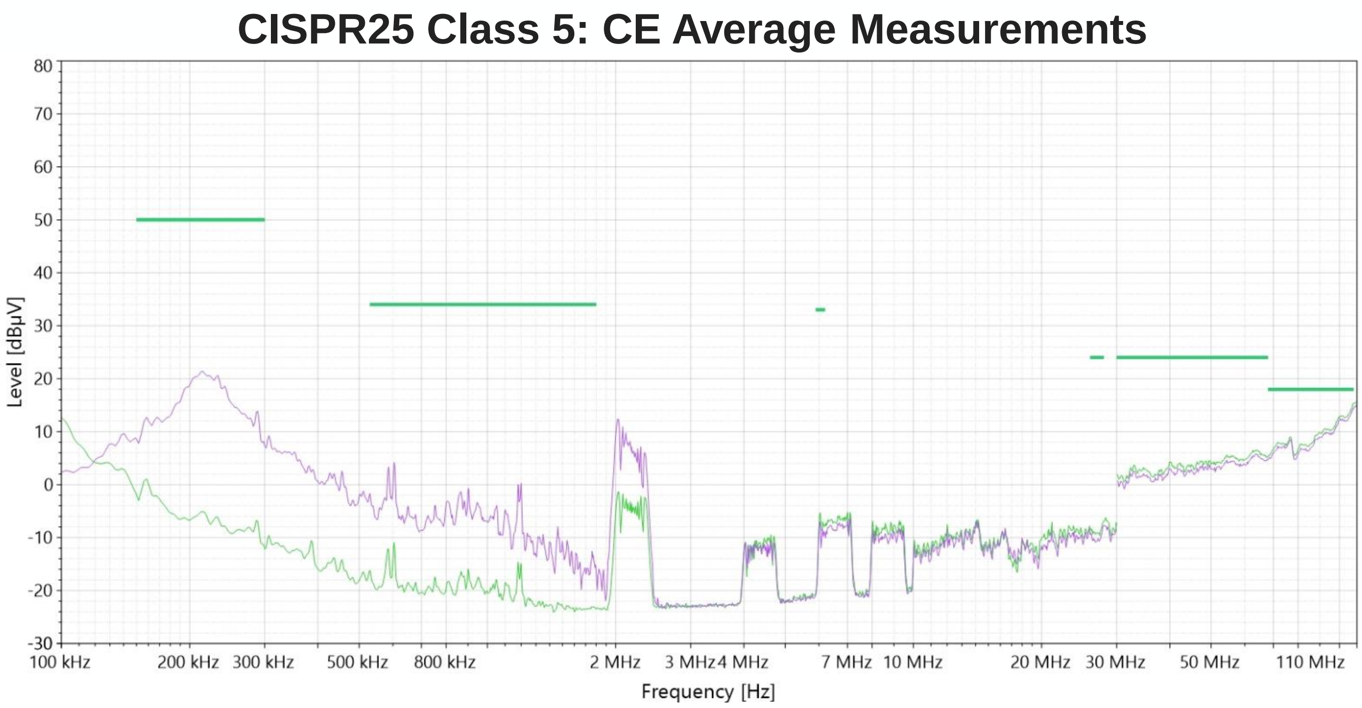
Lower Radiation

Credit. Christian Kueck

Extra Measurement: Changing the Filter from Inductor to Ferrite

TB15: L2 as 1µH Inductor

TB15: L2 as Ferrite Bead



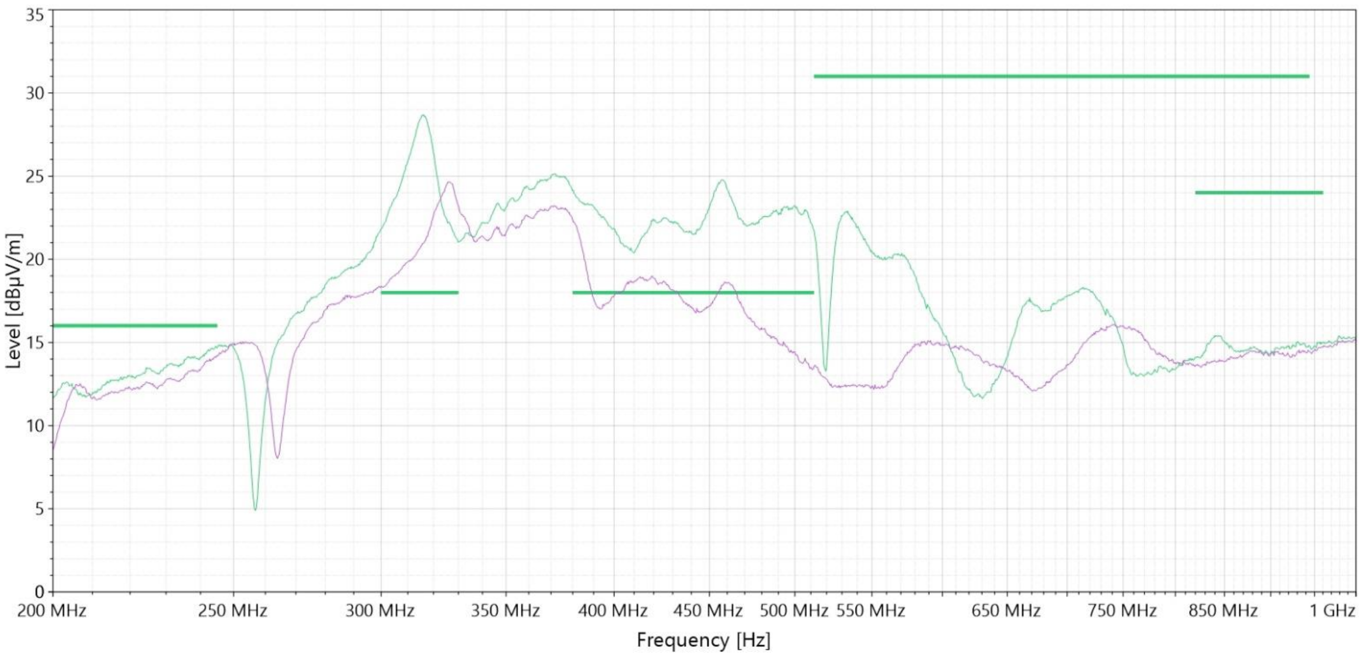
The ferrite bead provides less attenuation at the fundamental frequency, but is similar in the FM band.

Extra Measurement: Changing the Filter from Inductor to Ferrite

CISPR25 Class 5: RE Log Average Measurements (Vertical)

TB15: L2 as 1µH Inductor

TB15: L2 as Ferrite Bead



The ferrite bead provides improves radiated EMI across all bands.

Conclusions

- Many EMC recommendations given in seminars are not valid across all designs. There are several variables at play (e.g. PCB size, load type, harnesses, etc.).
- The best way to ensure that a design is going in the right direction is through testing in the early stages of development.
- Start the design following typical EMC best practices, such as symmetrical input capacitance, adding a 100nF capacitor, choosing a good inductor, etc.
- Test the initial design and see what its shortcomings are, then come up with a plan to fix the issues in the identified frequencies.
- Execute the improvement plan, then repeat the testing to confirm that the new system is on the right track.

Q&A

Let us know your questions