Multi-Phase MPQ2908A with Thermal Balancing

12V Output DC/DC Converter for 48V Batteries

Contents

1 Overview

1.1 Description

New automotive designs are adopting 48V power systems to reduce the weight and power loss in the vehicle's cable harnesses. Moreover, when the system must withstand high loads, the required power increases, which means it is vital to use power converter topologies with higher deliverable power, such as an interleaved topology. When using this topology, it is usually required to optimize thermal distribution to equalize the MOSFETs' degradation and avoid overheating parts of the board. An excellent layout can help with these thermal constraints, as well as promoting good current sharing between both controllers by equally distributing the load current between all converters. Passing the same current through both phases, as well as creating a symmetrical layout, helps the MOSFETs experience an equal temperature rise, which means they will degrade at a similar speed.

This reference design showcases a 48V to 12V interleaved converter that can supply up to 20A of output load. To improve current sharing between both controllers, a thermal balancing circuit is implemented, and a frequency spread spectrum (FSS) modulator is added to reduce EMC.

1.2 Features

- Wide 4V to 60V Operating Input Range
- Dual N-Channel MOSFET Driver Phases
- 0.8V Reference Voltage with ±1.5% Accuracy for Over-Temperature Conditions
- Low-Dropout Operation: Maximum Duty Cycle at 99.5%
- 100kHz to 1000kHz Configurable Frequency
- 180° Out-of-Phase SYNCO Pin
- Configurable Soft Start (SS)
- Power Good (PG) Output Voltage (V_{OUT}) Monitoring
- Selectable Cycle-by-Cycle Current Limit
- Output Over-Voltage Protection (OVP)
- Over-Current Protection (OCP)
- External Reverse-Polarity Protection (RPP)
- External Input OVP
- Forced Continuous Conduction Mode (CCM)
- External Frequency Spread Spectrum (FSS) Modulation
- Enable Phase Thermal Balancing
- Available in TSSOP20-EP and QFN-20 (3mmx4mm) Packages
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade 1

Figure 1: EVQ2908A_48V_L_02A

1.3 Applications

- Automotive and Industrial Power Systems

High Voltage

Warning: Although this board is designed to satisfy safety requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

2 Reference Design

2.1 Block Diagram

Figure 2 shows the reference design block diagram. The MPQ2908A is a buck converter with 48V nominal input, 12V/20A output capability, input EMI filter, reverse-polarity protection (RPP), over-voltage protection (OVP), two-phase interleaving, frequency spread spectrum (FSS) modulation, and phase thermal balancing.

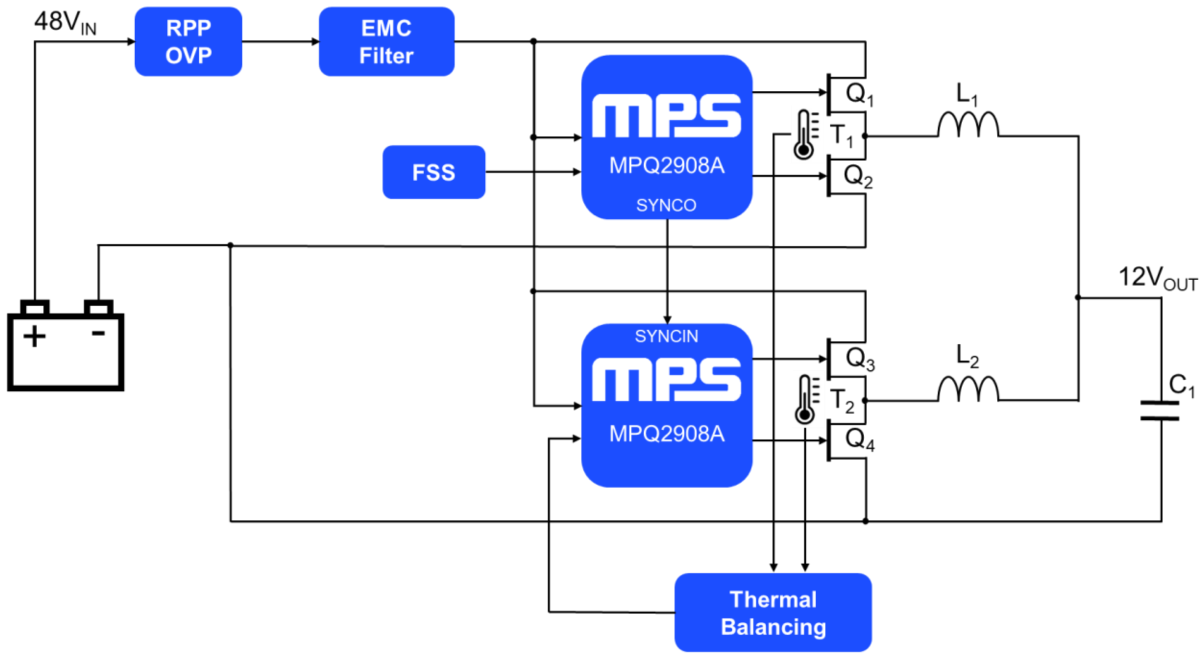


Figure 2: Block Diagram

2.2 Related Solutions

This reference design is based on the following MPS solution(s):

Table 1: System Specifications

MPS Integrated Circuit	Description
MPQ2908A	4V to 60V input, current mode, synchronous step-down controller, AEC-Q100 qualified

2.3 System Specifications

Table 2: System Specifications

Parameter	Specification
Input voltage range (V_{IN})	$24V_{DC}$ to $60V_{DC}$
Output voltage (V_{OUT})	$12V_{DC}$
Maximum output current (I_{OUT})	20A (with 12V output)
Switching frequency (f_{SW})	225kHz
Board form factor	150mmx100mm
Peak efficiency	95.83% (13A load, 48V input)
12V output ripple	$22mV_{PP}$

2.4 Schematic

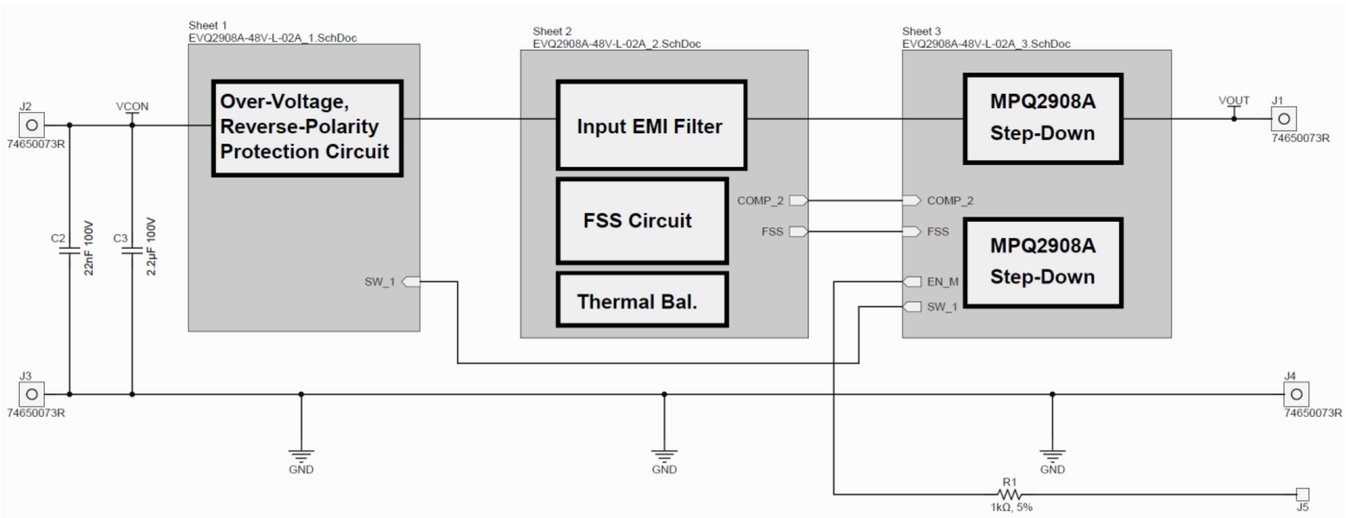


Figure 3: Schematic (Page 1)

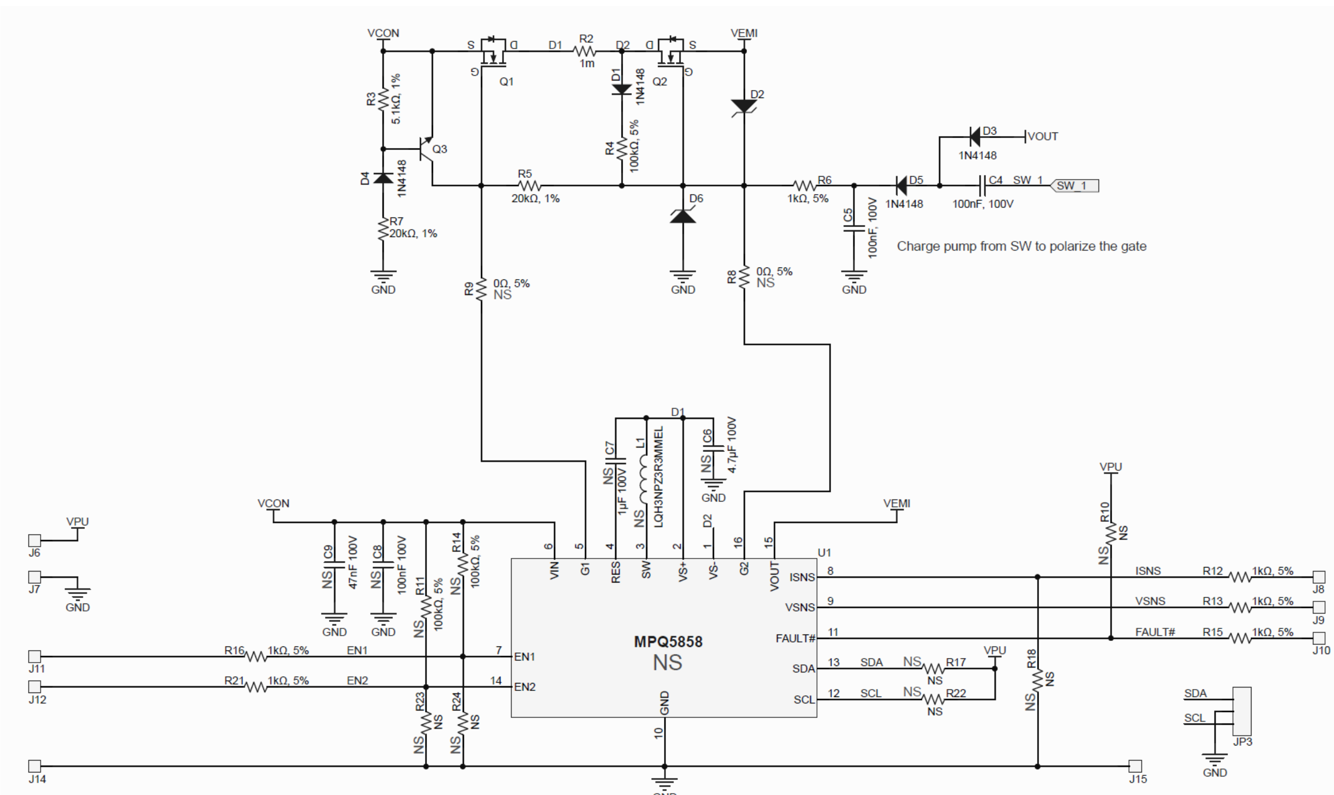


Figure 4. Schematic (Page 2)

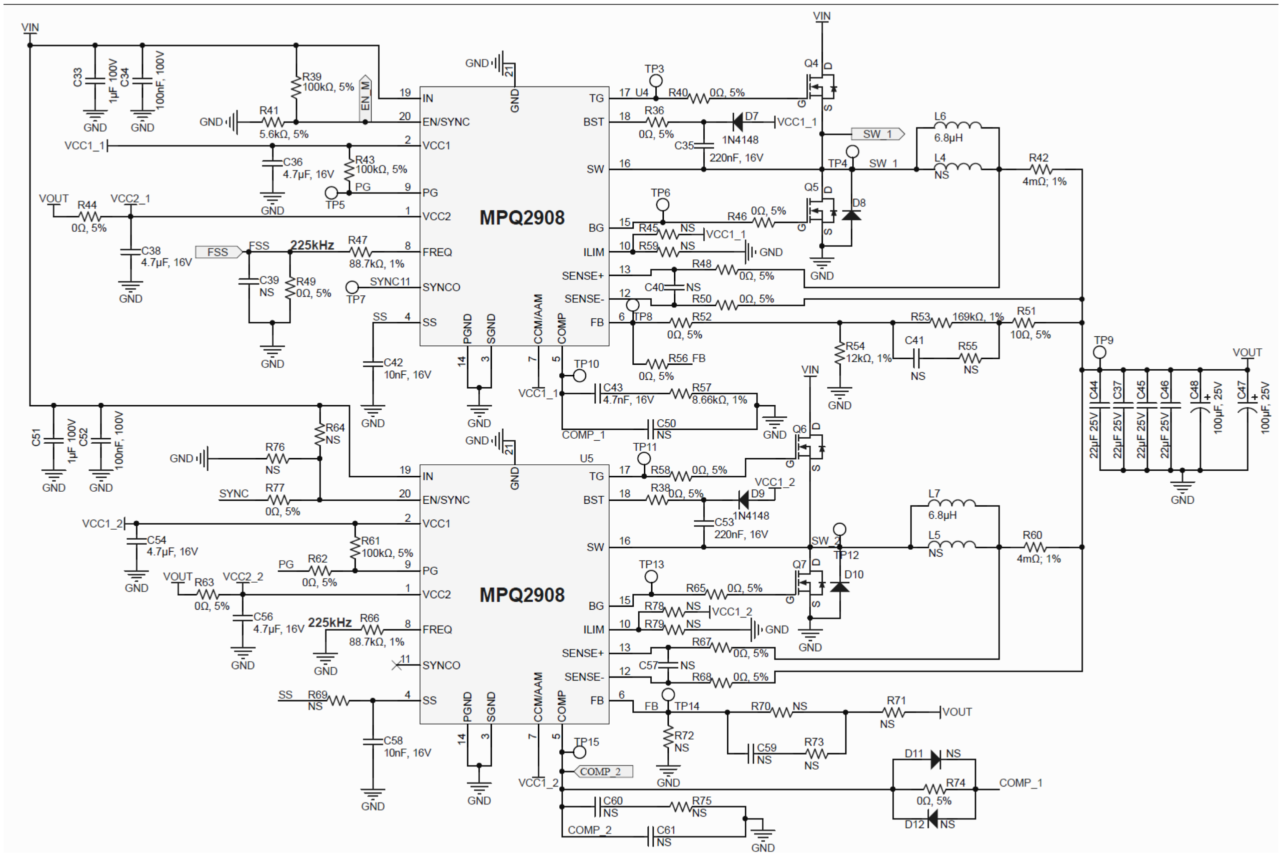


Figure 5: Schematic (Page 3)

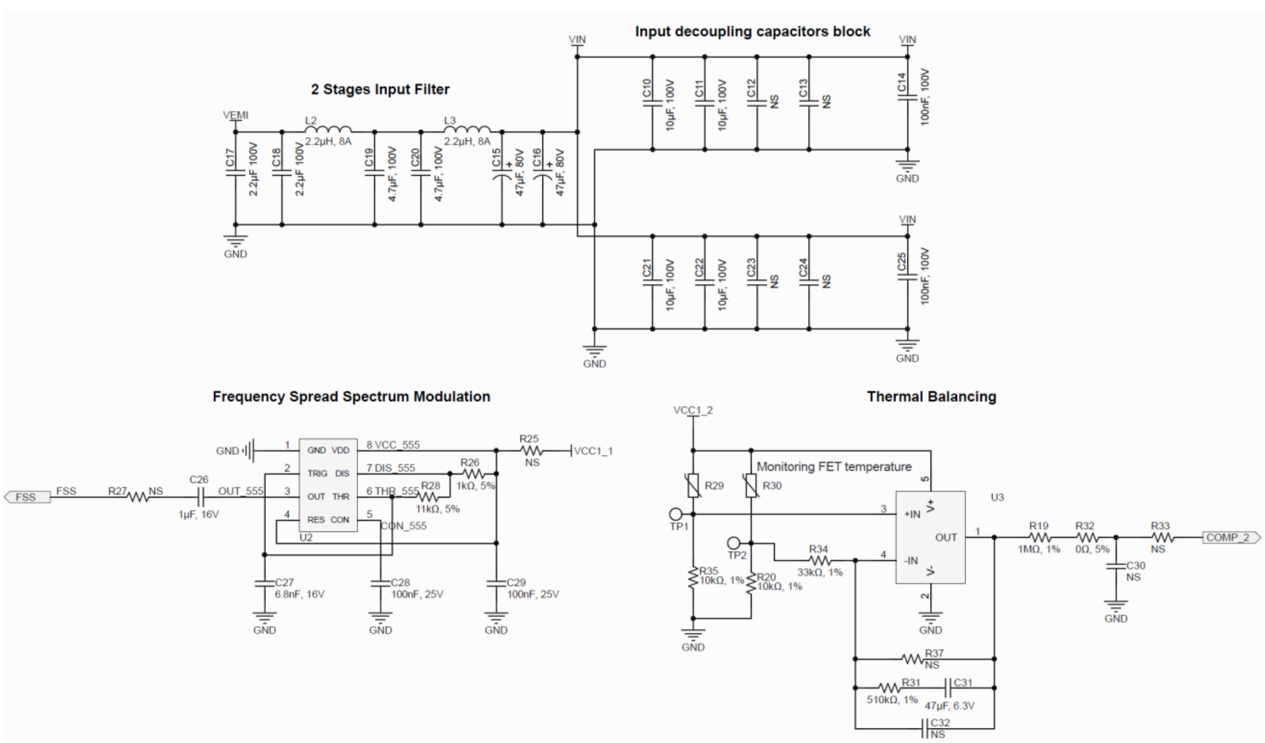


Figure 6. Schematic (Page 4)

2.5 BOM

Table 3: Bill of Materials

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
3	C1, C33, C51	1µF, 100V	10%, X7S, MLCC	0805	Murata	GCM21BC72A105KE36L
1	C2	22nF, 100V	5%, X7R, MLCC	1206	Kemet	C1206C223J1RACTU
3	C3, C17, C18	2.2µF, 100V	10%, X7S, MLCC	1206	Murata	GCM31CC72A225KE02L
6	C4, C5, C14, C25, C34, C52	100nF, 100V	10%, X7R, MLCC	0603	Murata	GCJ188R72A104KA01D
4	C10, C11, C21, C22	10µF, 100V	10%, X7S, MLCC	2210	TDK	CGA9N3X7S2A106K230KE
2	C15, C16	47µF, 80V	Aluminium electrolytic capacitor	10mmx 10mm	Panasonic	EEE-FN1K470UV
2	C19, C20	4.7µF, 100V	10%, X7S, MLCC	1210	Murata	GCM32DC72A475KE02L
1	C26	1µF, 16V	10%, X7R, MLCC	0603	Murata	GCM188R71C105KA64J
1	C27	6.8nF, 16V	10%, X7R, MLCC	0603	Vishay Vitramon	VJ0603Y682KXJCW1BC
2	C28, C29	100nF, 25V	10%, X7R, MLCC	0603	Kemet	C0603C104K3RAC7013
1	C31	47µF, 6.3V	20%, X5R, MLCC	0603	Taiyo Yuden	JMK107BBJ476MA-RE
2	C35, C53	220nF, 16V	10%, X7R, MLCC	0603	Kemet	C0603X224K4RACTU
4	C36, C38, C54, C56	4.7µF, 16V	10%, X5R, MLCC	0603	TDK	C1608X5R1C475K080AC
4	C37, C44, C45, C46	22µF 25V	10%, X5R, MLCC	1210	Kemet	C1210C226K3PACTU
2	C42, C58	10nF, 16V	5%, X7R, MLCC	0603	Kemet	C0603C103J4RACTU
1	C43	4.7nF, 16V	10%, X7R, MLCC	0603	Kemet	C0603C472K4RACTU
2	C47, C48	100µF, 25V	Aluminium electrolytic capacitors	10mmx 10mm	Panasonic	EEE-FN1E101UV
6	D1, D3, D4, D5, D7, D9	200V, 0.25A	General-purpose diode, V_{BREAK} = 200V	SOD-323	Nexperia	BAS321,115
1	D2	10V, 5mA	Zener diode	SOD-523	On Semiconductor	SZMM5Z10VT5G
1	D6	65V, 50nA	Zener diode	SOT-23	On Semiconductor	SZBZX84C62LT1G
2	D8, D10	150V, 1A	Schottky rectifier diode	SOD-123FL	Rohm	RB168MM150TFTR
4	J1, J2, J3, J4	M3, 50A	M3 through-hole terminal	7mmx 7mm	Wurth	74650073R
2	L2, L3	2.2µH, 8A	Fixed inductor	7030	Eaton Bussmann	HCMA0703-2R2-R
2	L6, L7	6.8µH, 11.6A	Fixed inductor	13mmx 12.5mm	TDK	SPM12565VT-6R8M-D
2	Q1, Q2	80V	N-channel MOSFET, I_D = 123A, $V_{DSBREAK}$ = 80V	SOIC-8	On Semiconductor	NVMFS6H818NT1G
1	Q3	NPN	NPN BJT	SOT-23-3	Nexperia	BC846215

4	Q4, Q5, Q6, Q7	80V	N-channel MOSFET, I_D = 60A, $V_{DSBREAK}$ = 80V	SO-8L	Vishay Siliconix	SQJA82EP-T1_GE3
8	R1, R6, R12, R13, R15, R16, R21, R26	1kΩ, 5%	Thick film resistor	0603	Yageo	RC0603JR-131KL
1	R2	1mΩ, 2%	Current-sense resistor	1530	Ohmite	FC4L76R001GER
1	R3	5.1kΩ, 1%	Thick film resistor	0603	Yageo	RC0603FR-075K1L
4	R4, R39, R43, R61	100kΩ, 5%	Thick film resistor	0603	Vishay	CRCW0603100KFKEBC
2	R5, R7	20kΩ, 1%	Thick film resistor	0603	Yageo	RC0603FR-1320KL
1	R19	1MΩ, 1%	Thick film resistor	0603	Yageo	RC0603FR-071ML
2	R20, R35	10kΩ, 1%	Thick film resistor	0603	Rohm	ESR03EZPF1002
1	R28	11kΩ, 5%	Thick film resistor	0603	Panasonic	ERJ-3GEYJ113V
2	R29, R30	10kΩ, 0.5%	NTC thermistor	0603	TDK	NTCG163JX103DTDS
1	R31	510kΩ, 1%	Thick film resistor	0603	Yageo	AC0603FR-07510KL
19	R32, R36, R38, R40, R44, R46, R48, R49, R50, R52, R56, R58, R62, R63, R65, R67, R68, R74, R77	0Ω	Thick film resistor	0603	Vishay Dale	CRCW06030000Z0EAHP
1	R34	33kΩ, 1%	Thick film resistor	0603	Yageo	RC0603FR-0733KL
1	R41	5.6kΩ, 5%	Thick film resistor	0603	Vishay Dale	CRCW06035K60JNEB
2	R42, R60	4mΩ, 1%	Current-sense resistor	2512	Susumu	KRL6432E-C-R004-F-T1
2	R47, R66	88.7kΩ, 1%	Thick film resistor	0603	Panasonic	ERJ-3EKF8872V
1	R51	10Ω, 5%	Thick film resistor	0603	Yageo	RC0603JR-0710RL
1	R53	169kΩ, 1%	Thick film resistor	0603	Panasonic	ERJ-3EKF1693V
1	R54	12kΩ, 1%	Thick film resistor	0603	Panasonic	ERJ-1GNF1202C
1	R57	8.66kΩ, 1%	Thick film resistor	0603	Panasonic	ERJ-3EKF8661V
1	U2	2V to 50V	555 timer	SOIC-8	TI	TLC555QDRQ1
1	U3	150kHz, 130dB	Rail-to-rail operational amplifier	TSOT-23	Analog Devices	LTC2054IS5#TRMPBF
2	U4, U5	MPQ2908A	Buck switching power converter	QFN-20 (3mmx 4mm)	MPS	MPQ2908AGLE-AEC1

2.6 PCB Layout

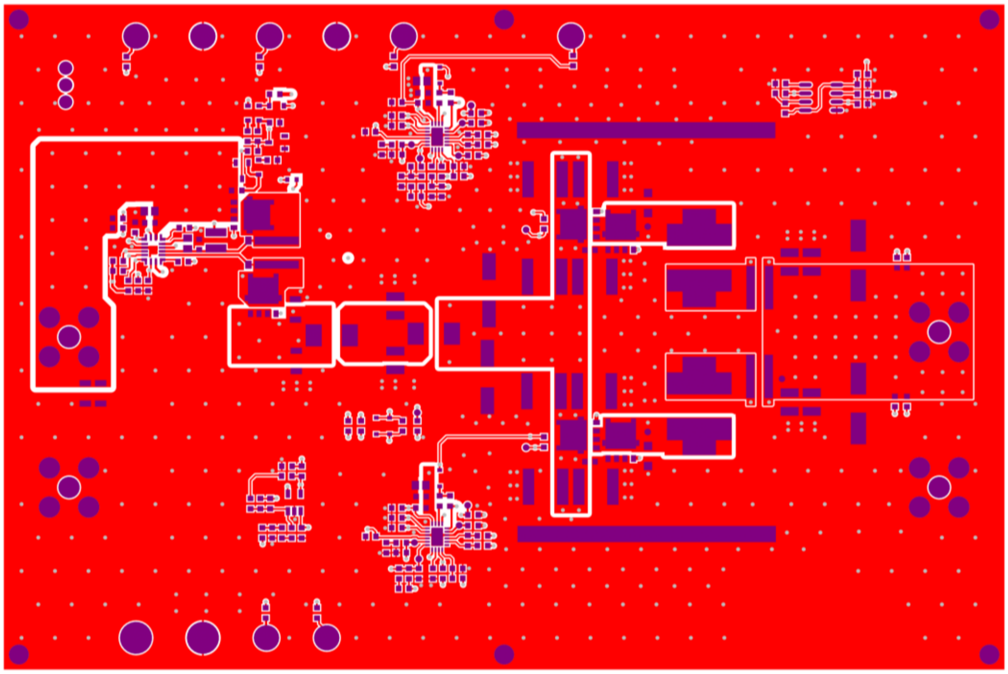


Figure 7: Top Layer

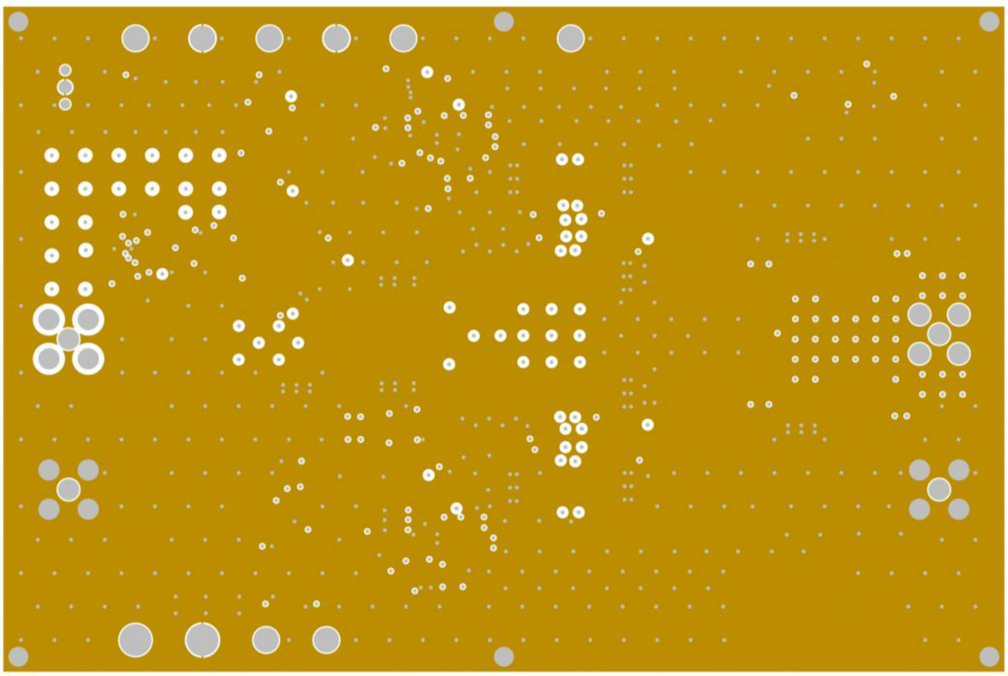


Figure 8: Mid-Layer 1

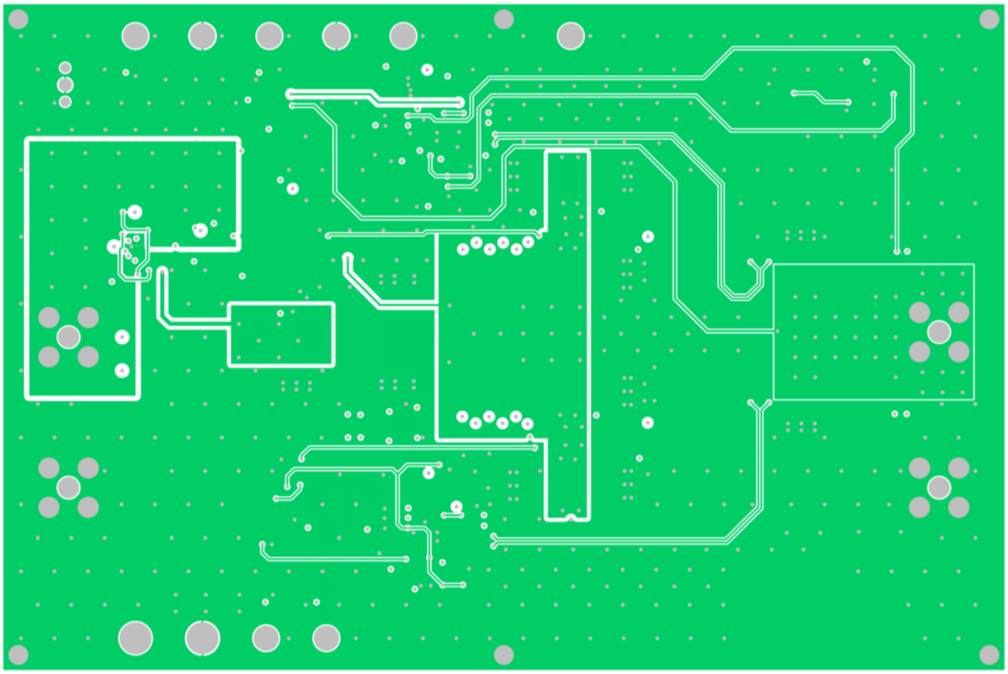


Figure 9: Mid-Layer 2

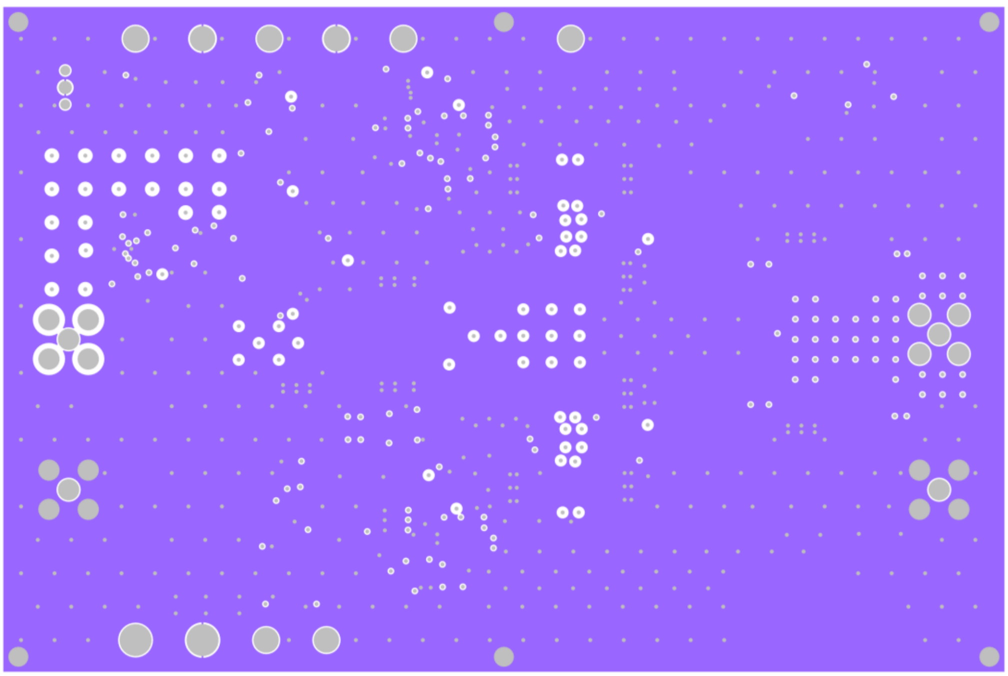


Figure 10: Mid-Layer 3

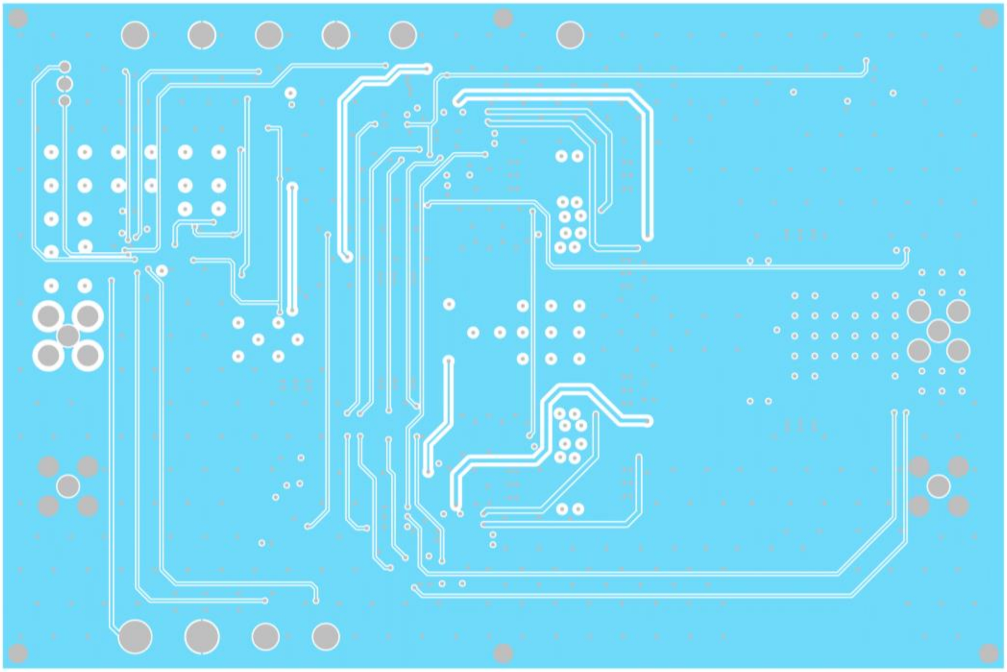


Figure 11: Mid-Layer 4

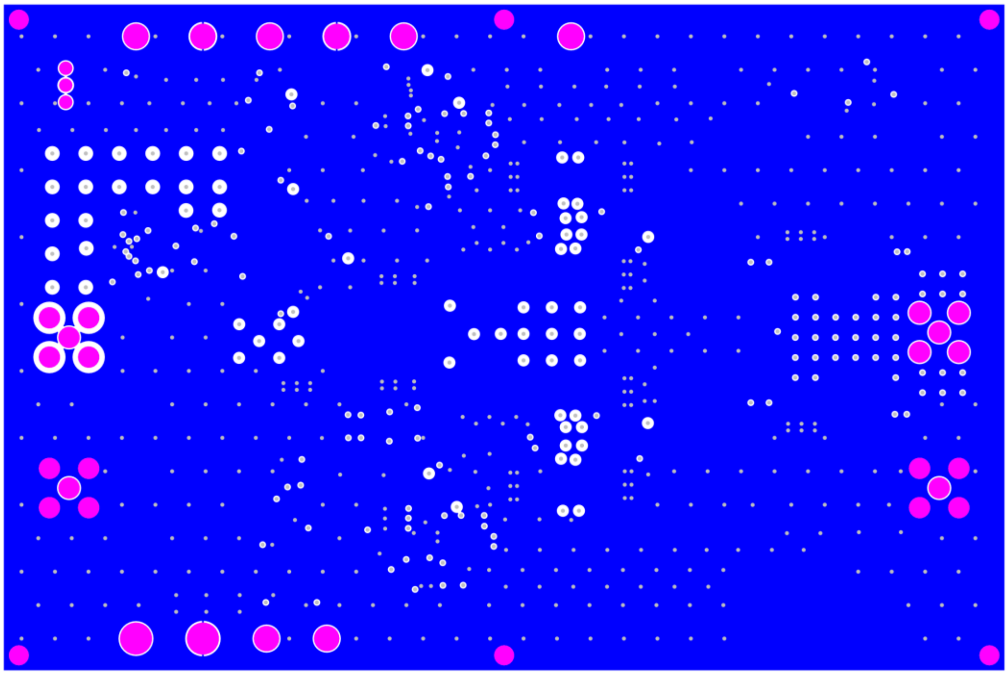


Figure 12: Bottom Layer

3 Test Results

3.1 Typical Performance Characteristics

V_{IN} = 48V, V_{OUT} = 12V, L = 6.8µH T_A = 25°C, CCM, unless otherwise noted.

Figure 13: Efficiency vs. Load Current
Light load, converter only

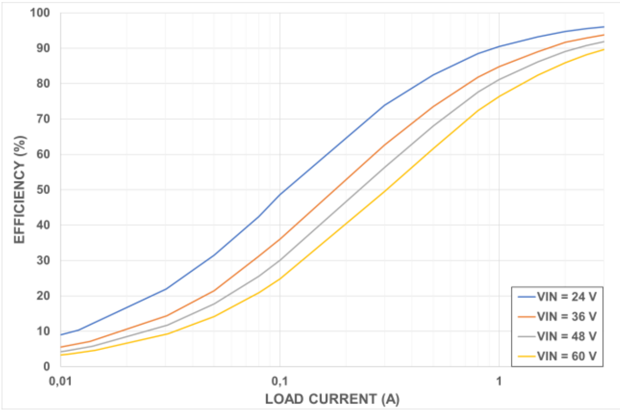


Figure 14: Efficiency vs. Load Current
High load, converter only

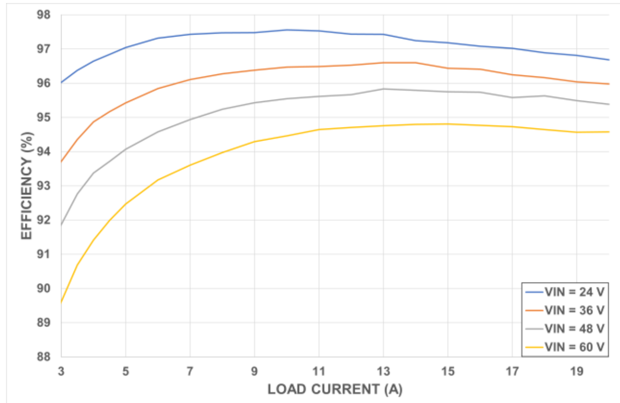


Figure 15: Efficiency vs. Load Current
Light load, full system

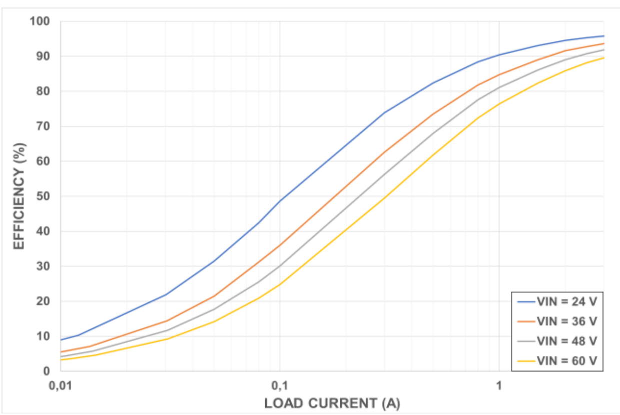


Figure 16: Efficiency vs. Load Current
High load, full system

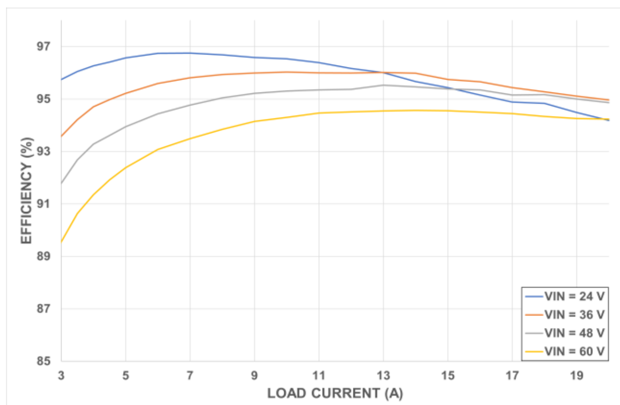


Figure 17: Power Loss vs. Load Current
Light load, converter only

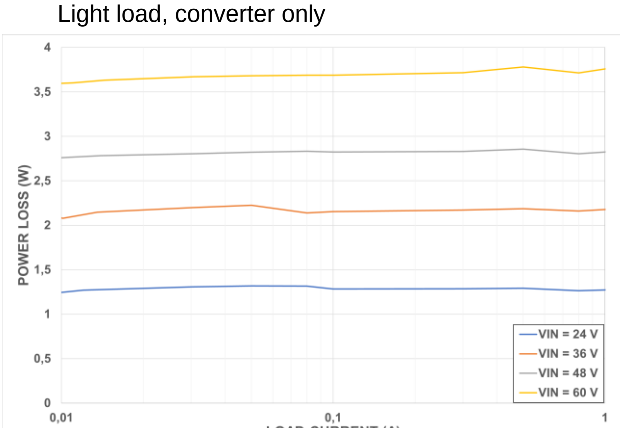


Figure 18: Power Loss vs. Load Current
High load, converter only

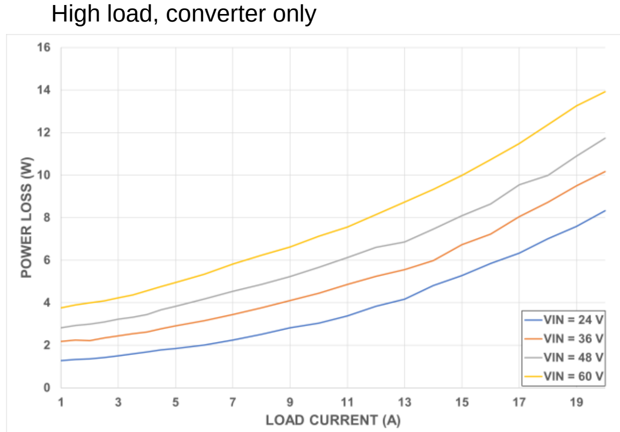


Figure 19: Power Loss vs. Load Current
Light load, full system

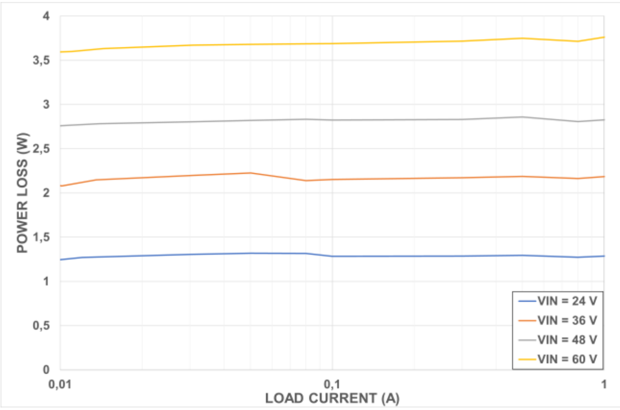


Figure 20: Power Loss vs. Load Current
High load, full system

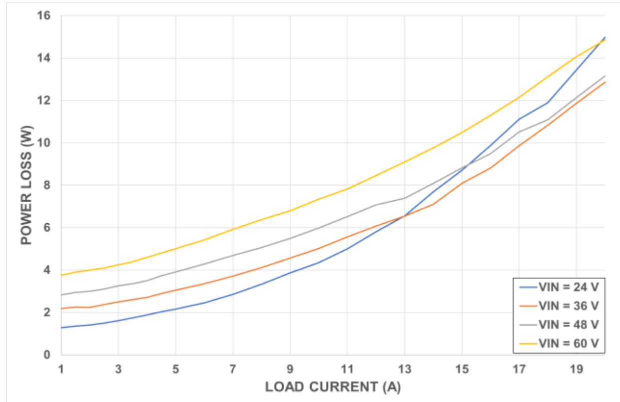


Figure 21: Output Voltage vs. Load Current

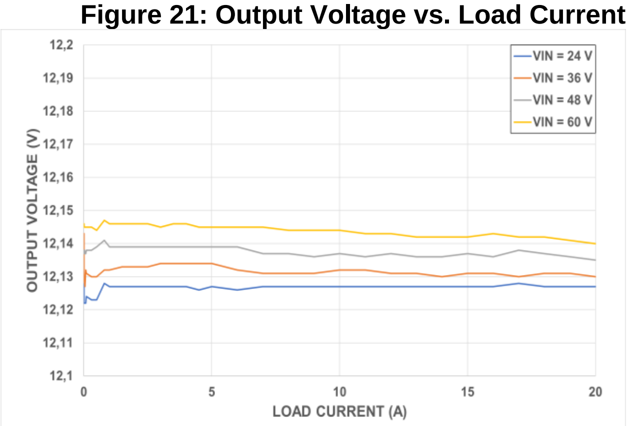


Figure 22: Output Voltage vs. Input Voltage

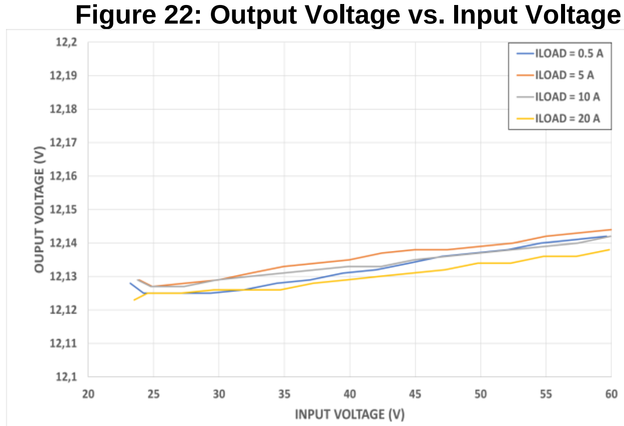
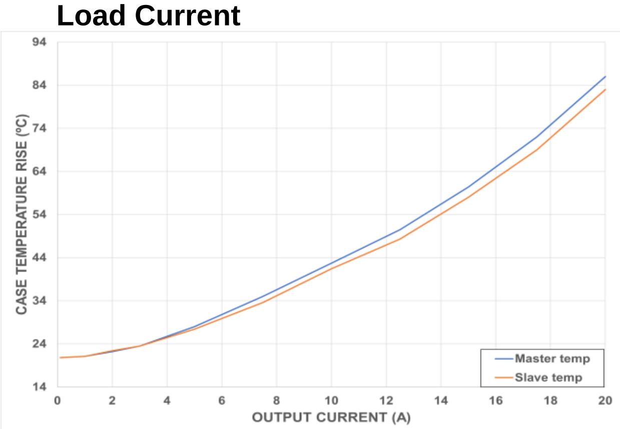


Figure 23: Case Temperature Rise vs. Load Current

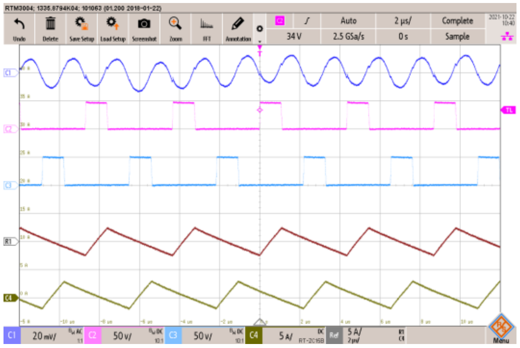


3.2 Time Domain Waveforms

V_{IN} = 48V, V_{OUT} = 12V, L = 6.8µH T_A = 25°C, CCM, unless otherwise noted.

Figure 24: Steady State
I_{OUT} = 0A

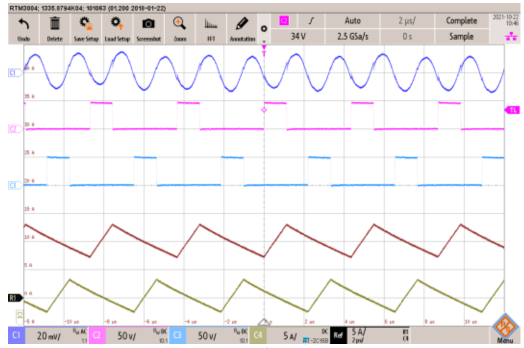
C1: V_{OUT}/AC 20mV/div.
C2: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R1: I_{L1} 5A/div.
C4: I_{L2} 5A/div.



2µs/div.

Figure 25: Steady State
I_{OUT} = 20A

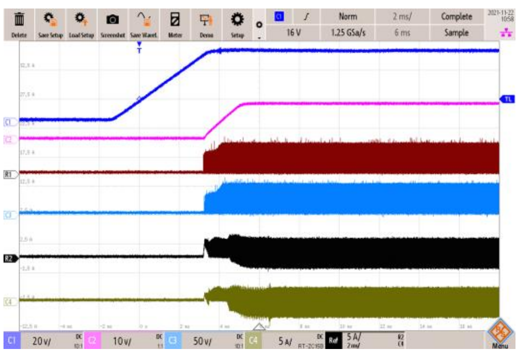
C1: V_{OUT}/AC 20mV/div.
C2: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R1: I_{L1} 5A/div.
C4: I_{L2} 5A/div.



2µs/div.

Figure 26: Start-Up through VIN
I_{OUT} = 0A

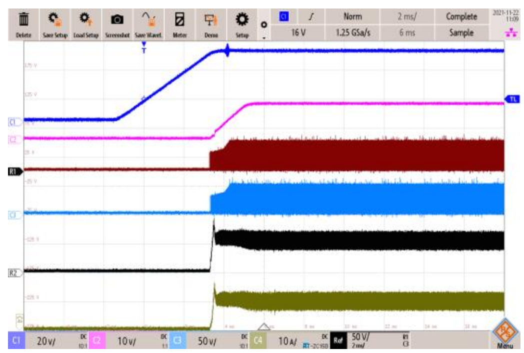
C1: V_{IN} 20V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 5A/div.
C4: I_{L2} 5A/div.



2ms/div.

Figure 27: Start-Up through VIN
I_{OUT} = 20A

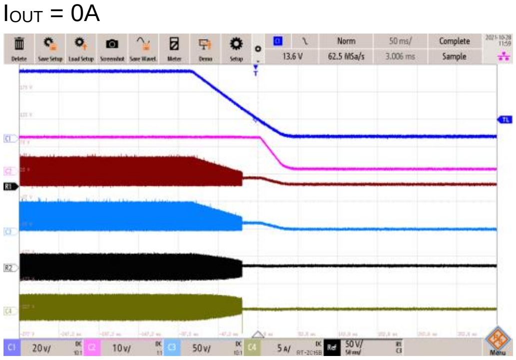
C1: V_{IN} 20V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.



2ms/div.

Figure 28: Shutdown through VIN
I_{OUT} = 0A

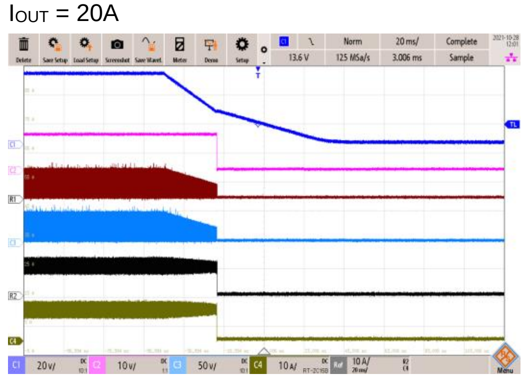
C1: V_{IN} 20V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 5A/div.
C4: I_{L2} 5A/div.



50ms/div.

Figure 29: Shutdown through VIN
I_{OUT} = 20A

C1: V_{IN} 20V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.

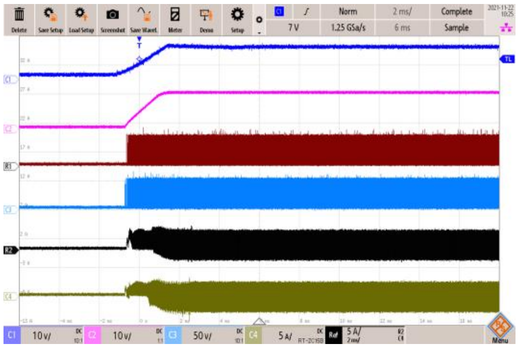


20ms/div.

Figure 30: Start-Up through EN/SYNC

I_{OUT} = 0A

C1: V_{EN} 10V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 5A/div.
C4: I_{L2} 5A/div.

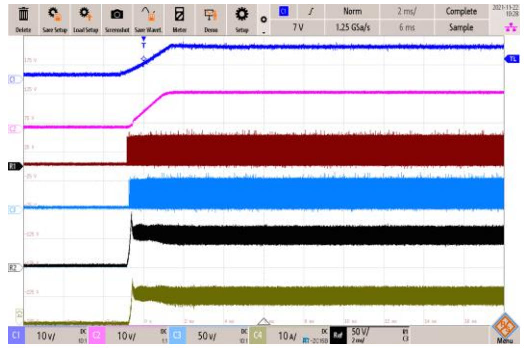


2ms/div.

Figure 31: Start-Up through EN/SYNC

I_{OUT} = 20A

C1: V_{EN} 10V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.

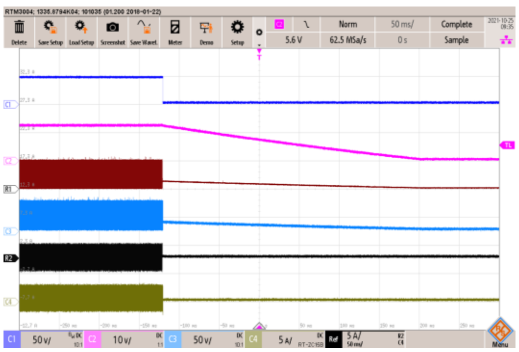


2ms/div.

Figure 32: Shutdown through EN/SYNC

I_{OUT} = 10mA

C1: V_{EN} 50V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 5A/div.
C4: I_{L2} 5A/div.

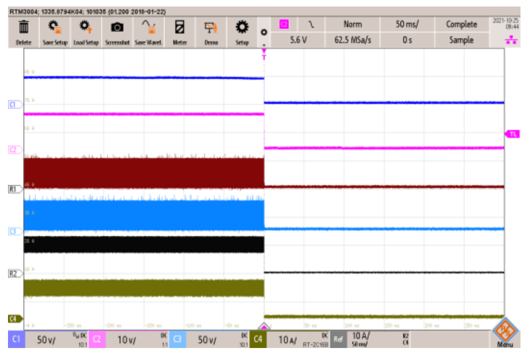


50ms/div.

Figure 33: Shutdown through EN/SYNC

I_{OUT} = 20A

C1: V_{EN} 50V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.

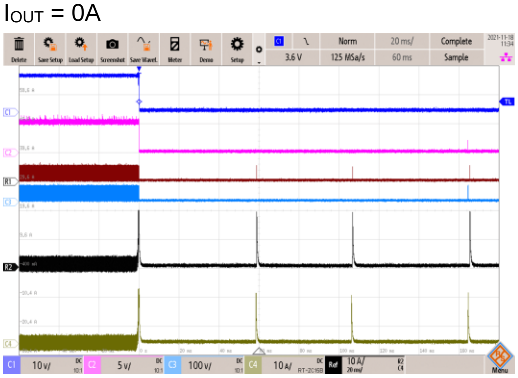


50ms/div.

Figure 34: SCP Entry

I_{OUT} = 0A

C1: V_{OUT} 10V/div.
C2: V_{PG} 5V/div.
R1: V_{SW1} 100V/div.
C3: V_{SW2} 100V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.

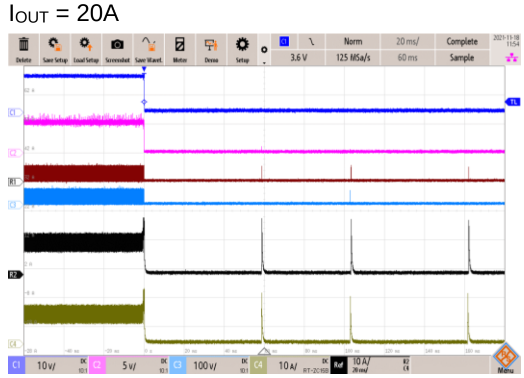


20ms/div.

Figure 35: SCP Entry

I_{OUT} = 20A

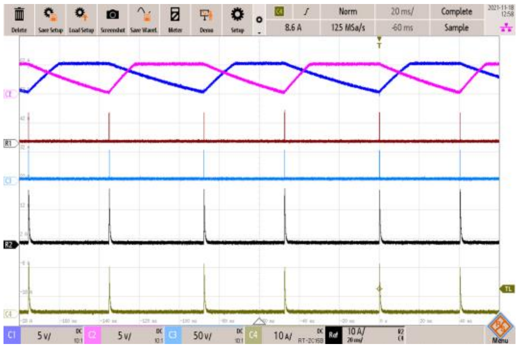
C1: V_{OUT} 10V/div.
C2: V_{PG} 5V/div.
R1: V_{SW1} 100V/div.
C3: V_{SW2} 100V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.



20ms/div.

Figure 36: SCP Steady State

Short circuit

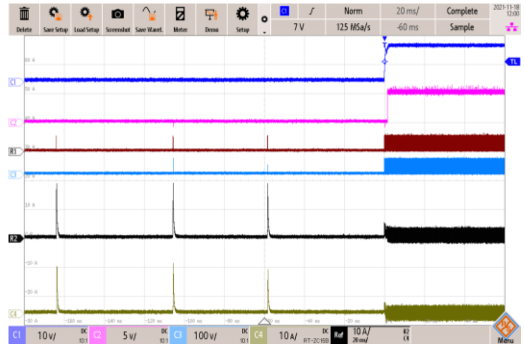


C1: V_{SS1} 5V/div.
C1: V_{SS2} 5V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.

20ms/div.

Figure 37: SCP Recovery

I_{OUT} = 0A

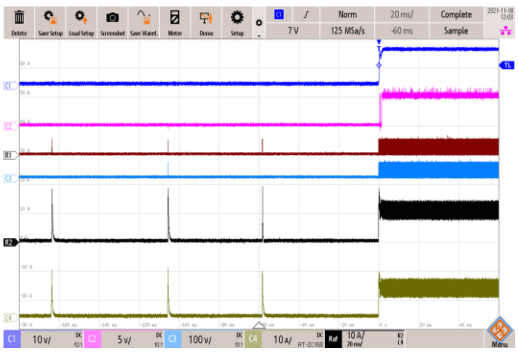


C1: V_{OUT} 10V/div.
C2: V_{PG} 5V/div.
R1: V_{SW1} 100V/div.
C3: V_{SW2} 100V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.

20ms/div.

Figure 38: SCP Recovery

I_{OUT} = 20A

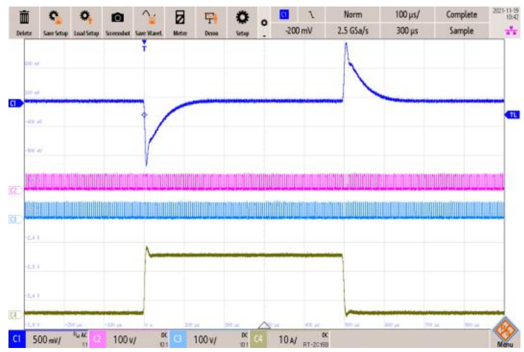


C1: V_{OUT} 10V/div.
C2: V_{PG} 5V/div.
R1: V_{SW1} 100V/div.
C3: V_{SW2} 100V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.

20ms/div.

Figure 39: Load Transient Response

I_{OUT} = 0A to 20A

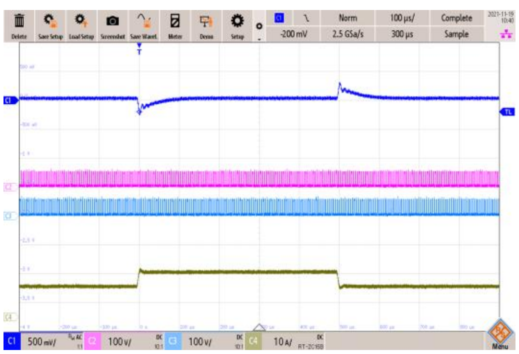


C1: V_{OUT}/AC 0.5V/div.
C2: V_{SW1} 100V/div.
C3: V_{SW2} 100V/div.
C4: I_{OUT} 10A/div.

100µs/div.

Figure 40: Load Transient Response

I_{OUT} = 10A to 15A

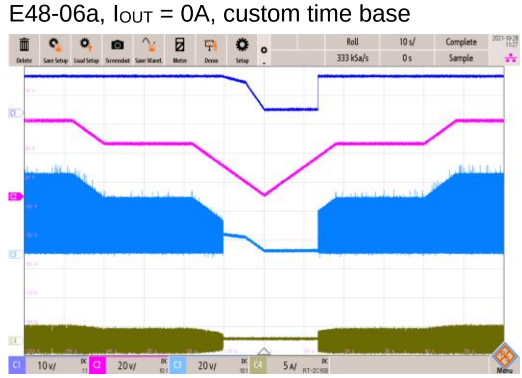


C1: V_{OUT}/AC 0.5V/div.
C2: V_{SW1} 100V/div.
C3: V_{SW2} 100V/div.
C4: I_{OUT} 10A/div.

100µs/div.

Figure 41: Test Pulse, Slow Ramp Up/Down

E48-06a, I_{OUT} = 0A, custom time base



C1: V_{OUT} 10V/div.
C2: V_{IN} 20V/div.
C3: V_{SW1} 20V/div.
C4: I_{L1} 5A/div.

10s/div.

Figure 42: Test Pulse (Slow Ramp Up/Down)
E48-06a, I_{OUT} = 20A, custom time base

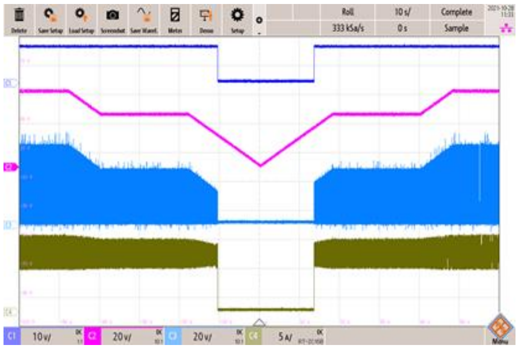


Figure 43: Test Pulse (Reset)
E48-08, V_{IN} = 52V, I_{OUT} = 0A, 1s pulses

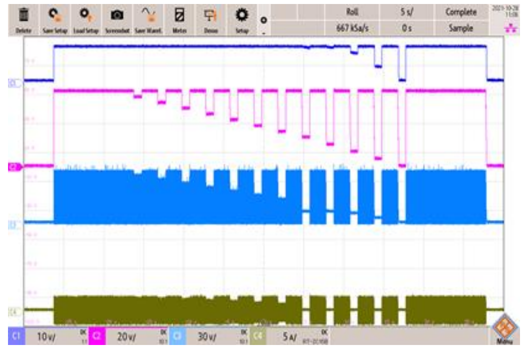


Figure 44: Test Pulse (Reset)
E48-08, V_{IN} = 52V, I_{OUT} = 20A, 1s pulses

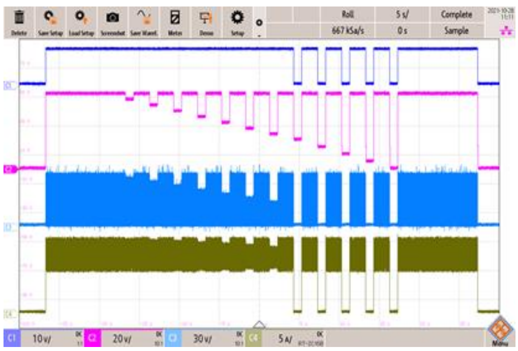


Figure 45: Test Pulse (Reset)
E48-08, V_{IN} = 52V, I_{OUT} = 0A, 100ms pulses

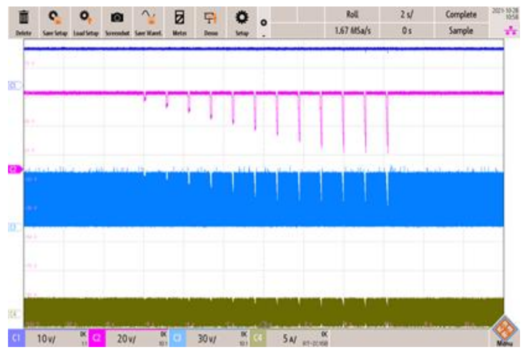


Figure 46: Test Pulse (Reset)
E48-08, V_{IN} = 52V, I_{OUT} = 20A, 100ms pulses

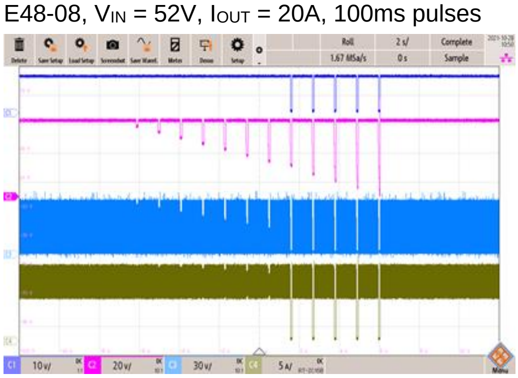


Figure 47: Cold Crank
E48-10, V_{IN} = 48V ↔ 24V, I_{OUT} = 0A

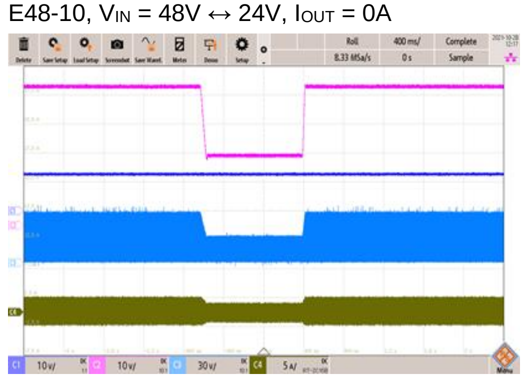
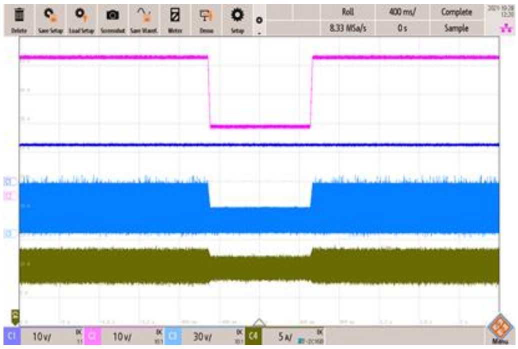


Figure 48: Cold Crank

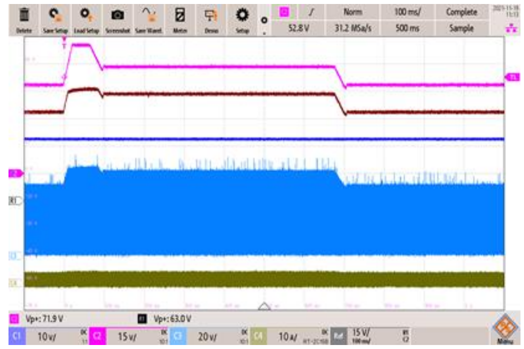
E48-10, V_{IN} = 48V to 24V, I_{OUT} = 20A



400ms/div.

Figure 49: Transient Response (Over-Voltage)

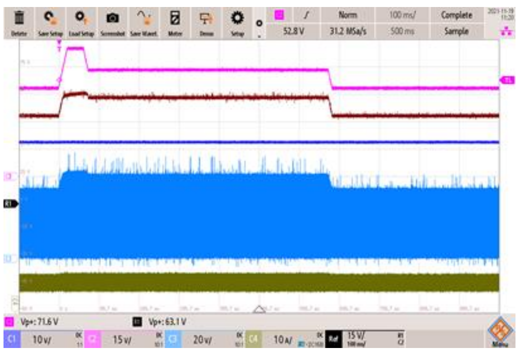
E48-02, I_{OUT} = 0A



100ms/div.

Figure 50: Transient Response (Over-Voltage)

E48-02, I_{OUT} = 20A

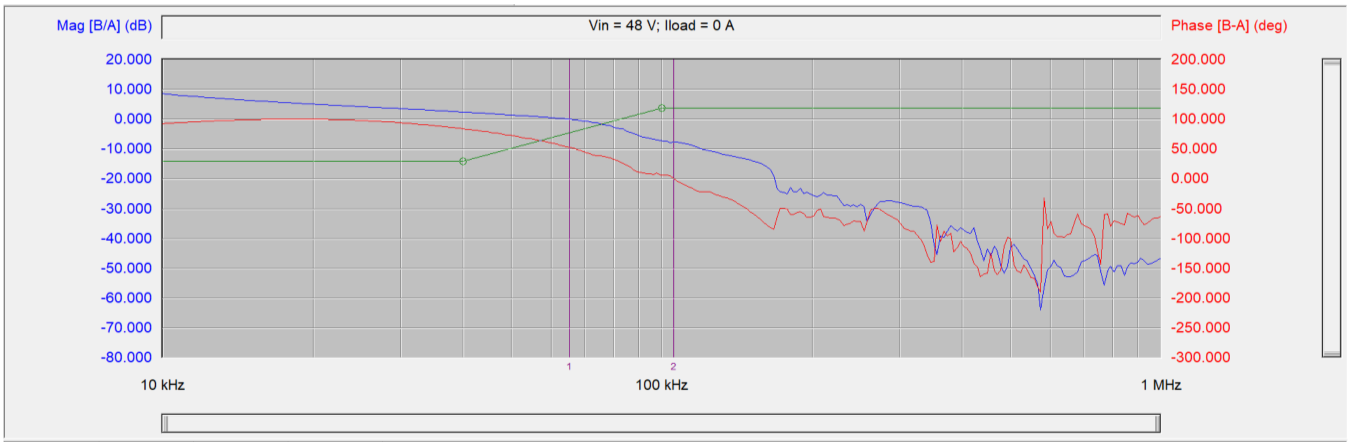


100ms/div.

3.3 Bode Plots

Figure 51: V_{IN} Bode Plot

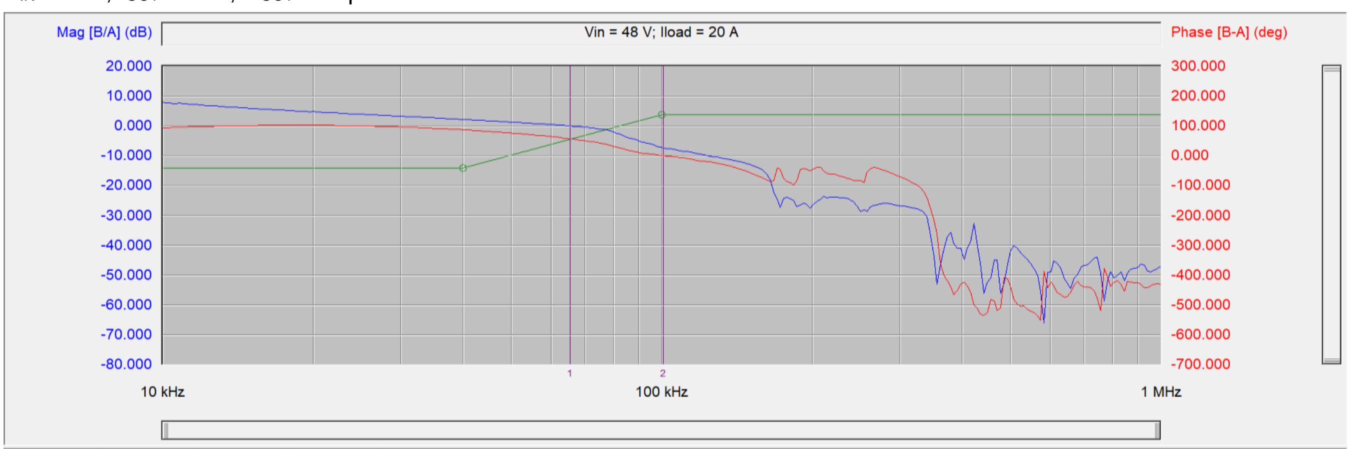
V_{IN} = 48V, I_{OUT} = 0A, C_{OUT} = 88µF



Data	M1	M2	M2 - M1
Frequency	65.20 kHz	105.57 kHz	40.38 kHz
Magnitude	0.004 dB	-7.539 dB	-7.543 dB
Phase	52.829 deg	-0.008 deg	-52.836 deg
Var. Source	471.74 mV	1.00 V	528.26 mV

Figure 52: V_{IN} Bode Plot

V_{IN} = 48V, I_{OUT} = 20A, C_{OUT} = 88µF



Data	M1	M2	M2 - M1
Frequency	65.49 kHz	100.52 kHz	35.02 kHz
Magnitude	0.001 dB	-7.242 dB	-7.243 dB
Phase	57.060 deg	-0.006 deg	-57.066 deg
Var. Source	475.52 mV	1.00 V	524.48 mV

4 Thermal Balance

While testing the previous version of the prototype, unequal current sharing was observed. This led to one phase's MOSFETs reaching a higher temperature than the other phase's MOSFETS. If the temperature difference became too great (due to unequal current sharing or one phase being exposed to a higher external temperature), the lifetime of one phase's MOSFETs would be greatly reduced.

A thermal balancing system was added to solve this issue. This system distributes the current across both phases to ensure that the phase temperatures are always equal. If one phase has a higher temperature, current is reduced in this phase so that the temperature difference is minimized. Then, as the overheated phase cools down, the load current distribution between both phases evens out.

Moreover, the thermal balancing circuit also reduces the BOM cost, while simultaneously reducing the required sizes of the MOSFETs and inductors. If heat is unequally shared between both phases, the designer must oversize circuit components (MOSFETs and inductors) to withstand larger currents and increase power dissipation. When heat is equally shared between phases, the design can be optimized for physically smaller MOSFETs and inductors.

Figure 53 shows the thermal balance schematic.

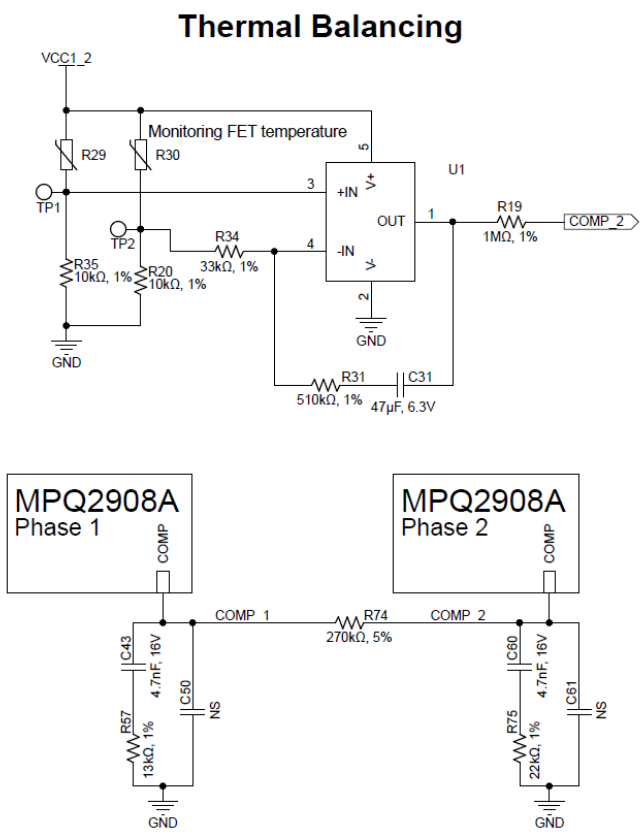


Figure 53: Thermal Balance Schematic

In this system, the temperature of both phases are compared. The differences between these temperatures is fed to a PI circuit. The PI transfer function can be calculated with Equation (1):

$$\frac{V_{OUT}}{V_{IN}}=-\left(\frac{R31}{R34}+\frac{1}{R34\times s\times C31}\right) \quad (1)$$

K_P and K_I can be estimated with Equation (2) and Equation (3), respectively:

$$K_P=\frac{R31}{R34} \quad (2)$$

$$K_I=\frac{1}{R34\times C31} \quad (3)$$

The PI controller's output is fed to the phase 2's COMP pin.

If the temperature of the phase 2 (T_2) is below the phase 1's temperature (T_1), the phase 2's COMP pin voltage (V_{COMP_2}) increases. Consequently, the current of this phase (I_{PHASE2}) increases. The same occurs when $T_1 < T_2$, though in this scenario, I_{PHASE2} decreases until $T_1 = T_2$.

Phase 1 is not connected to the thermal-balancing circuit. The output current (I_{LOAD}) is the combination of both phase currents ($I_{PHASE1} + I_{PHASE2}$) and is set by the load, meaning it is independent of the current distribution in the phases. Because of this, if I_{PHASE2} decreases due to thermal balancing control, then I_{PHASE1} automatically increases (and vice versa). As a result, phase 1 is influenced by the thermal-balancing circuit despite not being directly connected to it.

4.1 Thermal Balance Steady State Temperature Testing

V_{IN} = 48V, V_{OUT} = 12V, L = 6.8µH T_A = 25°C, CCM, unless otherwise noted.

Figure 58: Output Voltage
I_{OUT} = 0A, no external heat, thermal balance

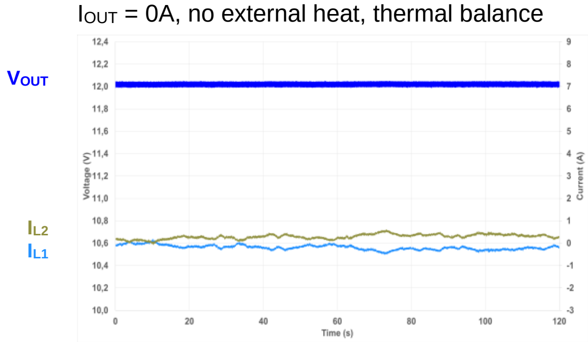


Figure 59: Phase Temperature
I_{OUT} = 0A, no external heat, thermal balance

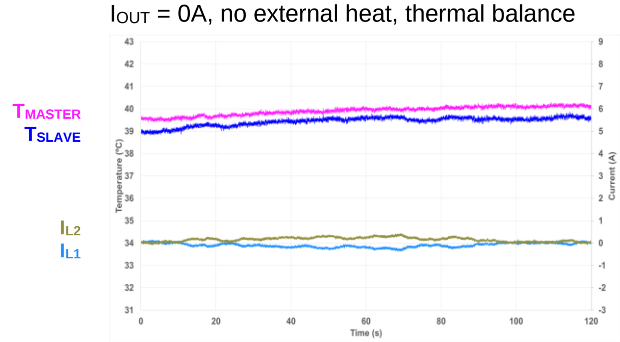


Figure 60: Output Voltage
I_{OUT} = 0A, 2W master heating, thermal balance

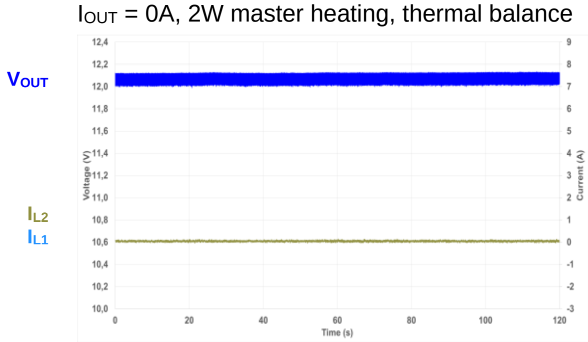


Figure 61: Phase Temperature
I_{OUT} = 0A, 2W master heating, thermal balance

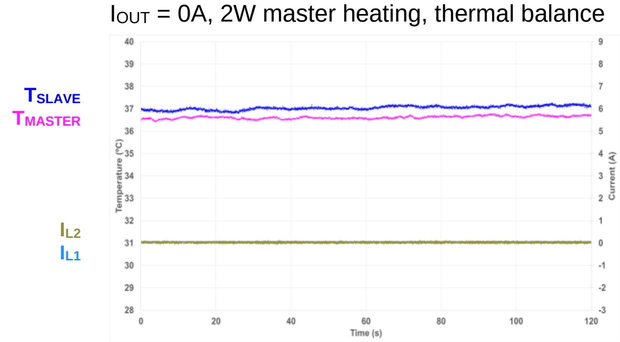


Figure 62: Output Voltage

I_{OUT} = 0A, 2W slave heating, thermal balance

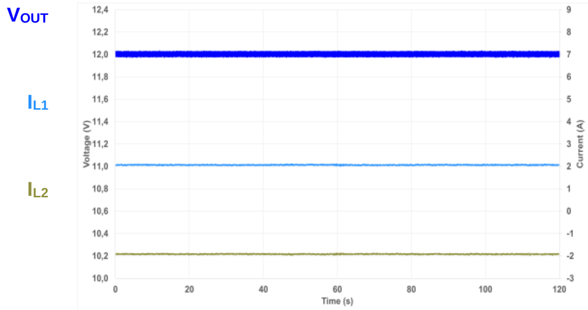


Figure 63: Phase Temperature

I_{OUT} = 0A, 2W slave heating, thermal balance

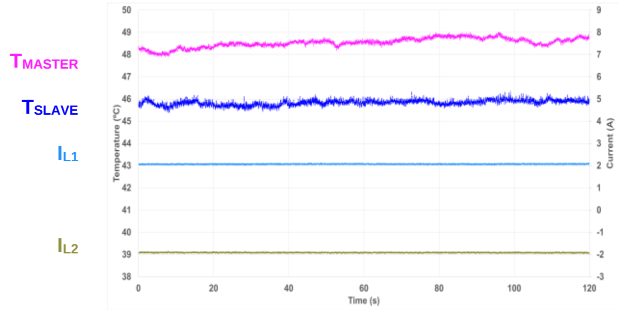


Figure 64: Output Voltage

I_{OUT} = 20A, no external heat, thermal balance

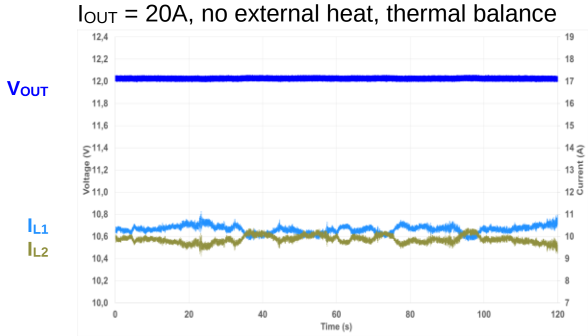


Figure 65: Phase Temperature

I_{OUT} = 20A, no external heat, thermal balance

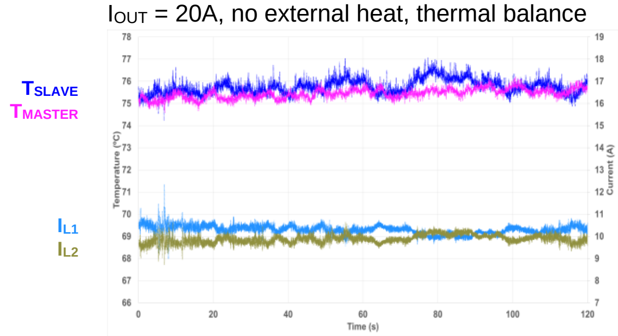


Figure 66: Output Voltage

I_{OUT} = 20A, 2W master heating, thermal balance

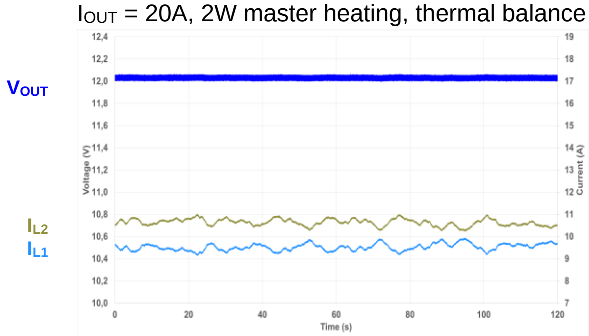
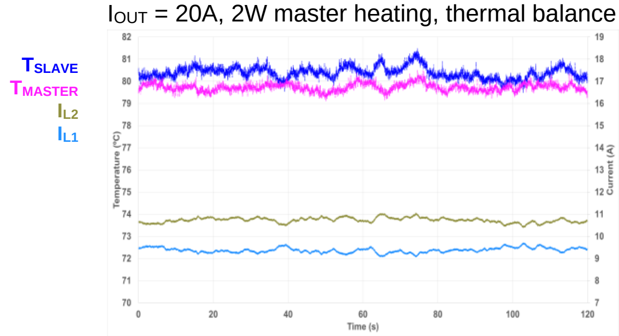


Figure 67: Phase Temperature

I_{OUT} = 20A, 2W master heating, thermal balance



n

Figure 68: Output Voltage

I_{OUT} = 20A, 2W slave heating, thermal balance

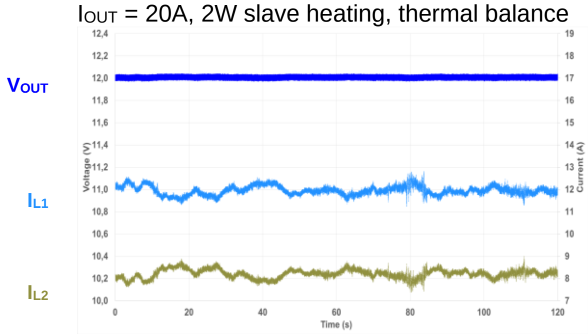
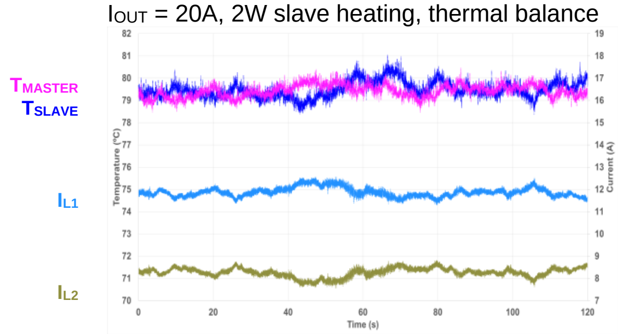


Figure 69: Phase Temperature

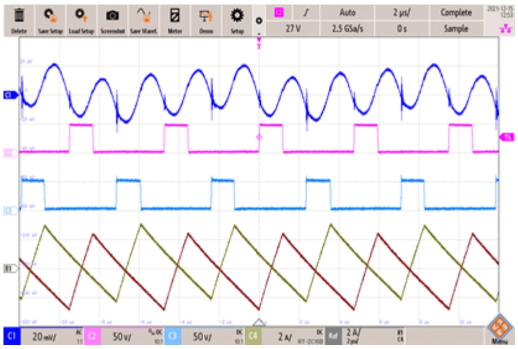
I_{OUT} = 20A, 2W slave heating, thermal balance



4.2 Thermal Balance Behavior Changes

Figure 70: Steady State
I_{OUT} = 0A, thermal balance

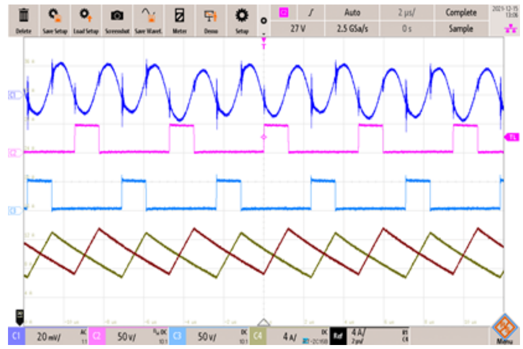
C1: V_{OUT}/AC 20mV/div.
C2: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R1: I_{L1} 2A/div.
C4: I_{L2} 2A/div.



2µs/div.

Figure 71: Steady State
I_{OUT} = 20A, thermal balance

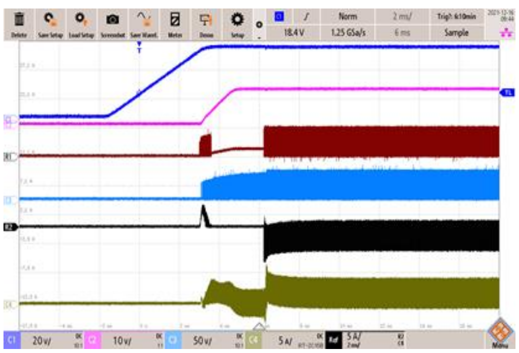
C1: V_{OUT}/AC 20mV/div.
C2: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R1: I_{L1} 4A/div.
C4: I_{L2} 4A/div.



2µs/div.

Figure 72: Start-Up Through VIN
I_{OUT} = 0A, thermal balance

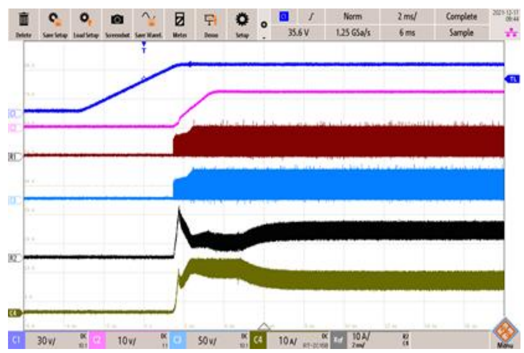
C1: V_{IN} 20V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 5A/div.
C4: I_{L2} 5A/div.



2ms/div.

Figure 73: Start-Up Through VIN
I_{OUT} = 20A, thermal balance

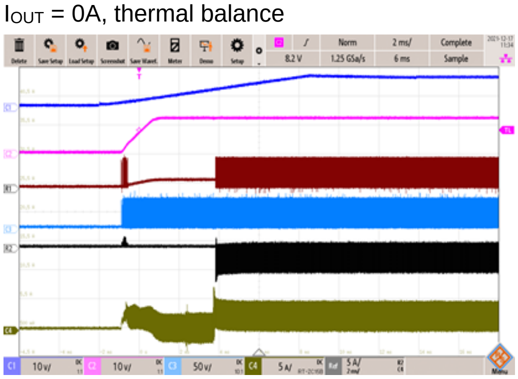
C1: V_{IN} 30V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.



2ms/div.

Figure 74: Start-Up Through EN/SYNC
I_{OUT} = 0A, thermal balance

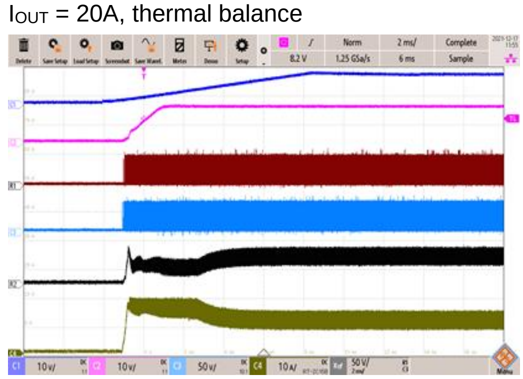
C1: V_{EN} 10V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 5A/div.
C4: I_{L2} 5A/div.



2ms/div.

Figure 75: Start-Up Through EN/SYNC
I_{OUT} = 20A, thermal balance

C1: V_{EN} 10V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.

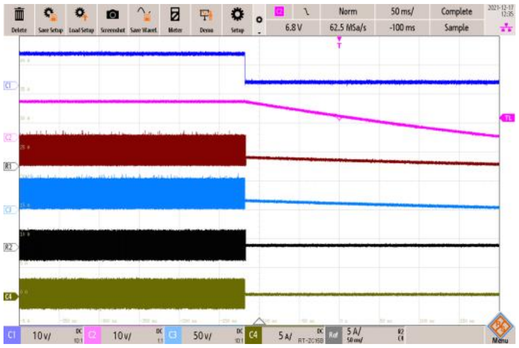


2ms/div.

Figure 76: Shutdown Through EN/SYNC

I_{OUT} = 10mA, thermal balance

C1: V_{EN} 10V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 5A/div.
C4: I_{L2} 5A/div.

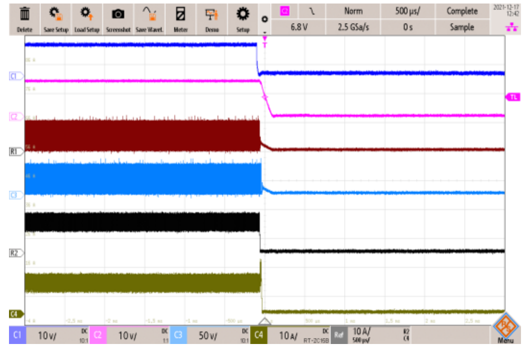


50ms/div.

Figure 77: Shutdown Through EN/SYNC

I_{OUT} = 20A, thermal balance

C1: V_{EN} 10V/div.
C2: V_{OUT} 10V/div.
R1: V_{SW1} 50V/div.
C3: V_{SW2} 50V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.

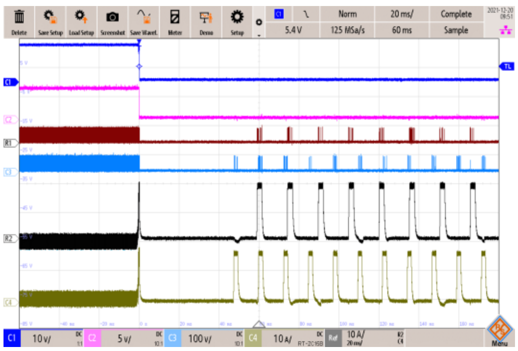


500μs/div.

Figure 78: SCP Entry

I_{OUT} = 0A, thermal balance

C1: V_{OUT} 10V/div.
C2: V_{PG} 5V/div.
R1: V_{SW1} 100V/div.
C3: V_{SW2} 100V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.

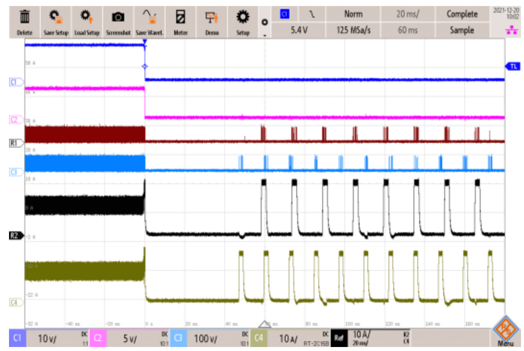


20ms/div.

Figure 79: SCP Entry

I_{OUT} = 20A, thermal balance

C1: V_{OUT} 10V/div.
C2: V_{PG} 5V/div.
R1: V_{SW1} 100V/div.
C3: V_{SW2} 100V/div.
R2: I_{L1} 10A/div.
C4: I_{L2} 10A/div.

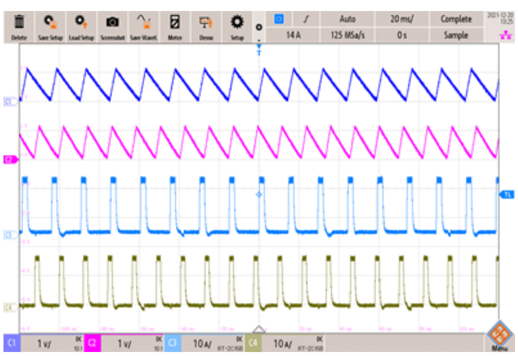


20ms/div.

Figure 80: SCP Steady State

Thermal balance

C1: V_{SS1} 1V/div.
C2: V_{SS2} 1V/div.
C3: I_{L1} 10A/div.
C4: I_{L2} 10A/div.

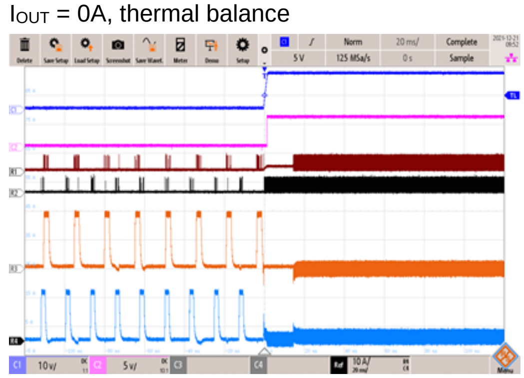


20ms/div.

Figure 81: SCP Recovery

I_{OUT} = 0A, thermal balance

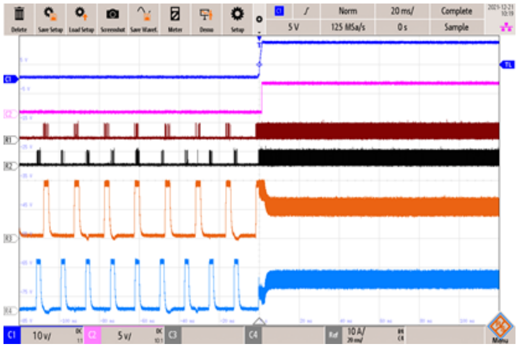
C1: V_{OUT} 10V/div.
C2: V_{PG} 5V/div.
R1: V_{SW1} 100V/div.
R2: V_{SW2} 100V/div.
R3: I_{L1} 10A/div.
R4: I_{L2} 10A/div.



20ms/div.

Figure 82: SCP Recovery
I_{OUT} = 20A, thermal balance

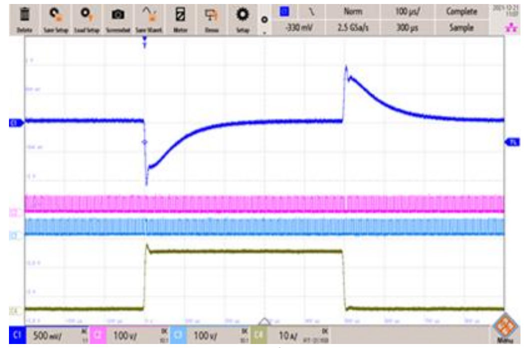
C1: V_{OUT} 10V/div.
C2: V_{PG} 5V/div.
R1: V_{SW1} 100V/div.
R2: V_{SW2} 100V/div.
R3: I_{L1} 10A/div.
R4: I_{L2} 10A/div.



20ms/div.

Figure 83: Load Transient Response
I_{OUT} = 0 to 20A, no thermal balance

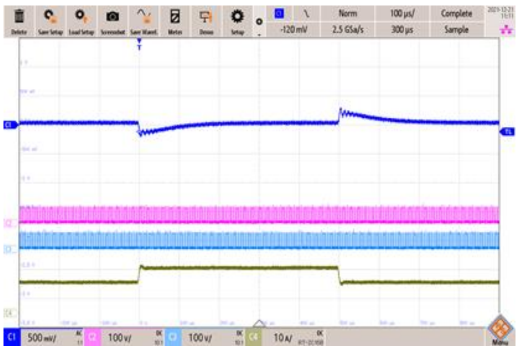
C1: V_{OUT}/AC 0.5V/div.
C2: V_{SW1} 100V/div.
C3: V_{SW2} 100V/div.
C4: I_{OUT} 10A/div.



100µs/div.

Figure 84: Load Transient Response
I_{OUT} = 10 to 15A, thermal balance

C1: V_{OUT}/AC 0.5V/div.
C2: V_{SW1} 100V/div.
C3: V_{SW2} 100V/div.
C4: I_{OUT} 10A/div.

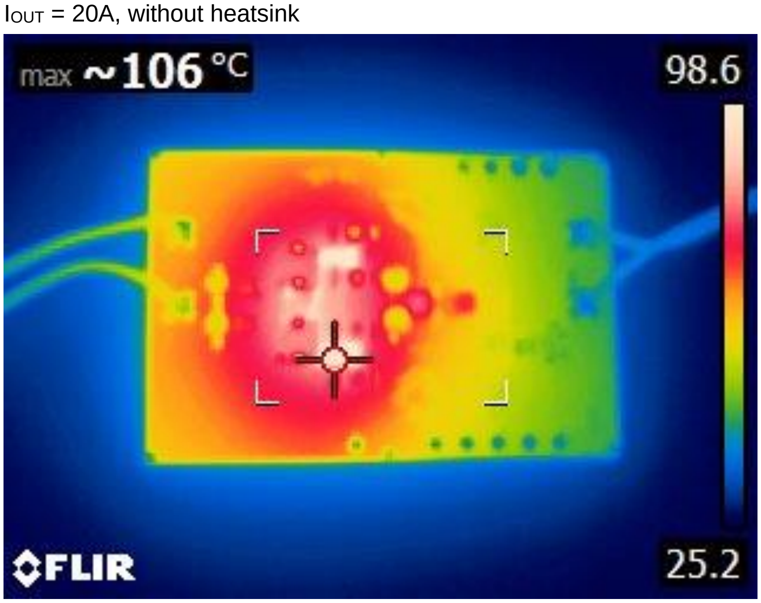


100µs/div.

4.3 Thermal Measurements

V_{IN} = 48V, V_{OUT} = 12V, L = 6.8µH, f_{SW} = 225kHz T_A = 26°C, CCM, no airflow.

Figure 85: Thermal Image
I_{OUT} = 20A, without heatsink



5 Start-Up

1. Connect the load terminals to:
   a. Positive (+): VOUT
   b. Negative (-): GND
2. Set the load current between 0A and 20A. Note that electronic loads represent a negative impedance to the regulator. If the current is set to high, it can trigger over-current protection (OCP) or short-circuit protection (SCP).
3. Preset the power supply output to be between 28V and 60V, and then turn the power supply off.
4. Connect the power supply terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND
5. Turn the power supply on. The board should automatically start up. The default output voltage (V_{OUT}) is 12V.
6. The external resistor divider (R53 and R54) sets V_{OUT} (see Figure 5 on page 7). To set V_{OUT} to 12V, R53 and R54 must be 169kΩ and 12kΩ, respectively. R53 and R54 can be calculated with Equation (4):

$$R54 = \frac{R53}{\frac{V_{OUT}}{0.8} - 1} \quad (4)$$

7. If the part is working at a high V_{IN} and f_{SW}, ensure that the junction temperature (T_J) of the high-side MOSFETs does not exceed 175°C.

6 Thermal Balance

Due to manufacturing tolerances, the behaviour of each MPQ2908A device is not the exact same, which can lead to unequal current sharing. To solve this issue, a system can be implemented to control each phase's temperature and adjust their currents so that the temperatures match. This leads to excellent current sharing when both phases have the same ambient temperature, and excellent thermal sharing when the ambient temperature of both phases is uneven.

To implement the thermal balancing system, modify the following components on the board:

- Remove R57 and replace it with 13kΩ, 0603, 1% resistor.
- Remove R74 and replace it with 0603 resistor, with a value between 270kΩ and 330kΩ depending on the operating conditions.
- Mount a 22kΩ, 0603, 1% resistor on R75.
- Mount a 4.7nF, 0603 capacitor (with a voltage rating of at least 6.3V) on C60.
- Mount a 22pF 0603 capacitor (with a voltage rating of at least 6.3V) on C61.
- Mount a 0Ω, 0603 resistor on R33.

To disable the thermal balancing system, revert these components to their original values.

7 Frequency Spread Spectrum (FSS)

Most switching mode power supplies (SMPSs) generate a significant amount of noise when working from 48V systems. This board has an optional frequency spread spectrum (FSS) modulation feature that can be used to improve the system's EMC performance when the system fails to comply with EMC regulations by a few dB.

FSS consists in making the DC/DC switching power converter commute on several side bands around its fundamental f_{SW}, instead of having just one fixed frequency. These side bands are created by modulating f_{SW} with a triangle modulation waveform. The emission power of the fundamental switching frequency and its harmonics are distributed into smaller pieces; thus, the peak EMI noise is reduced significantly.

FSS is especially effective in reducing the noise levels of lower frequencies, and its effectiveness decreases as the measurement frequency increases.

MPS has conducted an in-depth webinar on FSS, explaining how it works, and what improvements can be expected from it. This webinar can be found on the MPS website.

To enable FSS, a few components must be changed on the board. The modifications are listed below:

- Mount a 0Ω, 0603 resistor on R25.
- Mount a 10kΩ, 0603 resistor on R27.
- Mount a 330nF, 0603 capacitor (with a voltage rating of at least 6.3V) on C39.
- Remove R49 and substitute it with a 1kΩ, 0603 resistor.

8 Disclaimer

Monolithic Power Systems (MPS) reserves the right to make changes to its products and to discontinue products without notice. The applications information, schematic diagrams, and other reference information included herein is provided as a design aid only and are therefore provided as-is. MPS makes no warranties with respect to this information and disclaims any implied warranties of merchantability or non-infringement of third-party intellectual property rights.

MPS cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in an MPS product. No circuit patent licenses are implied.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

MPS PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE SUPPORT APPLICATIONS, DEVICES OR SYSTEMS, OR OTHER CRITICAL APPLICATIONS.

Inclusion of MPS products in critical applications is understood to be fully at the risk of the customer.

Questions concerning potential risk applications should be directed to MPS.

MPS semiconductors are typically used in power supplies in which high voltages are present during operation. High-voltage safety precautions should be observed in design and operation to minimize the chance of injury.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/5/2022	Initial Release	-