DC/DC Converter
EMC Trouble-shooting

March 2022

Agenda

- General Guidelines for DC/DC EMC Troubleshooting
- Optimization Examples with MPS DC/DC Evaluation Boards
- Conclusion

Step of Troubleshooting

➢ Test background understanding

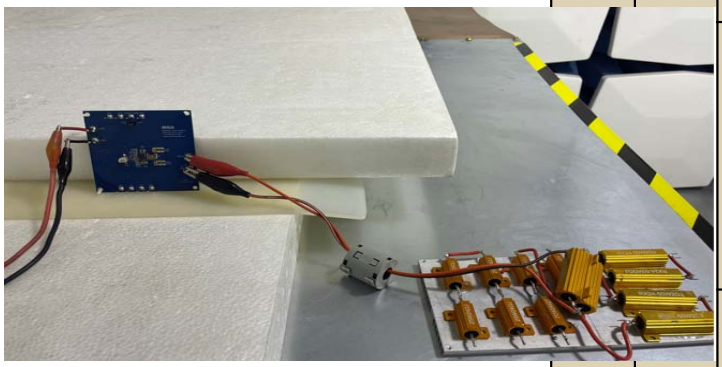
- **Which EMC tests are failed by DUT?** CE? RE? Or Immunity?
- **What's the test standard and limit?** CISPR? Or Customer specific (TL81000)?
- **How does the test spec & set-up look like?**

  Input and output voltage? Load?

  Input and output cable length?

  Voltage method CE or current method CE?

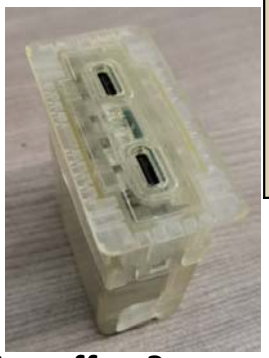
  Antenna type and placement, 1m or 3m?



- **How does DUT look like?**

  Load size, on board or out of board with long cable connection?

  Housing: metal or plastic? Heatsink? X/Y/Z placement?



- **At what frequency does the DUT exceed the limits?**

  Any regularity on failed frequency?

- **Any modification/optimization done before and corresponding effect?**

	EMI	CE	电源线时域传导发射
			电源线频域传导发射
		RE	辐射发射-天线接收法
			辐射发射-TEM小室法
			辐射抗扰度-TEM小室法
			扰度-带状线法
			度-磁场环照射法
			放电实验

Step of Troubleshooting

➢ DUT information review

- **Schematic review**

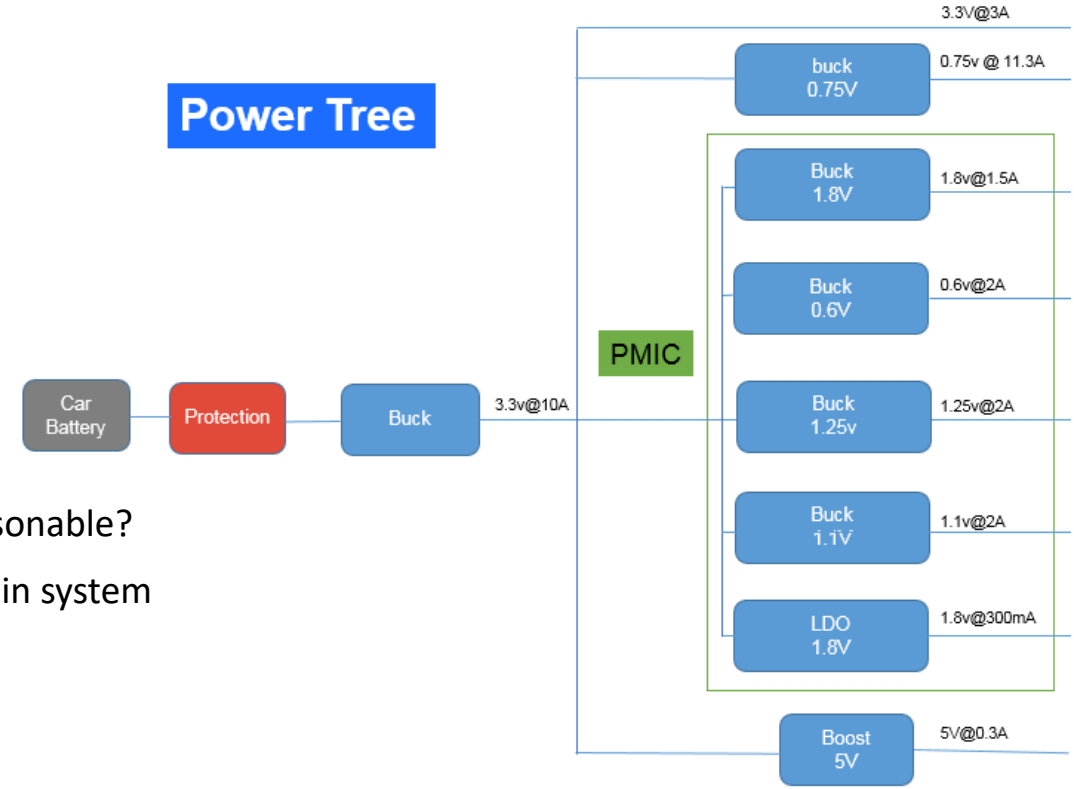
  How many DC/DC converters placed in the system?

  Which topo for each DC/DC?

  What's the switching frequency for each DC/DC?

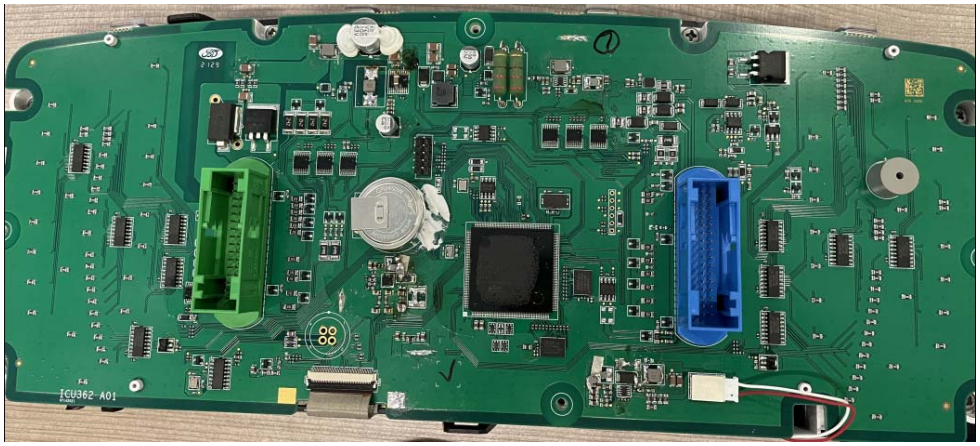
  If schematic and components value correct and reasonable?

  Check all input and output filters or common choke in system



Step of Troubleshooting

➢ DUT information review



- **Schematic review**

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  Which topo for each DC/DC?

  What's the switching frequency for each DC/DC?

  If schematic and components value correct and reasonable?

  Check all input and output filters or common chock in system

- **Layout and board review**

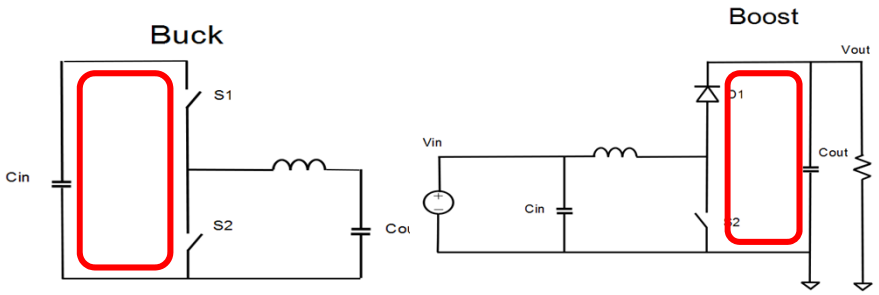
  Where are the DC/DC converters placed in the system?

  Identify and mark all high dV/dt and dI/dt circuit nodes

  EMI filter placement

  GND placement

  Inductor type and size



Step of Troubleshooting

➢ Issue identification

- **Quick EMI shot on DUT with default status**

If can duplicate same of similar problem/ failure frequency?

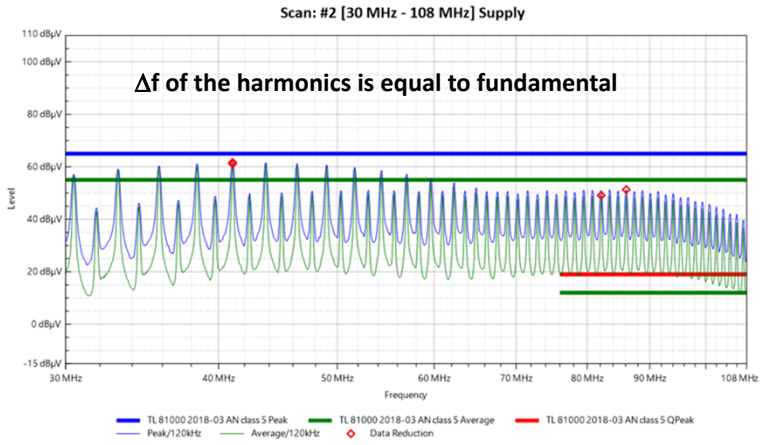
Probe SW, Vout and other test point to confirm all circuit works normally

Measure the clock of each DC/DC, create a table with fundamental, harmonics

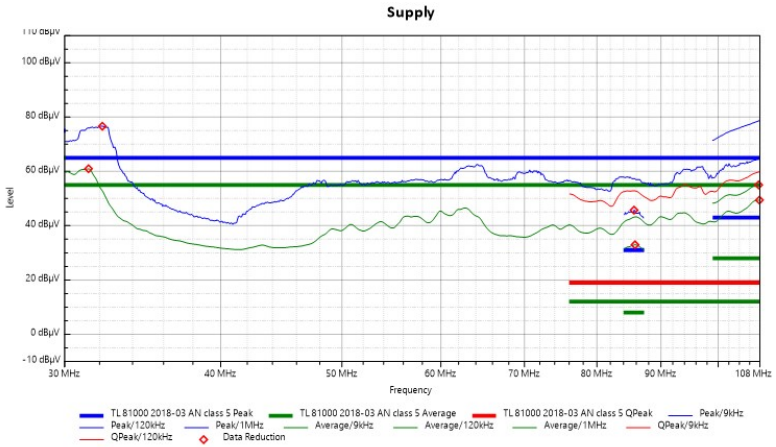
If failure frequency related with clock of any DC/DC? Failure by DM or CM noise?

	f1 [MHz]	f2 [MHz]	f3 [MHz]
Fsw	0.489	1.93	20.03
2x	0.978	3.86	40.06
3x	1.467	5.79	60.09
4x	1.956	7.72	80.12
5x	2.445	9.65	100.15
6x	2.934	11.58	120.18

Sometimes the source is obvious with discrete frequency lines



But sometimes as "mountains"



Step of Troubleshooting

➢ Issue identification

- **Identify issue place on DUT**

Change large and complex connecters to simple wire connection

Change load to small size and short cable

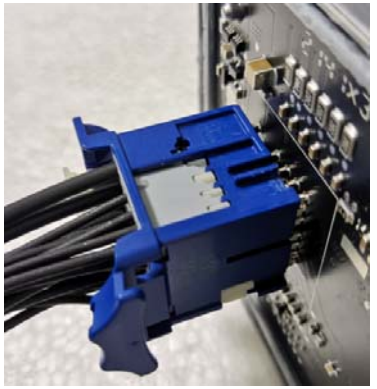
Remove heatsink or housing if any

Use snap-on ferrites on cables, and try to distinguish CM and DM noise

Disable each DC/DC converter one by one

Add small shielding on each DC/DC converter or small circuit area one by one

Use field probe to find detailed issue device and place



Step of Troubleshooting

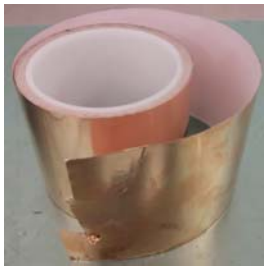
➢ EMI performance optimization

- Add or increase input/output EMI filters
- Add small capacitance cap close to connectors
- Change switching frequency if allowable
- Change / decrease high frequency noise loop area
- Change inductor with smaller size one
- Adjust inductor, input/output caps placement
- Add BST resistor or snubber
- Adjust heatsink or housing connection to DUT GND
- Do cut on PCB
- Add common chokes if allowable
- Add shielding if allowable

Tool Set for Troubleshooting

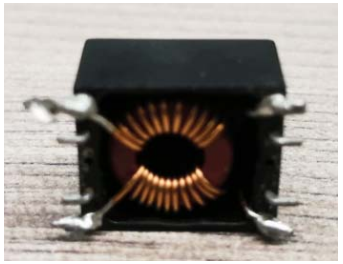
- LC filter

- Small size inductor



- Cu-Foil / Shielding

- Snap-On Ferrite/ Common Choke

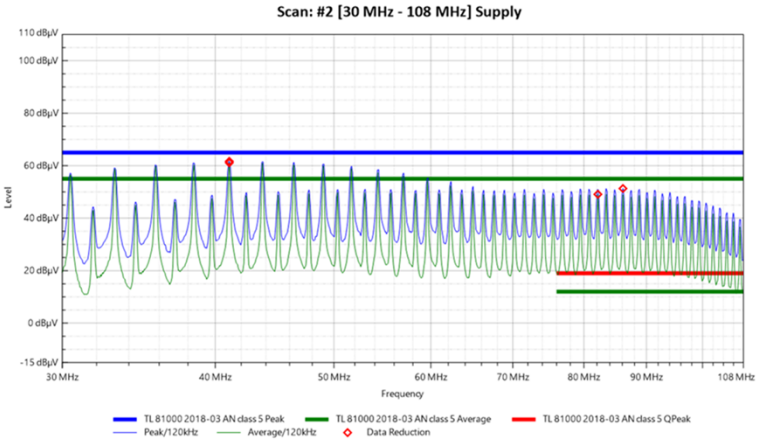


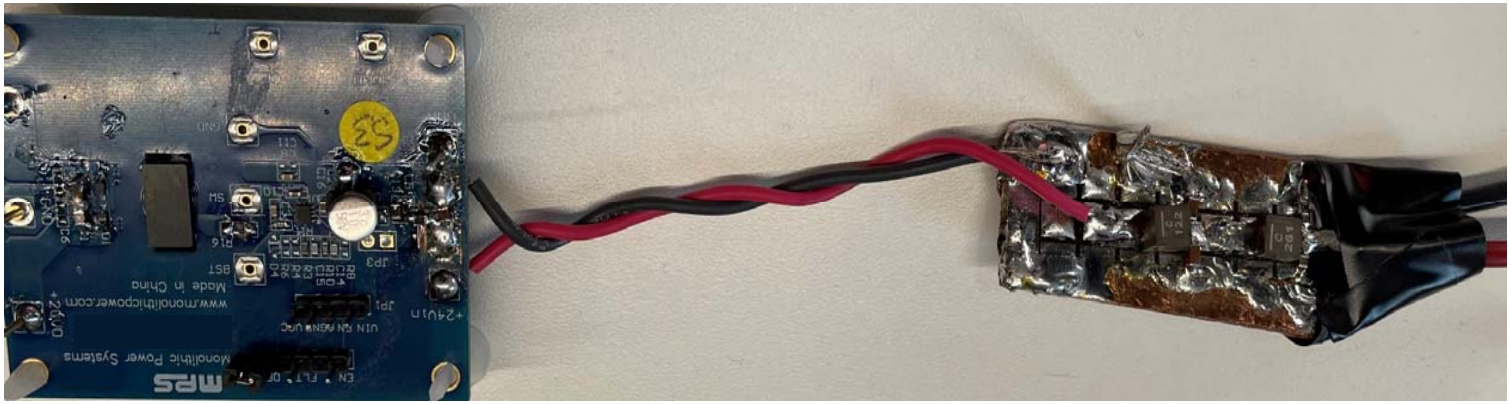
- Field Probes

Choose appropriate input filter

LC filter debug step

- Increase the input filter capacitors by 2x
- Increase the input filter coil by 2x
- Use two-stage filter
- What is the distance between the buck C_{IN} and the filter?
- Is an off-board filter effective?

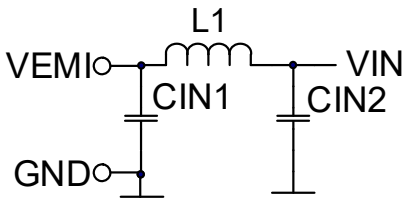




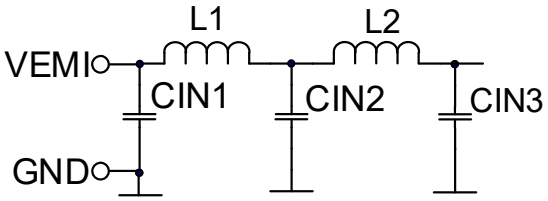
Choose appropriate input filter

Single-Stage vs. Two-Stage

Single-Stage



Two-Stage



Input EMC Filter Calculation

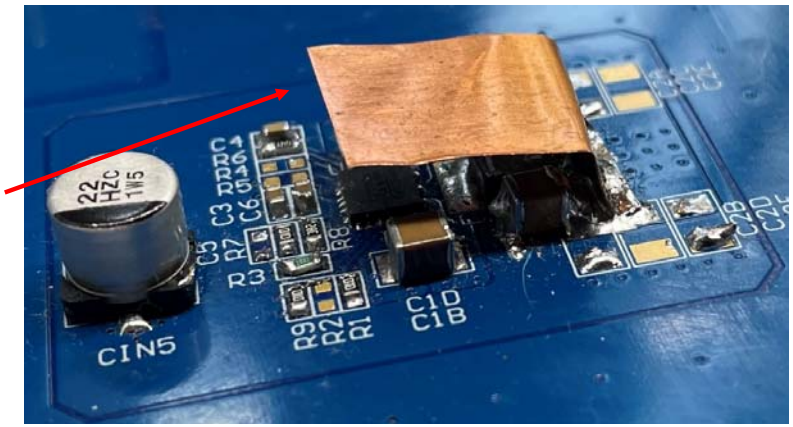
=Enter your parameter

Single-Stage	Fundamental		1st Harm	2nd Harm	3rd Harm	4th Harm	5th Harm
f_{sw}:	2.2	MHz	4.40	6.60	8.80	11.00	13.20
Omega f_{sw}	13.82	1/µs	27.65	41.47	55.29	69.11	82.94
L_single:	0.33	µH					
XL:	4.56	Ω	9.12	13.68	18.25	22.81	27.37
C-effective:	0.70	µF					
XC:	0.10	Ω	0.052	0.034	0.026	0.021	0.017
Damping	**-33.09**	**dB**	**-44.99**	**-52.00**	**-56.99**	**-60.86**	**-64.03**
Two-Stage Filter Design:							
1st L:	0.10	µH					
XL:	1.38	Ω	2.76	4.15	5.53	6.91	8.29
1st C:	0.60	µF					
XC:	0.121	Ω	0.060	0.040	0.030	0.024	0.020
Damping 1	-21.91	dB	-33.42	-40.36	-45.32	-49.18	-52.33
2nd L:	0.10	µH					
XL:	1.38	Ω	2.76	4.15	5.53	6.91	8.29
2nd C:	0.40	µF					
XC:	0.181	Ω	0.090	0.060	0.045	0.036	0.030
Damping 2:	-18.73	dB	-29.99	-36.88	-41.82	-45.67	-48.82
Total Damping:	**-40.65**	**dB**	**-63.40**	**-77.23**	**-87.13**	**-94.84**	**-101.16**

Simplified calculation: 20 log (Xc / (Xc + XL)) at f_{sw}, 2 x f_{sw}, etc.

Use Cu-Foil shielding

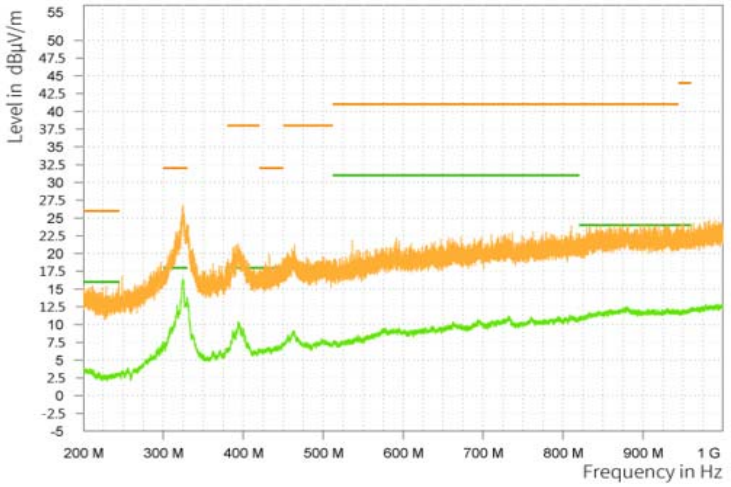
Start with the DC/DC converter and coil…



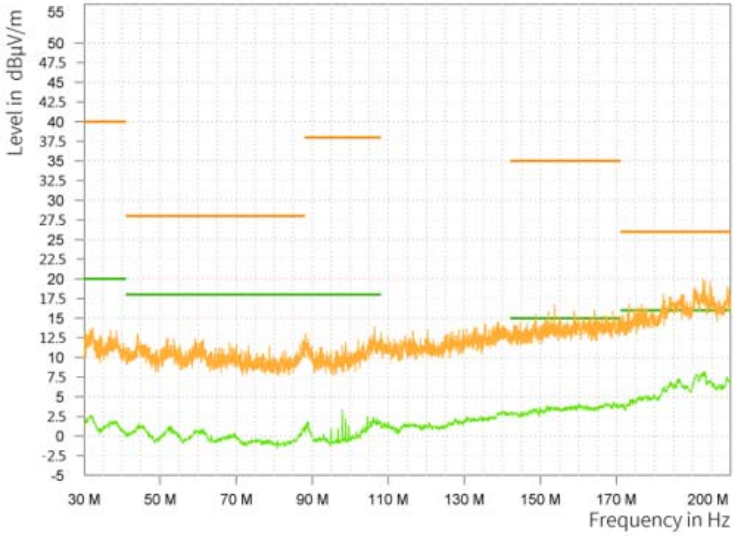
…. to part of the PCB.

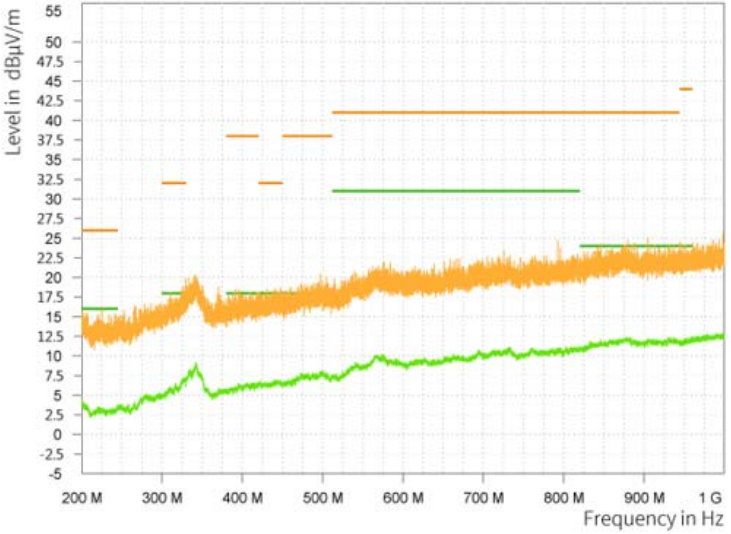
Use snap-on ferrite / common choke

w/o common choke



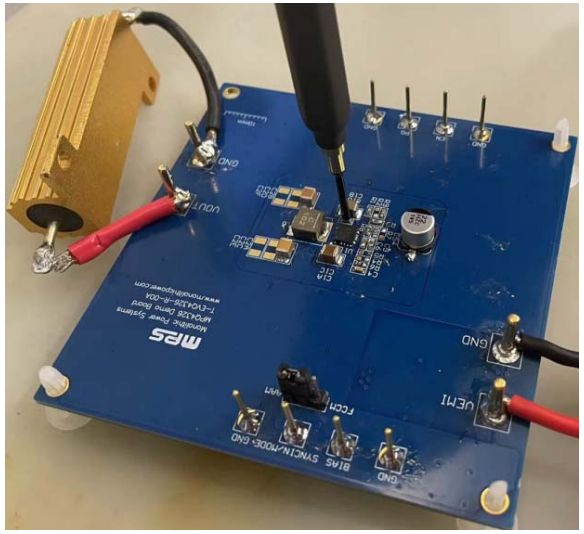
w/ common choke

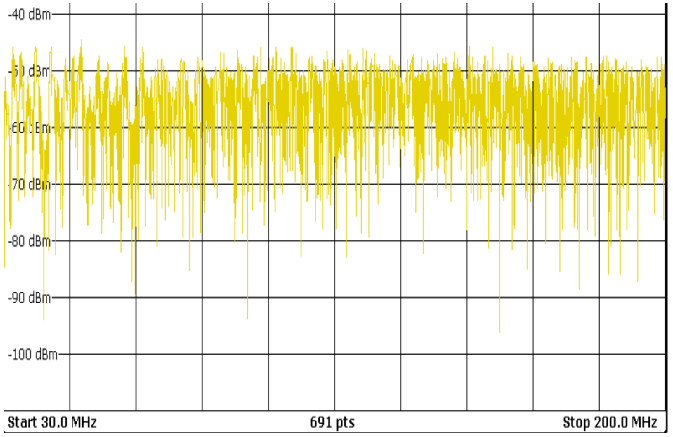




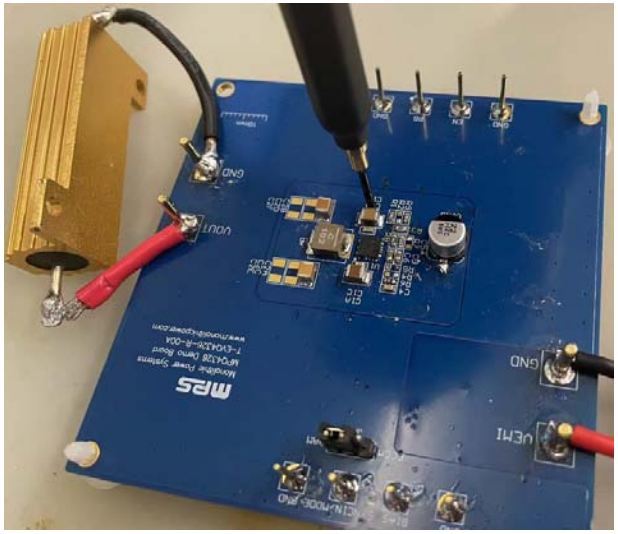
Use field probes

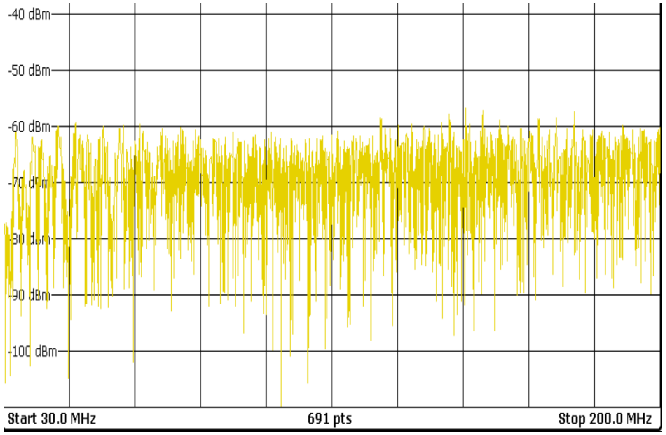
Small CIN



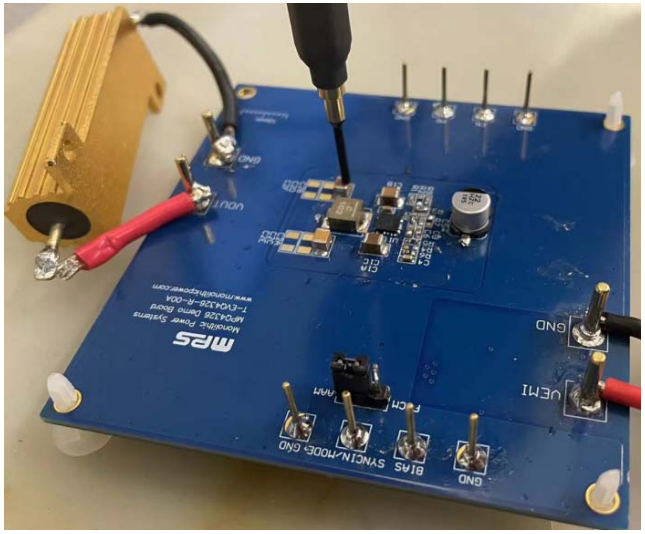


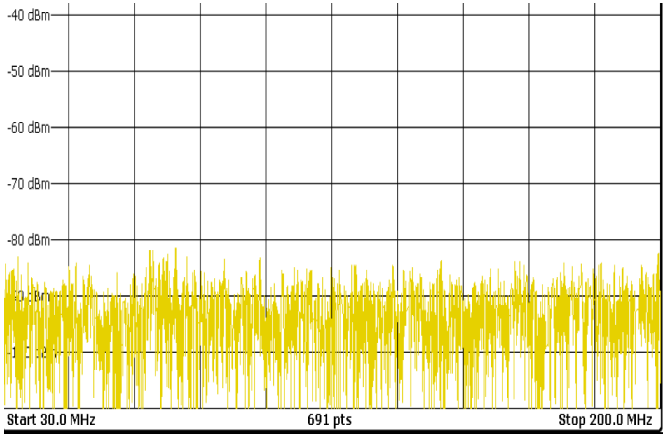
Large CIN





Cout





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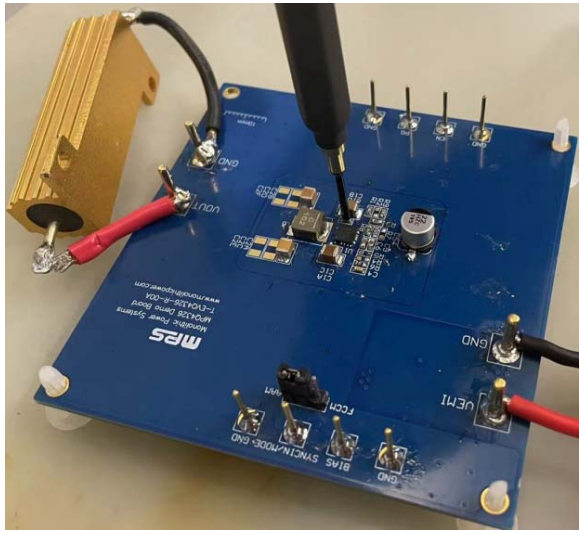

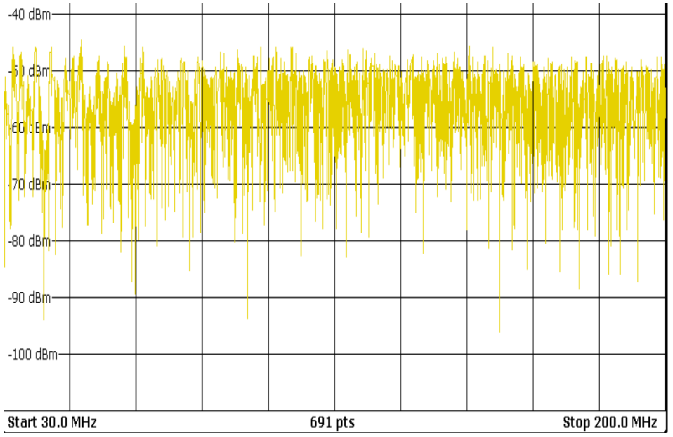

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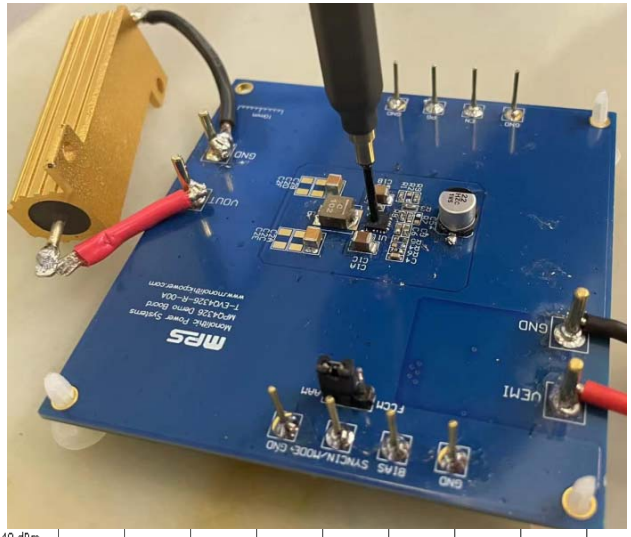
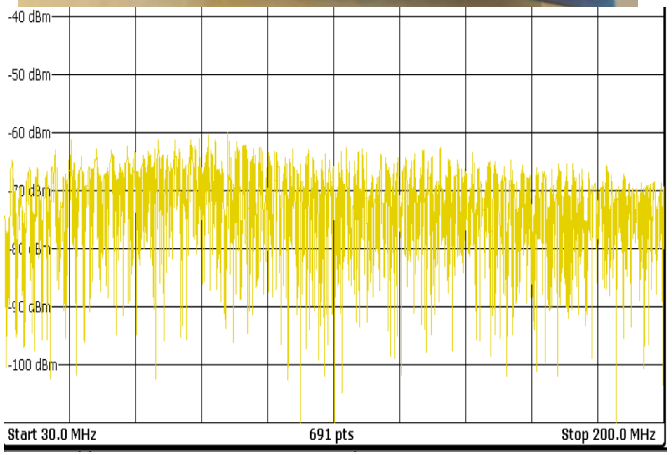
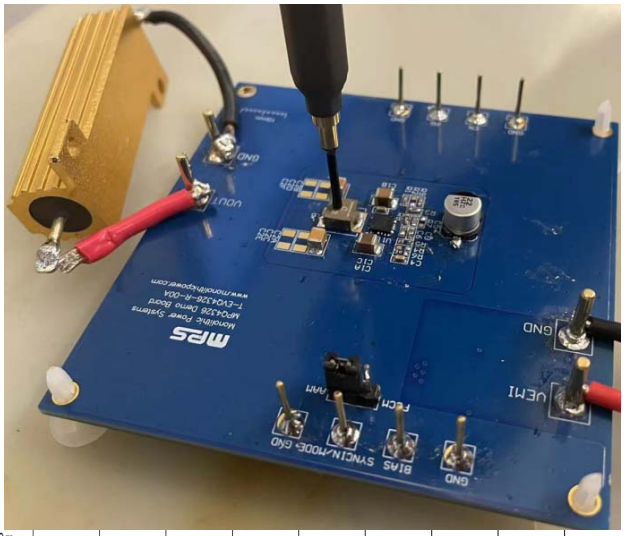
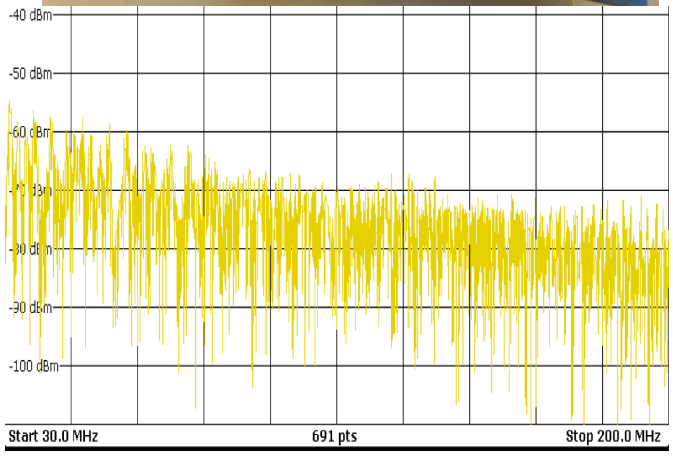


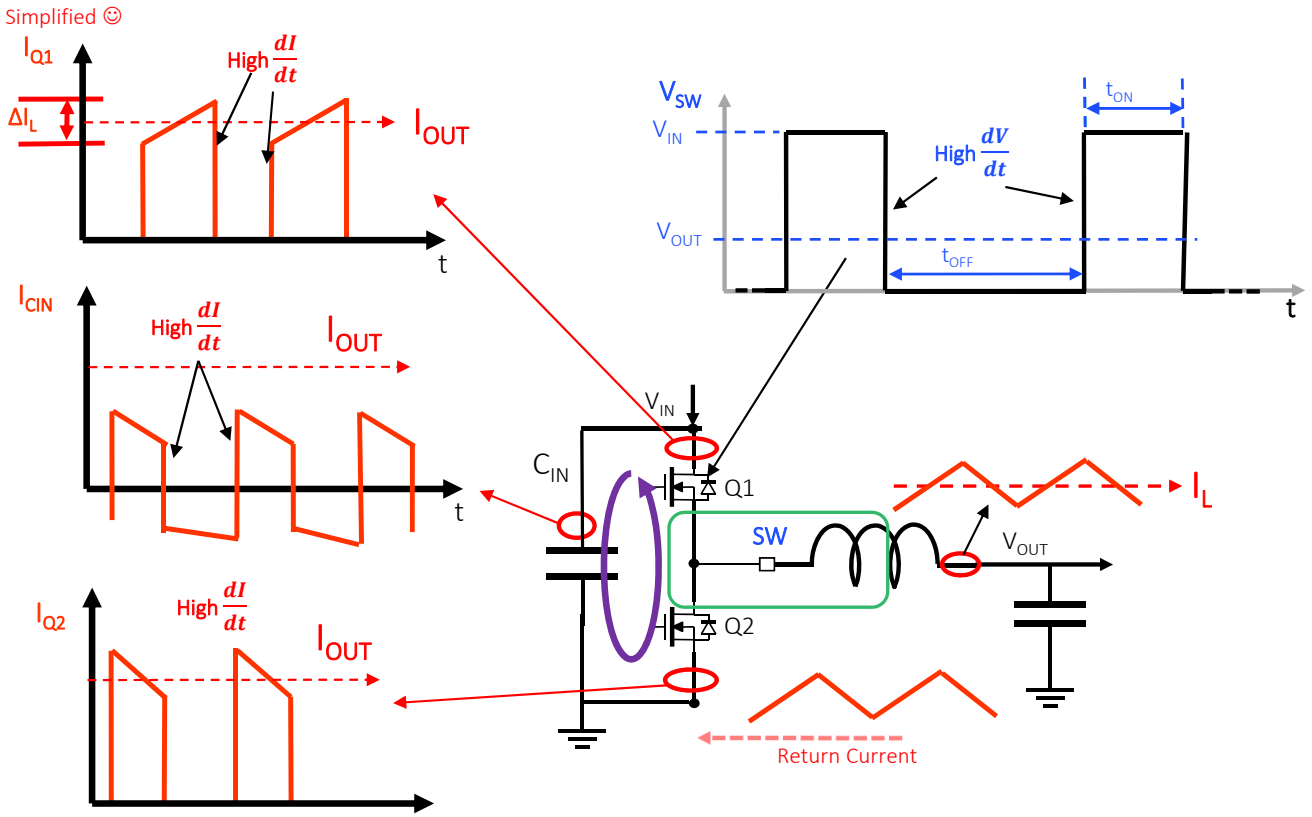


Inductor





Refresh: Buck Converter Voltage & Current Waveforms



High $\frac{dV}{dt} \Rightarrow \boldsymbol{E - Field}$

Increases with voltage

Increases with SW area size

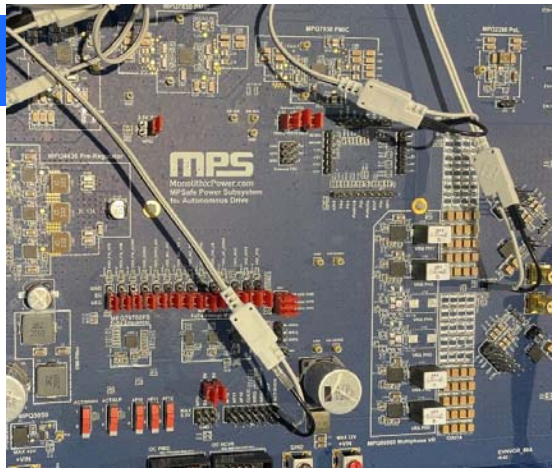
High $\frac{dI}{dt} \Rightarrow \boldsymbol{H - Field}$

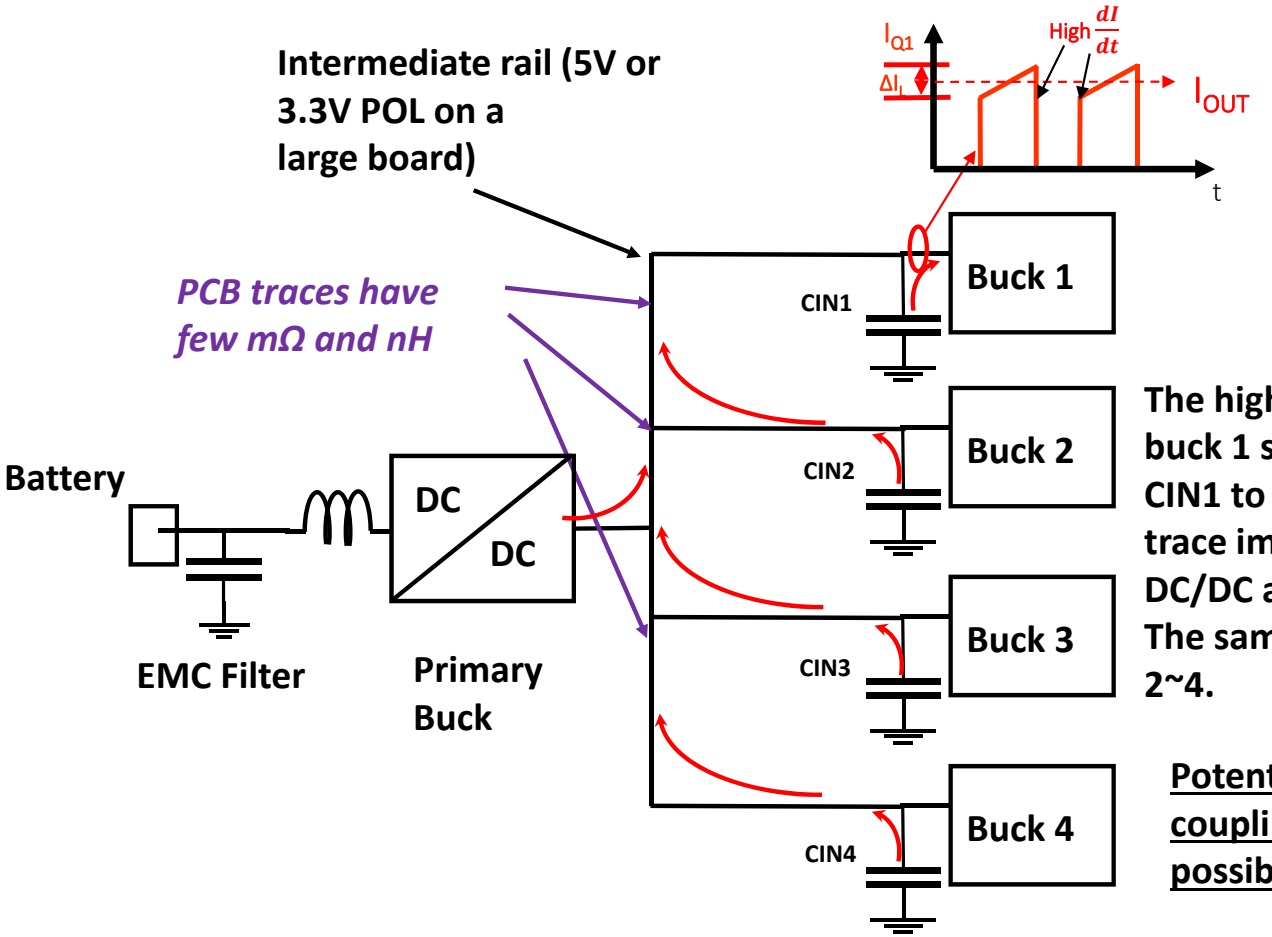
Increases with current

Increases with loop size

A boost converter is just a mirror image.

Several DC/DC Converters on One Large Board

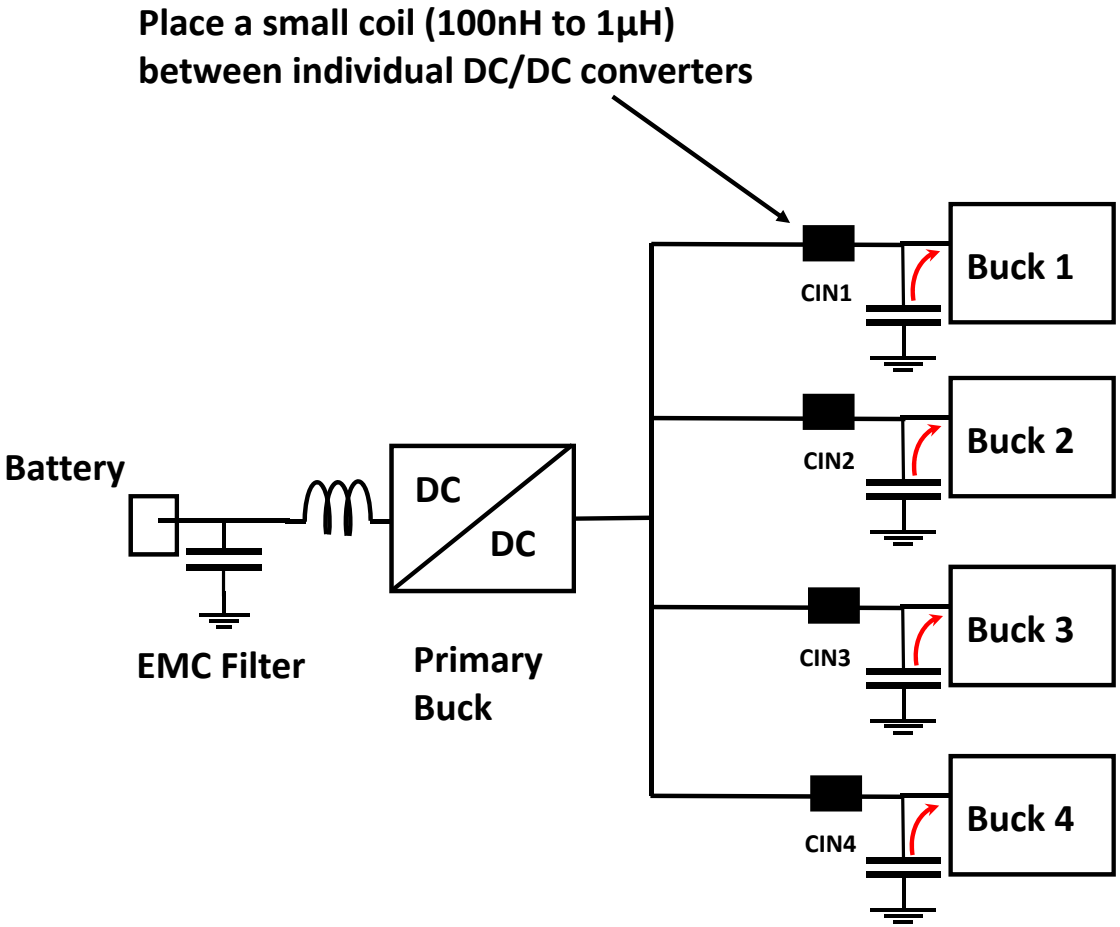




The high dI/dt input current of buck 1 splits to CIN1 to CIN4, according to the trace impedance between DC/DC and CINx. The same applies for bucks 2~4.

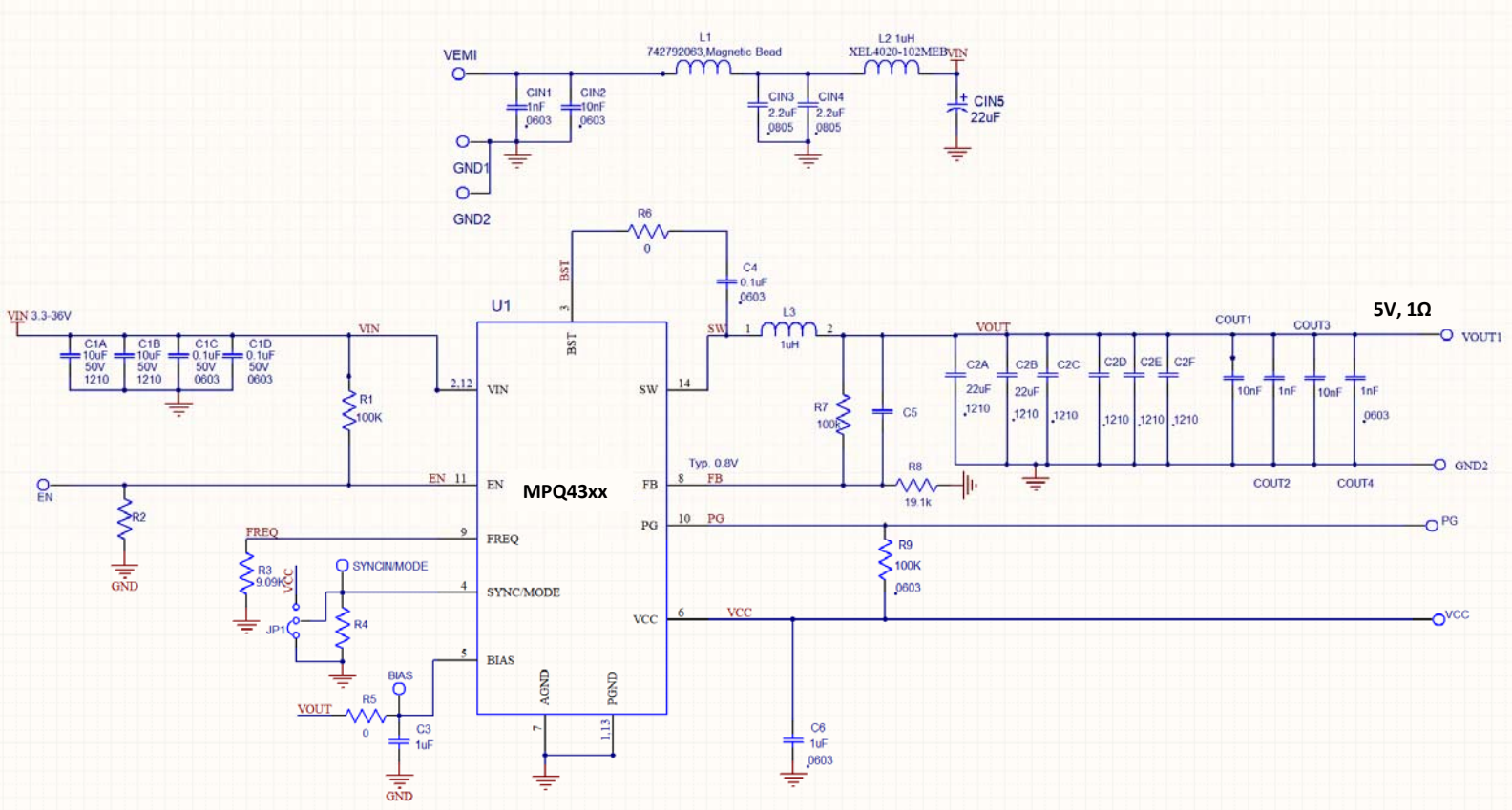
<u>Potential radiation and coupling in other circuits is possible!</u>

Several DC/DC Bucks on One Large Power Rail



This configuration forces the high dI/dt of each buck to flow in its local CIN!

Optimization Example #1: 5A Buck F_{SW} = 2MHz with SSFM



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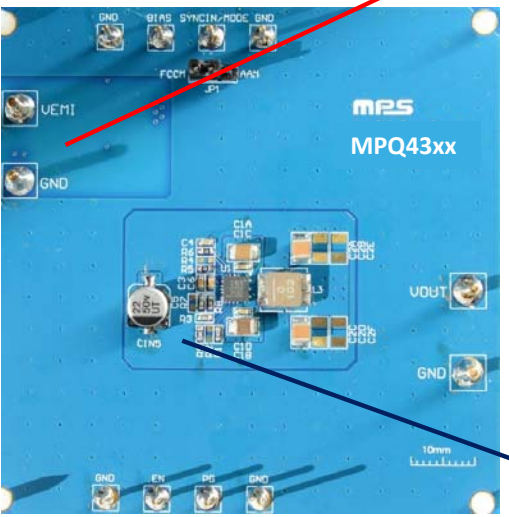
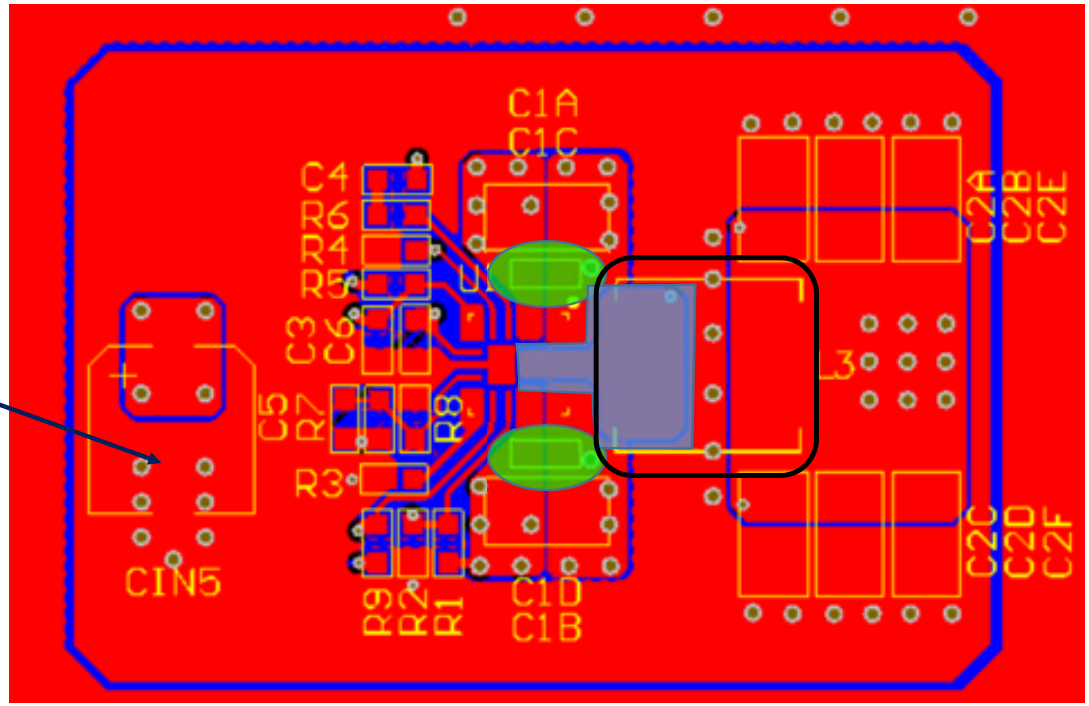


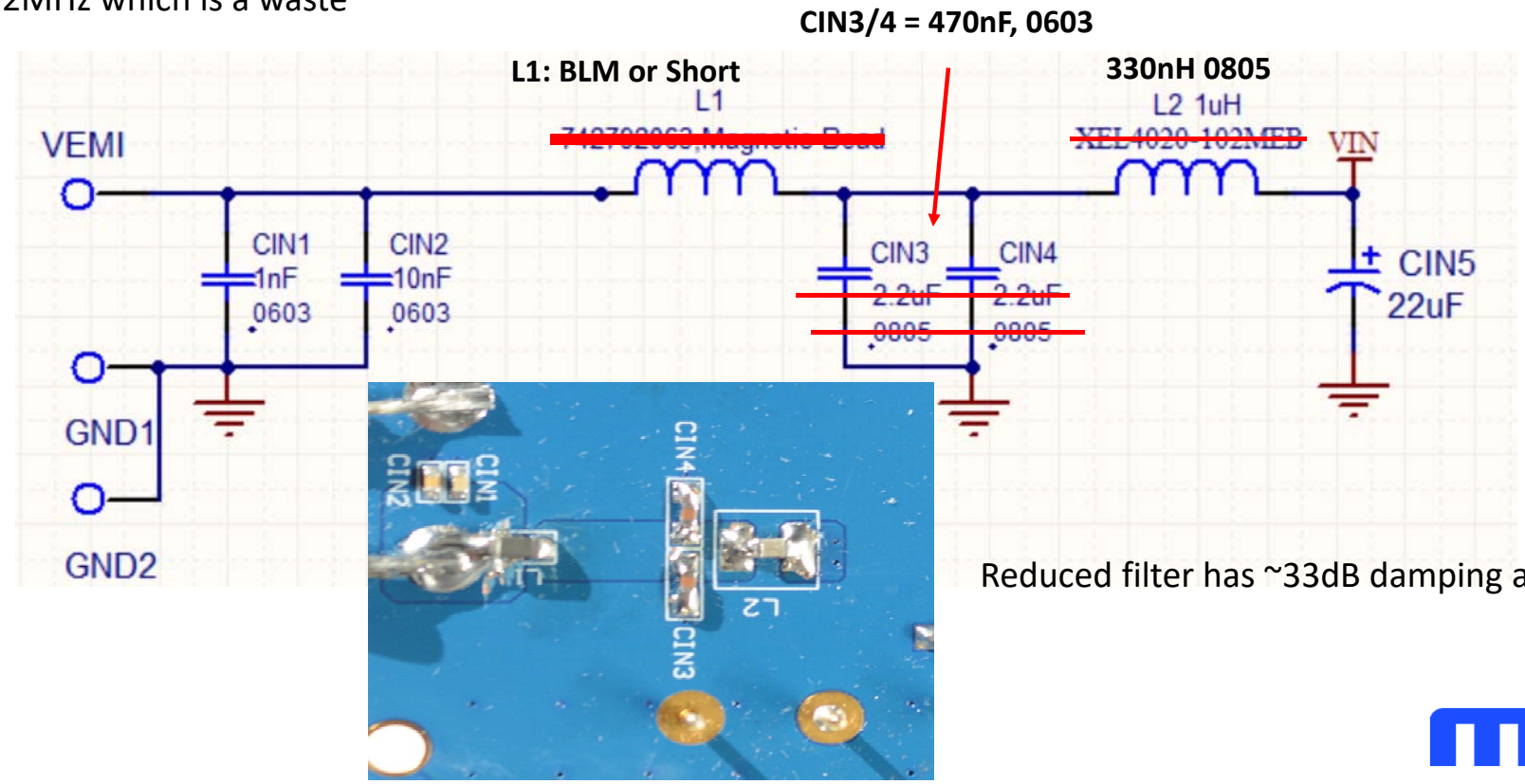
- Input Filter Placed on the Bottom Side
- Small size Cin placed close to VIN and PGND pin for small hot loop
- Symmetric input cap placement
- Small SW copper and small size inductor



Optimization Example #1: 5A Buck F_{SW} = 2MHz with SSFM

Reduce Input Filter

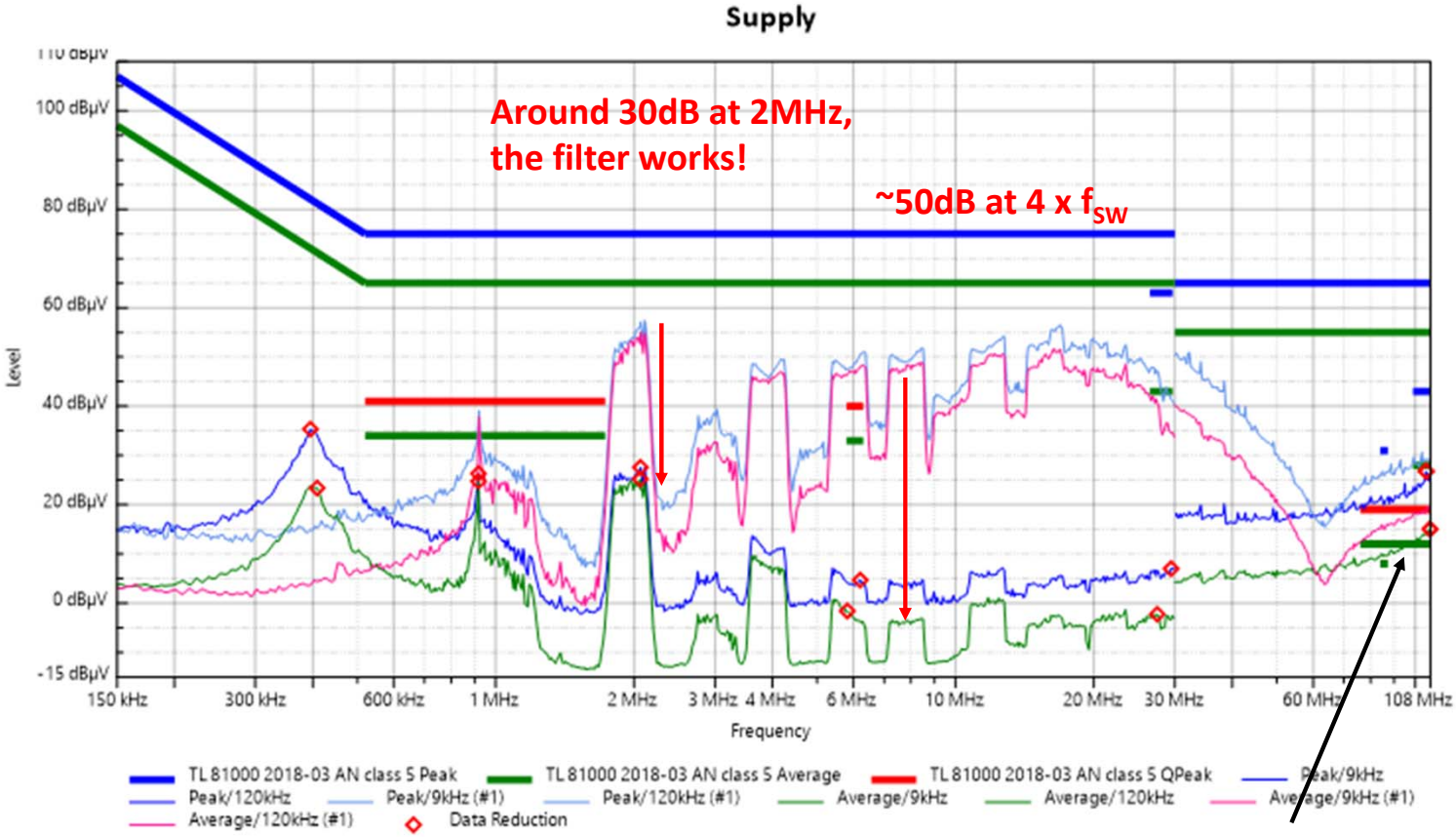
The initial input filter has about 50dB damping at 2MHz which is a waste



Reduced filter has ~33dB damping at 2MHz

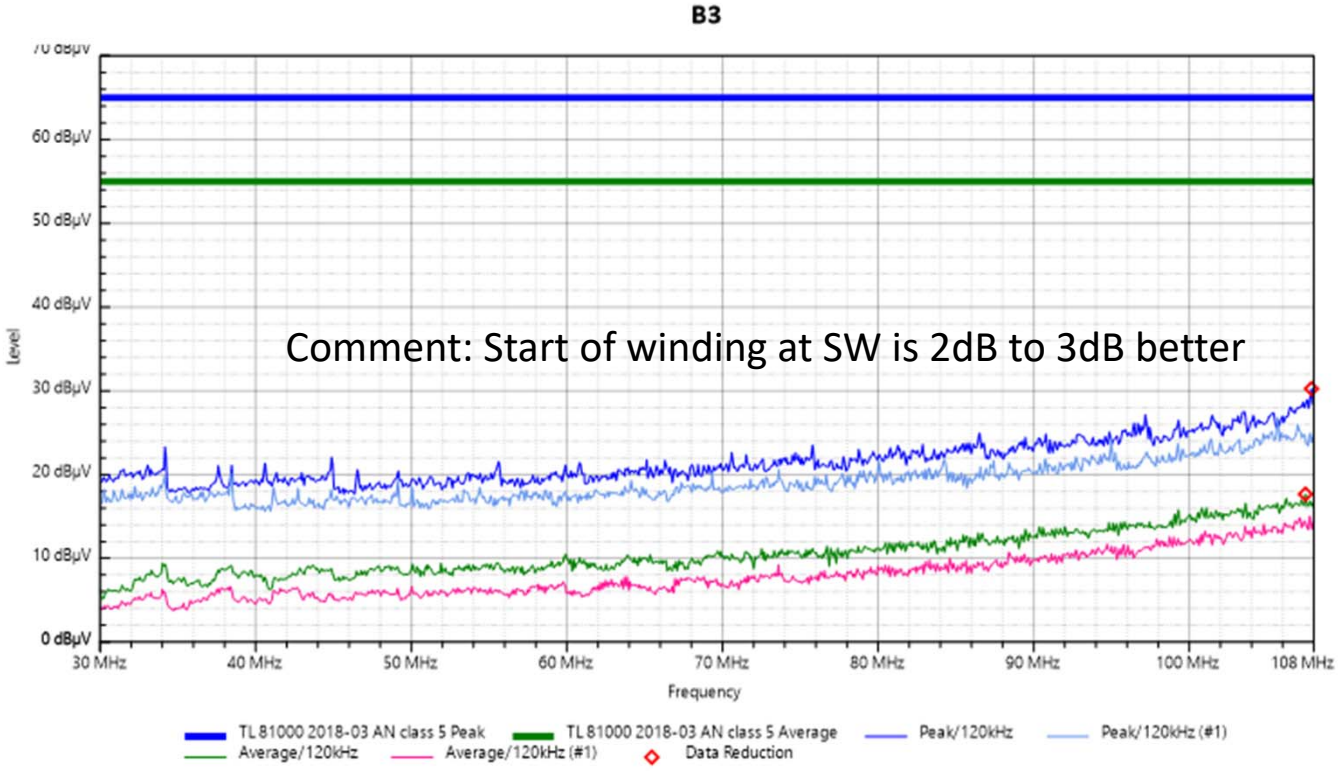
Optimization Example #1: 5A Buck F_{SW} = 2MHz with SSFM

CE Test w/o & w/ Reduced Input Filter

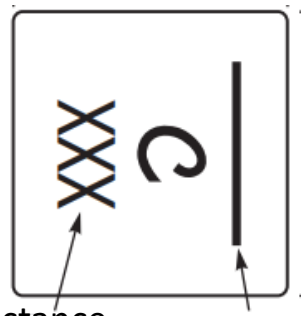


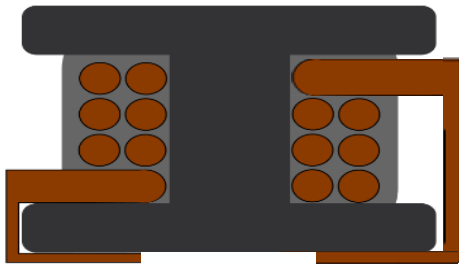
Optimization Example #1: 5A Buck F_{sw} = 2MHz with SSFM

Comparison between inductor with different directions



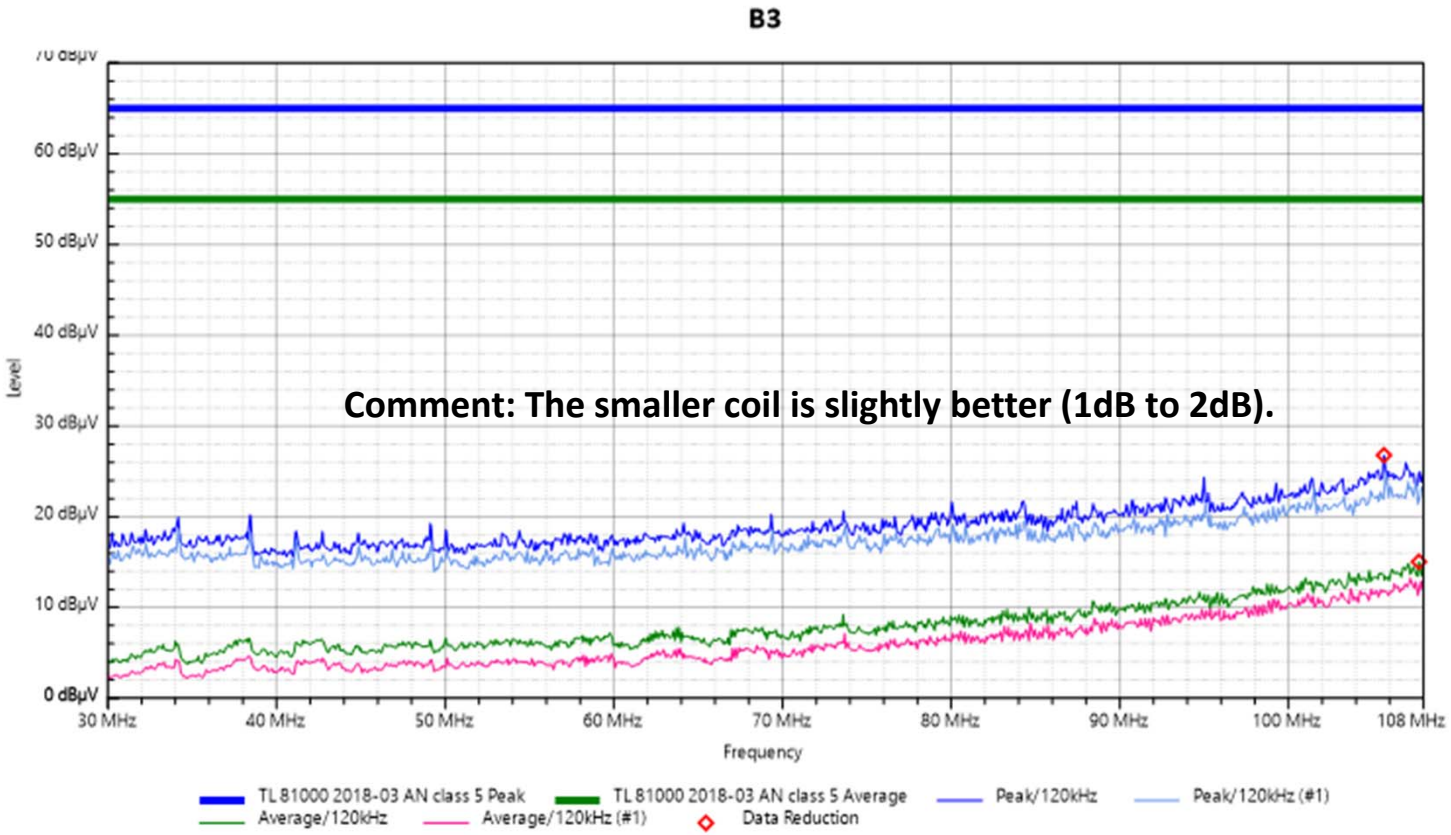
Comment: Start of winding at SW is 2dB to 3dB better





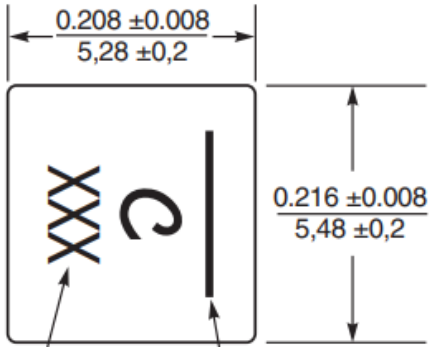
Optimization Example #1: 5A Buck F_{SW} = 2MHz with SSFM

Replace XAL5030-1µH by XAL4020-1µH

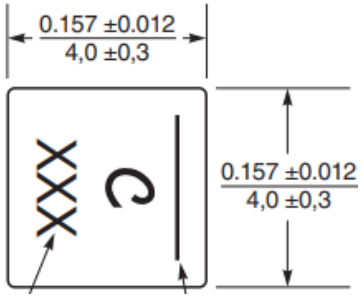


Comment: The smaller coil is slightly better (1dB to 2dB).

XAL5030

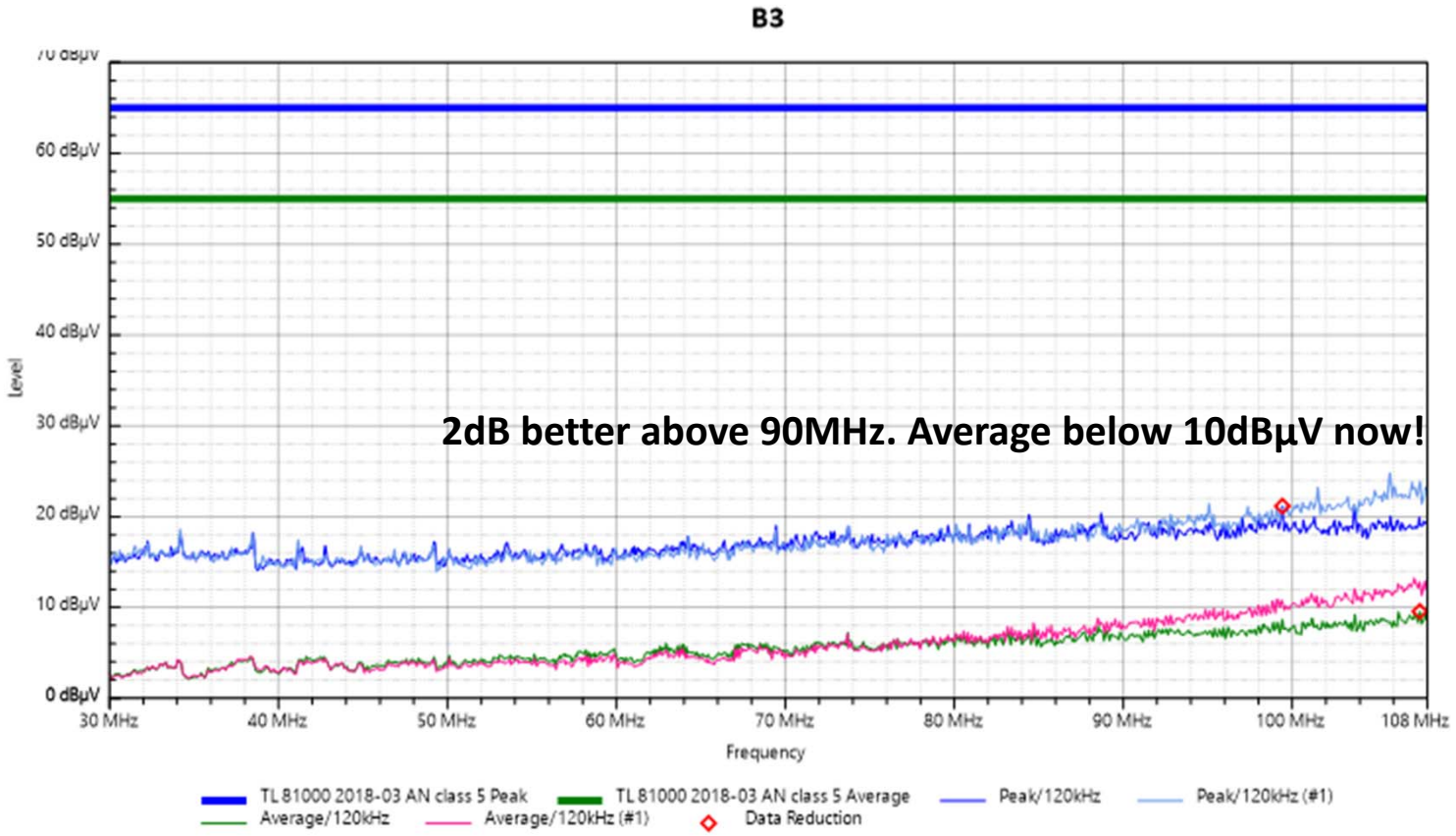


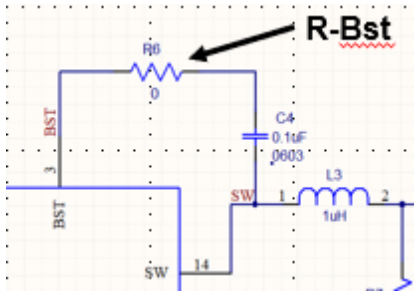
XAL4020



Optimization Example #1: 5A Buck F_{SW} = 2MHz with SSFM

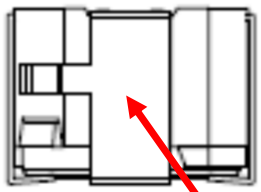
Add 4.7Ω Into BST Circuit

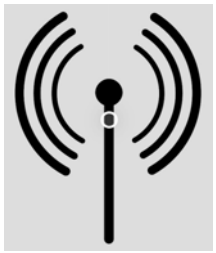




Optimization Example #2: More about Inductor & EMC

4.5mm Height

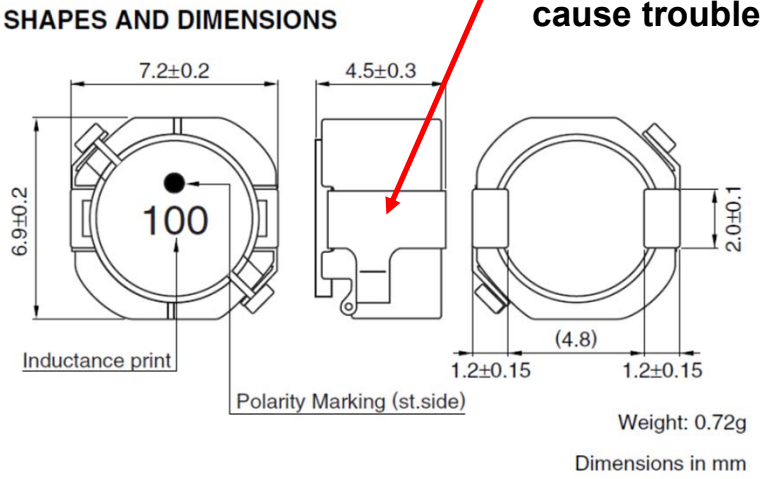




Contact metal acts as an antenna for the E-field from the SW node dV/dt

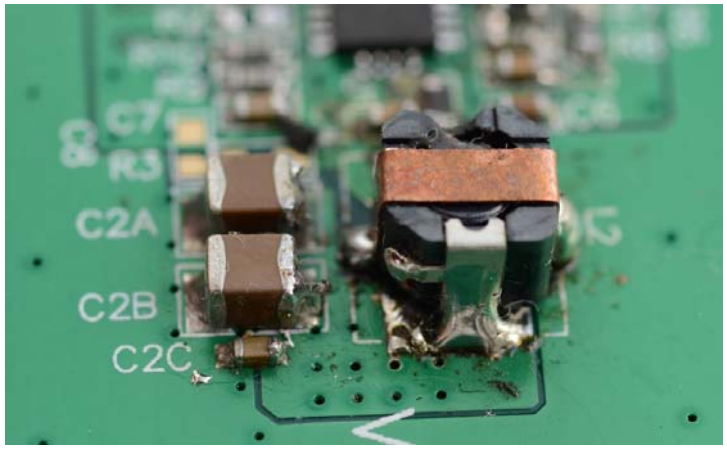
End-of-winding side contact metal with two clips into airgap for mechanical robustness

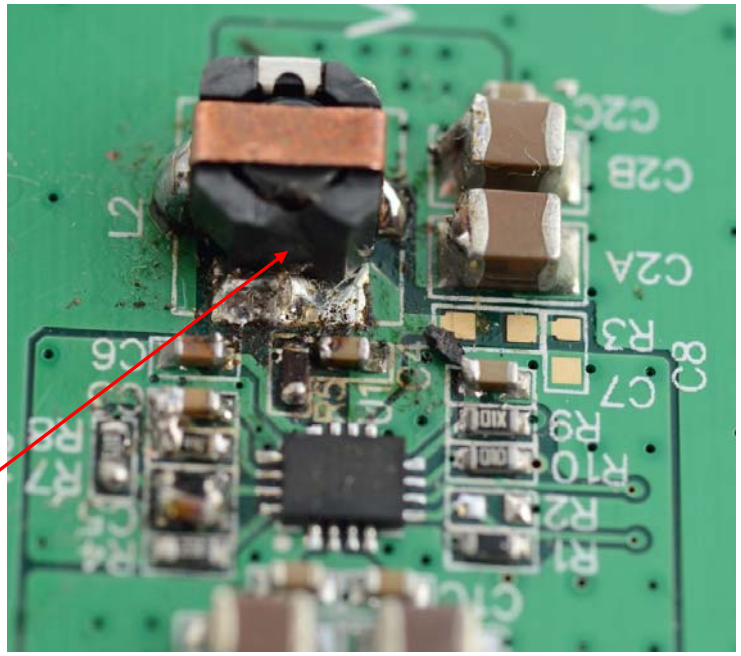
Even if the SoW is at SW, the plate will cause trouble



Example Drawings from Murata, TDK and ABC

Optimization Example #2: More about Inductor & EMC



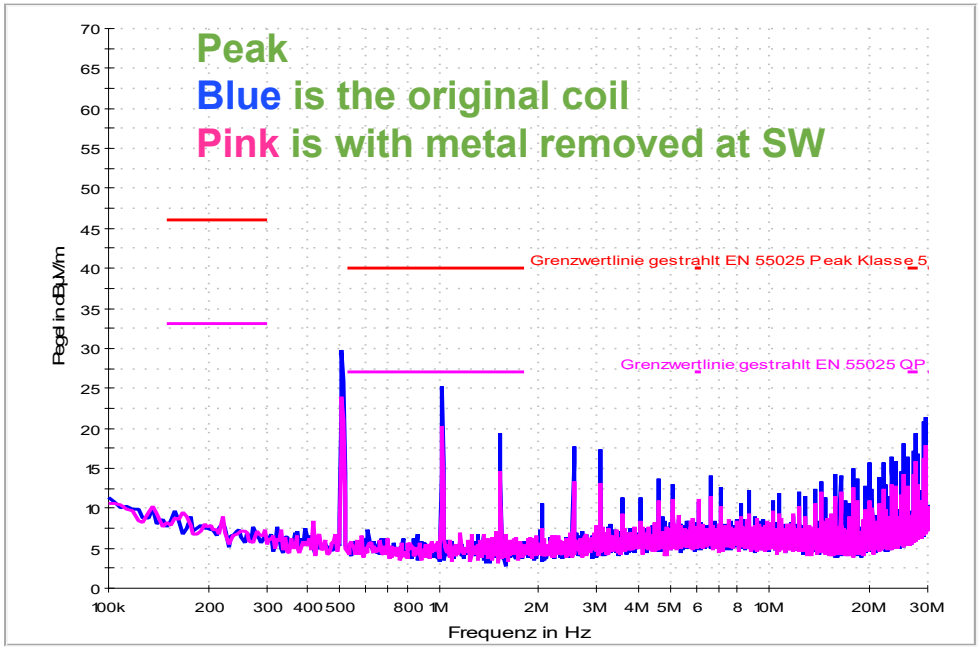


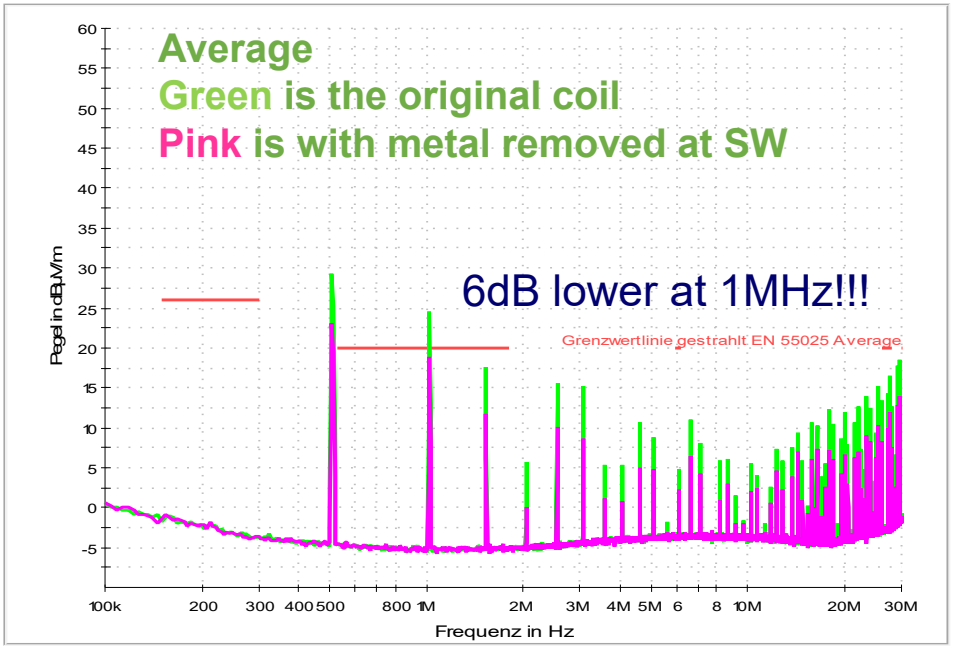
The SW node contact plate has been removed, and the winding is soldered directly to the PCB.
6dB lower emissions at 1MHz in monopole antenna testing

A 4.5mm height contact plate acts as an E-field antenna for the SW node's high dV/dt. The optimum coil should have an SW contact at the bottom.

Optimization Example #2: More about Inductor & EMC

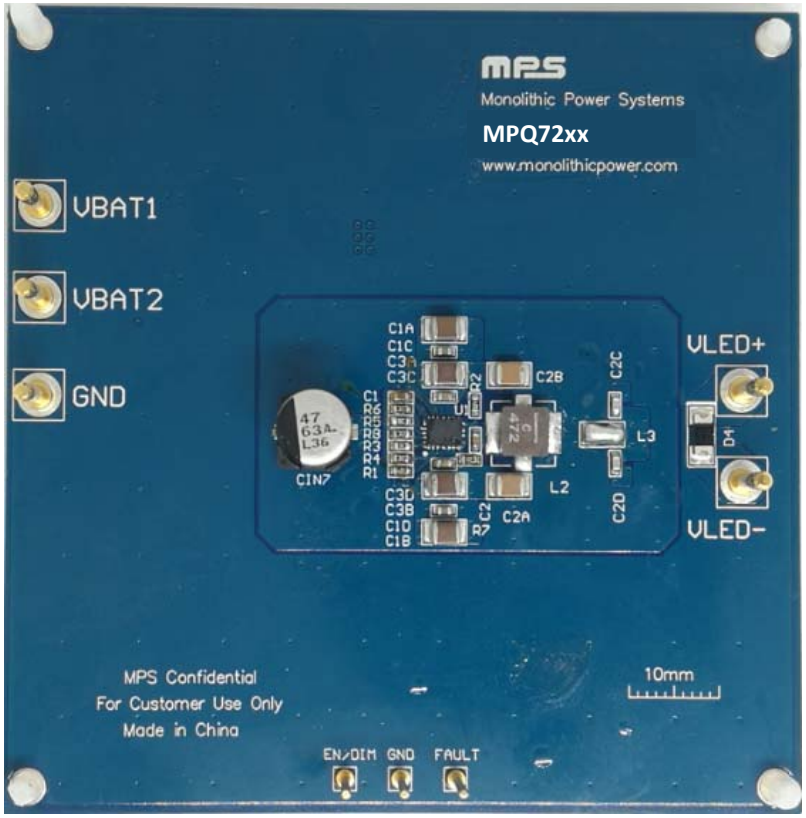
RE Monopole Test 0.1MHz to 30MHz

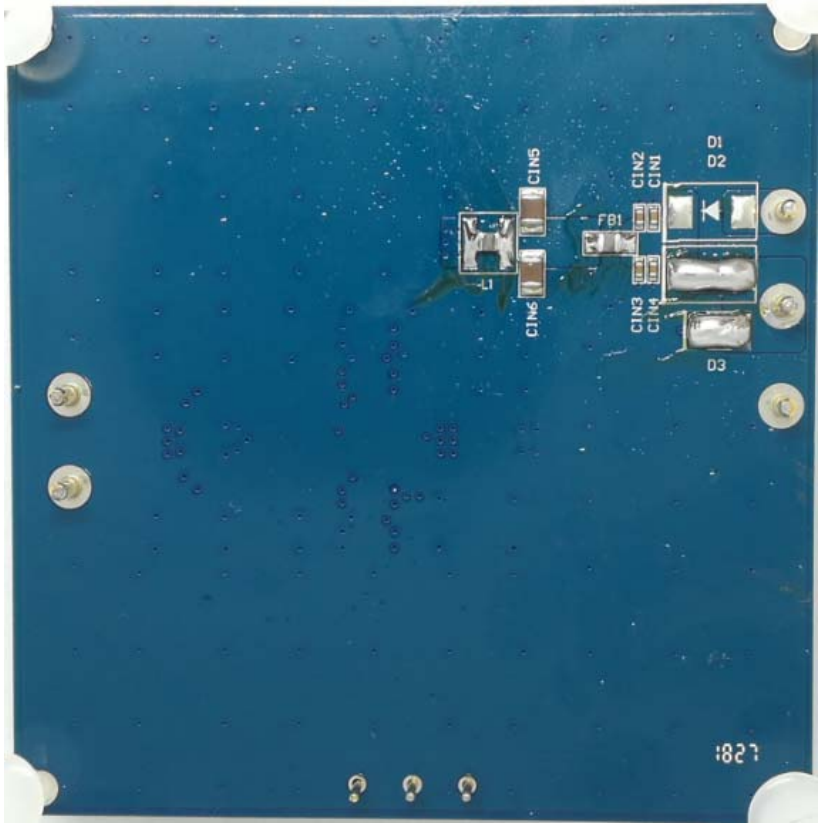




Case #3: 1.2A LED Driver, Buckboost, F_{SW} = 1MHz with SSFM

Initial / default board figure, already quite good on layout



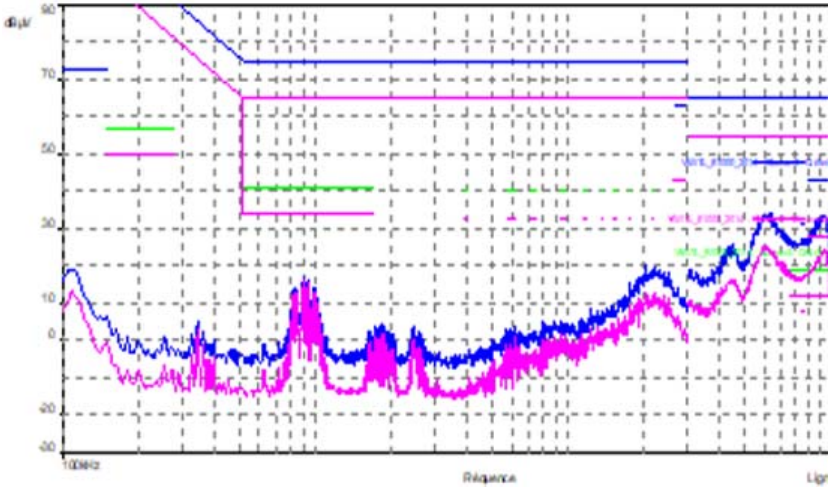


Note for buckboost, both input loop and output loop are hot loop with high di/dt

Case #3: 1.2A LED Driver, Buckboost, F_{SW} = 1MHz with SSFM

First EMI shot to duplicate customer test result

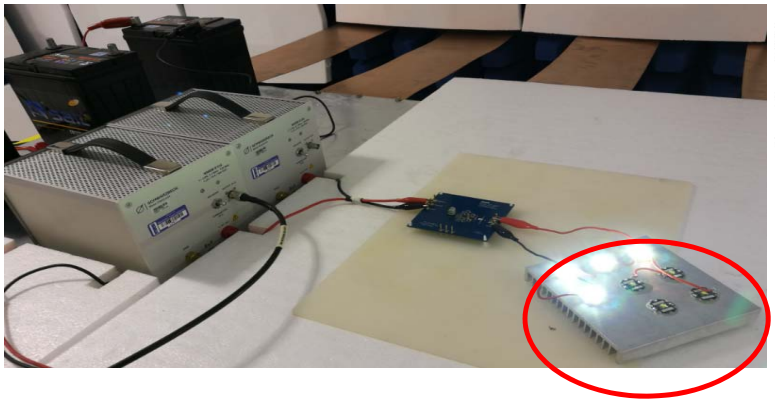
Customer Setup

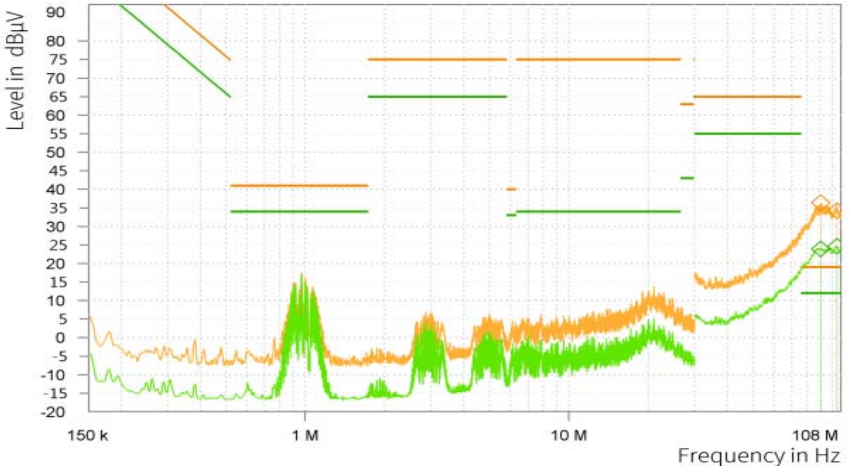


Duplicate similar result with similar setup

MPS Setup

similar bad setup
long output cable
large heatsink LED

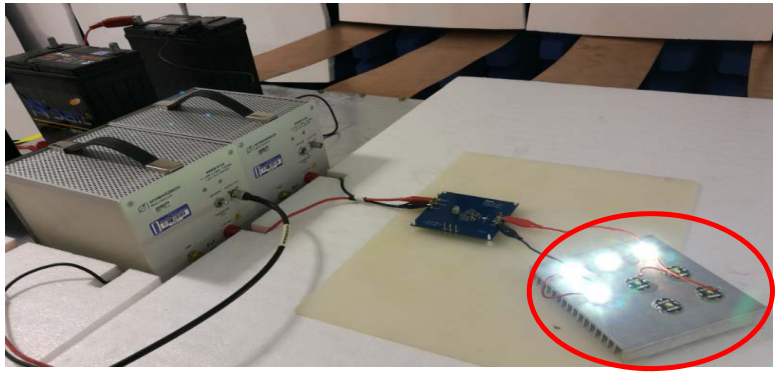




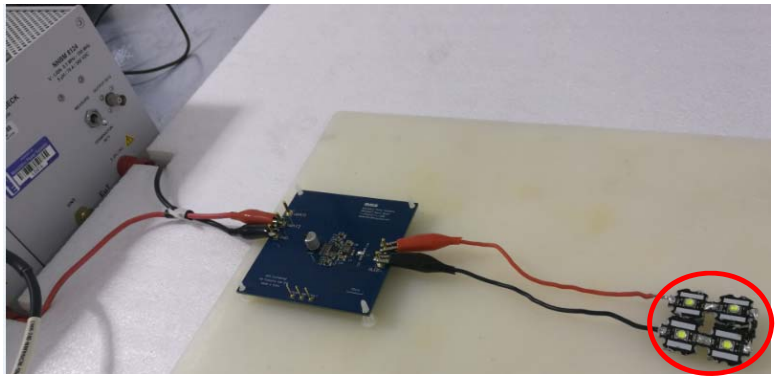
Case #3: 1.2A LED Driver, Buckboost, F_{SW} = 1MHz with SSFM

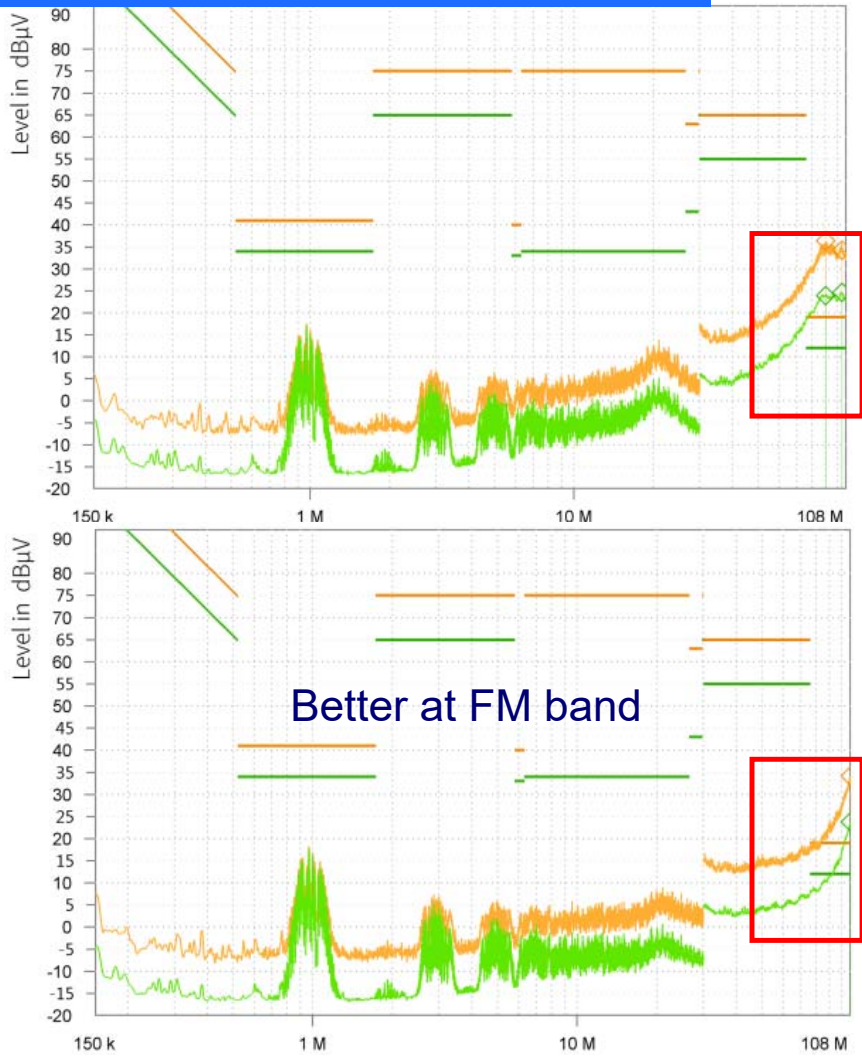
Optimization 1: smaller size load

Long wire and large heatsink LED load



Long wire but small heatsink LED load

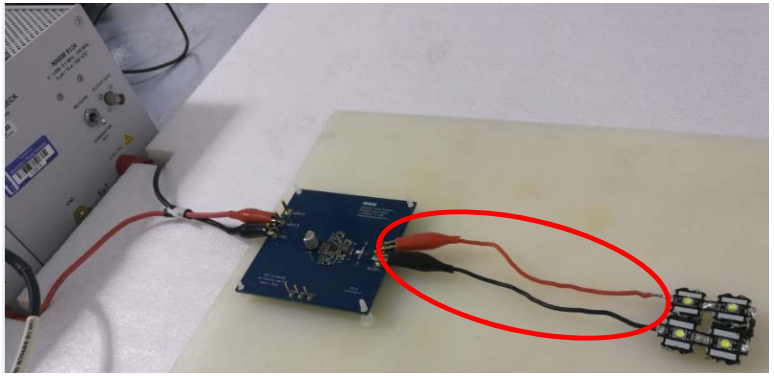




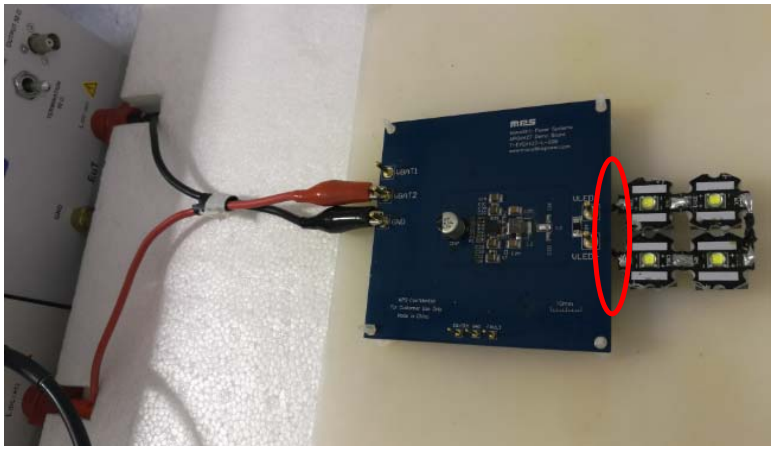
Case #3: 1.2A LED Driver, Buckboost, F_{SW} = 1MHz with SSFM

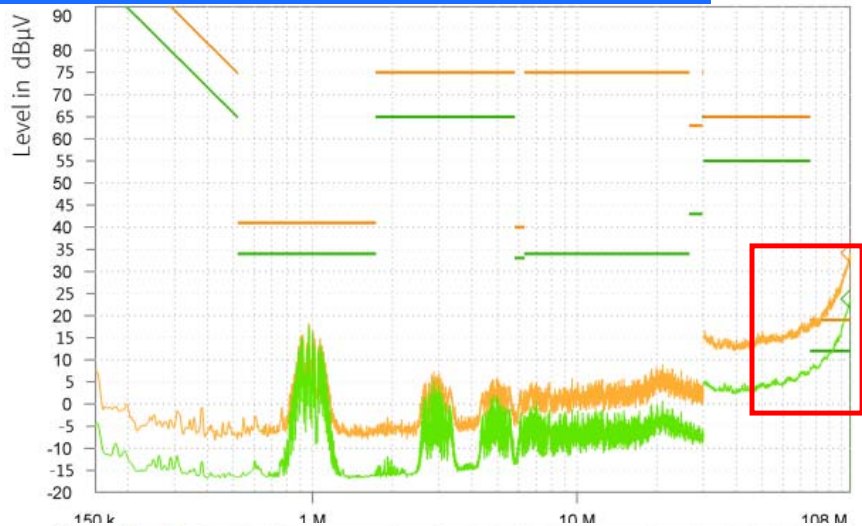
Optimization 2: Shorter output cable

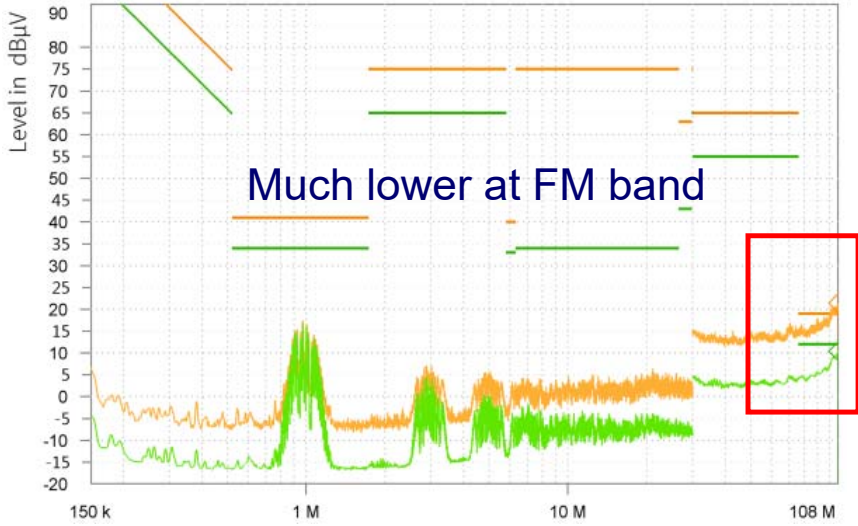
Long wire and small heatsink LED load



Short wire but small heatsink LED load



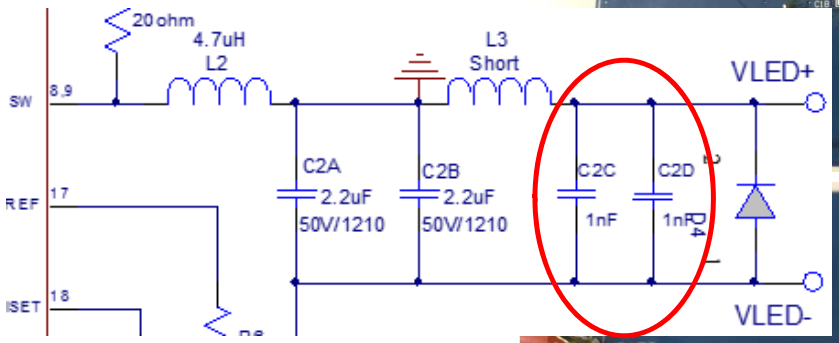




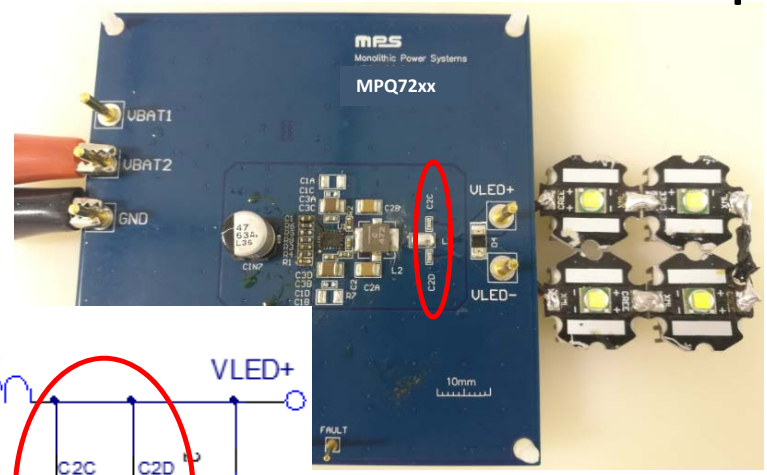
Case #3: 1.2A LED Driver, Buckboost, F_{SW} = 1MHz with SSFM

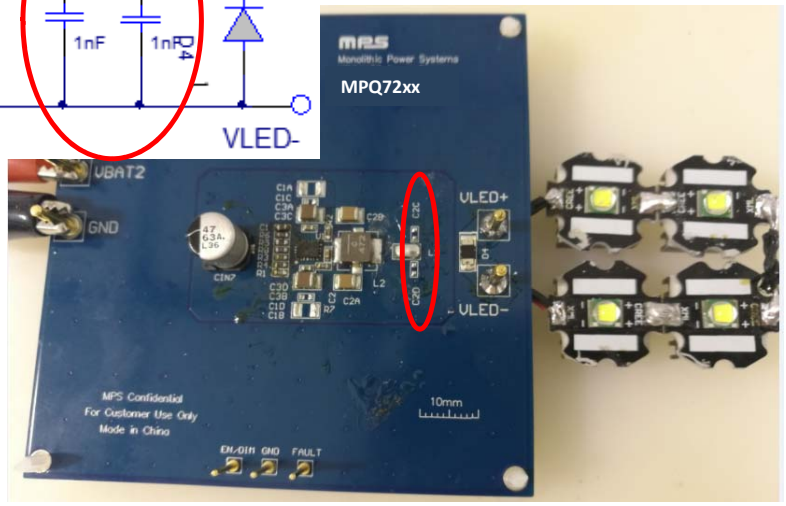
Optimization 3: Remove some Cout for small hot loop

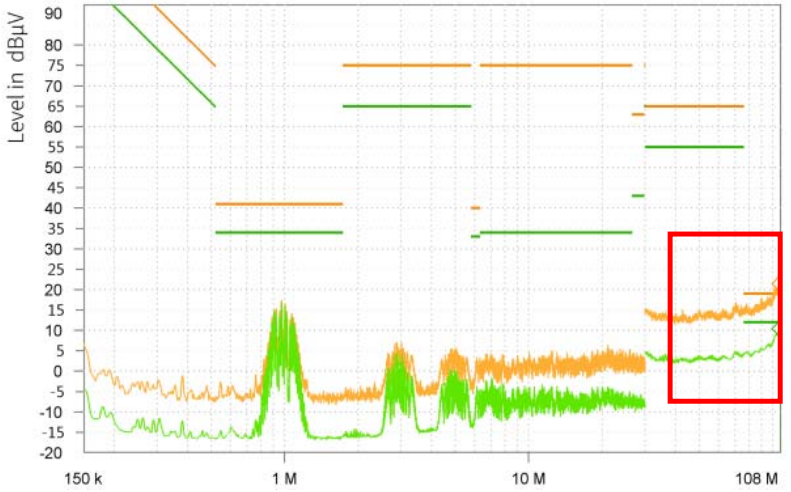
Wtih C2C & C2D as shown in SCH

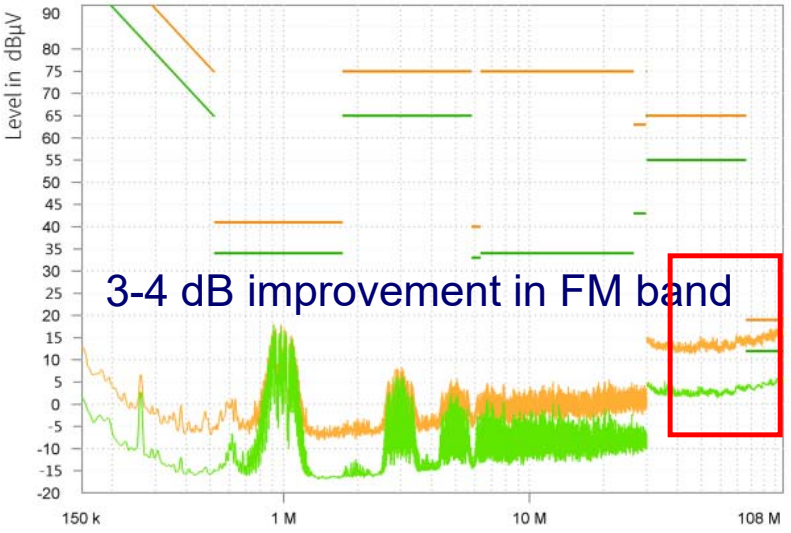


Remove C2C & C2D





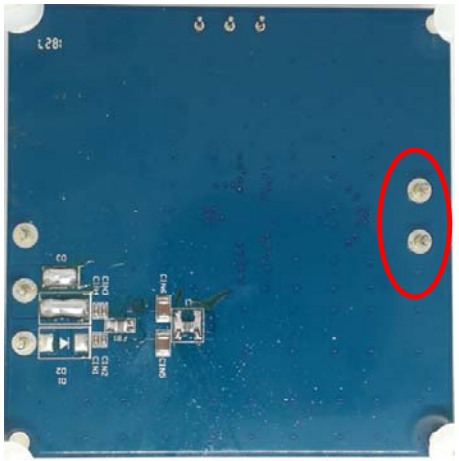




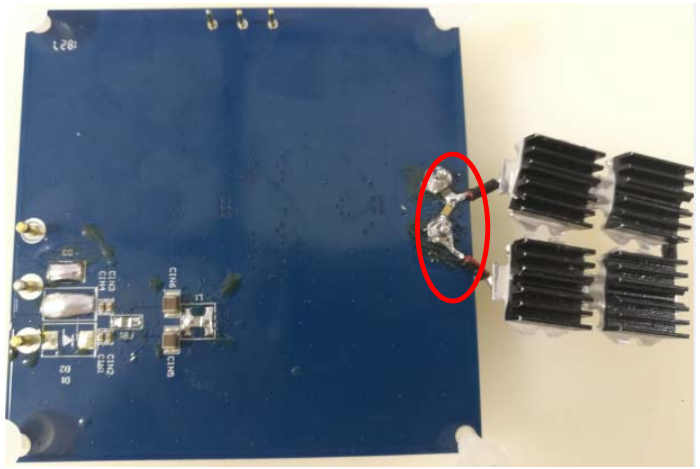
Case #3: 1.2A LED Driver, Buckboost, F_{SW} = 1MHz with SSFM

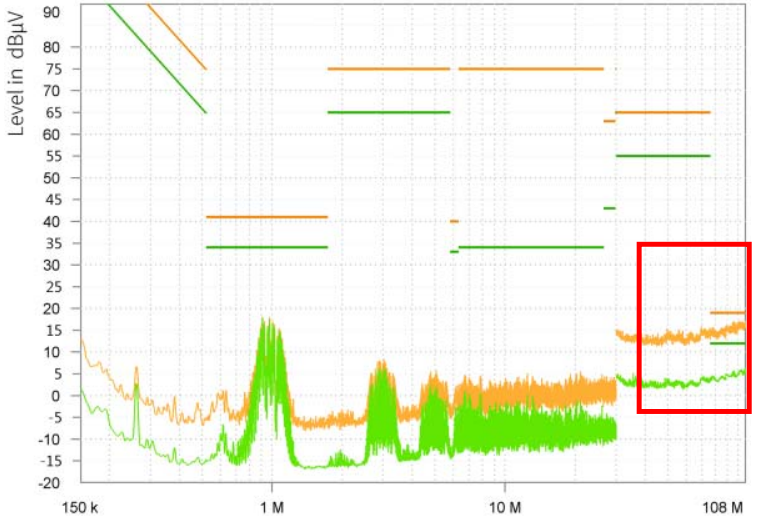
Optimization 4: Add output filter

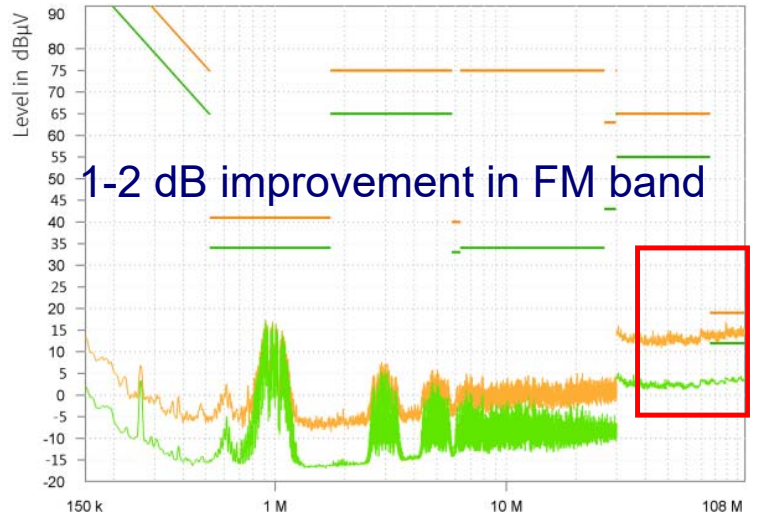
No output filter
in default SCH



Add 330nH L and 100nF
Cap on LED- trace as
output filter



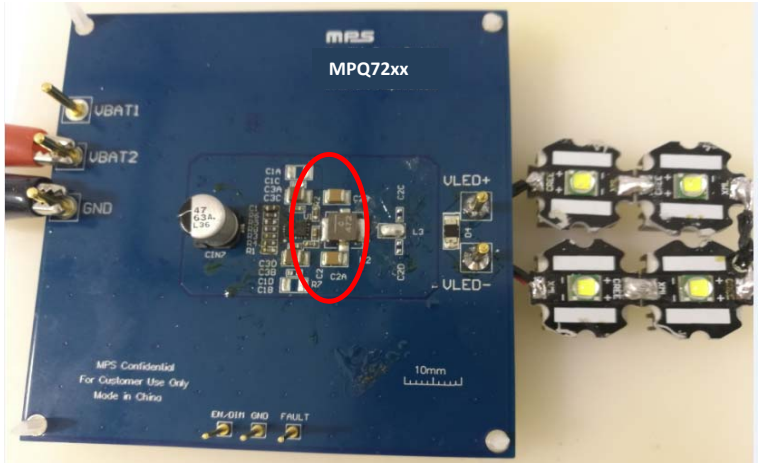




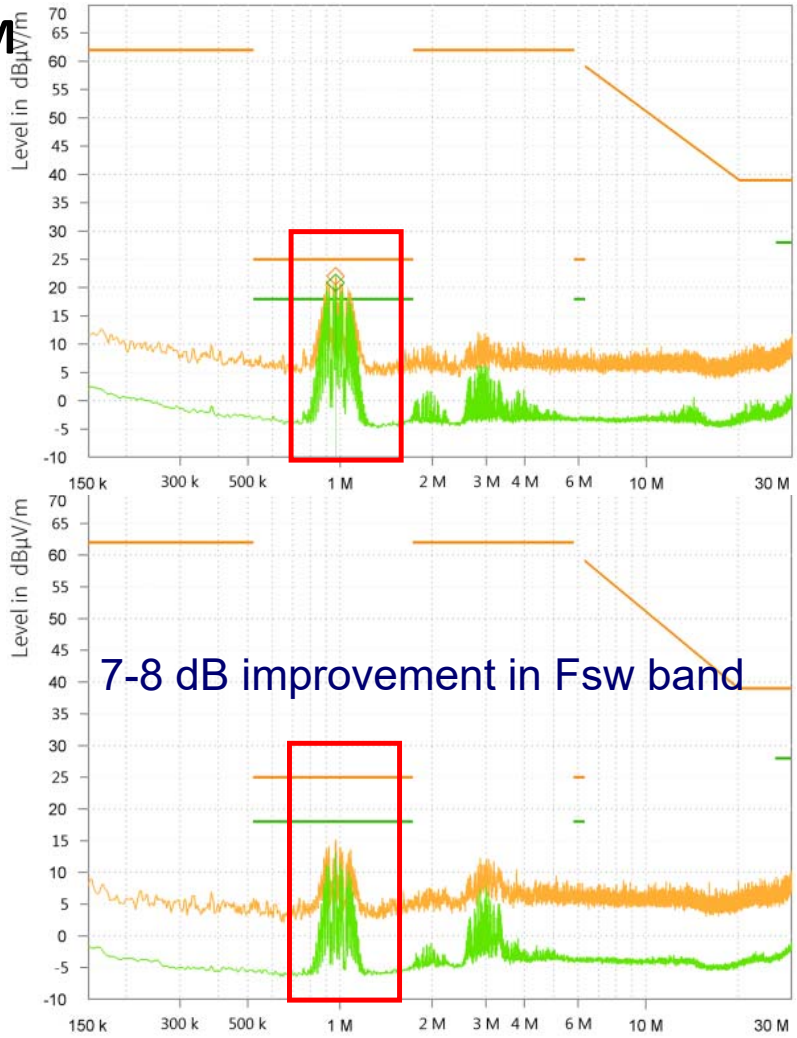
Case #3: 1.2A LED Driver, Buckboost, F_{sw} = 1MHz with SSFM

Optimization 5: Adjust L & Cout placement for RE 150k-30M

Placement as default layout



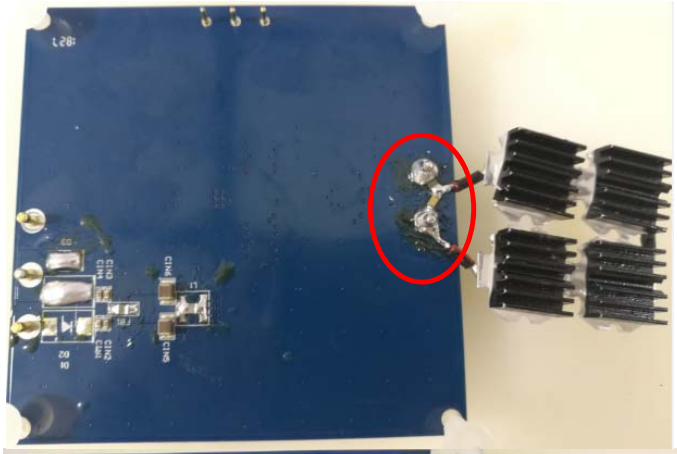
Place L2 closer to IC,
Place C2A & C2B closer
to L2 for some shielding



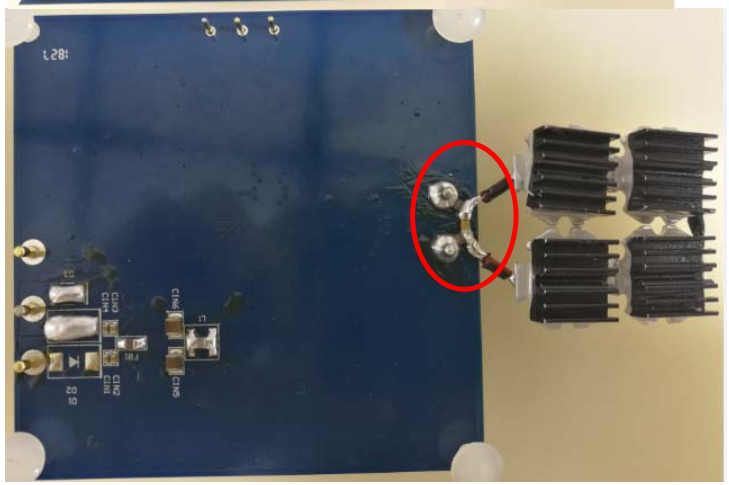
Case #3: 1.2A LED Driver, Buckboost, F_{SW} = 1MHz with SSFM

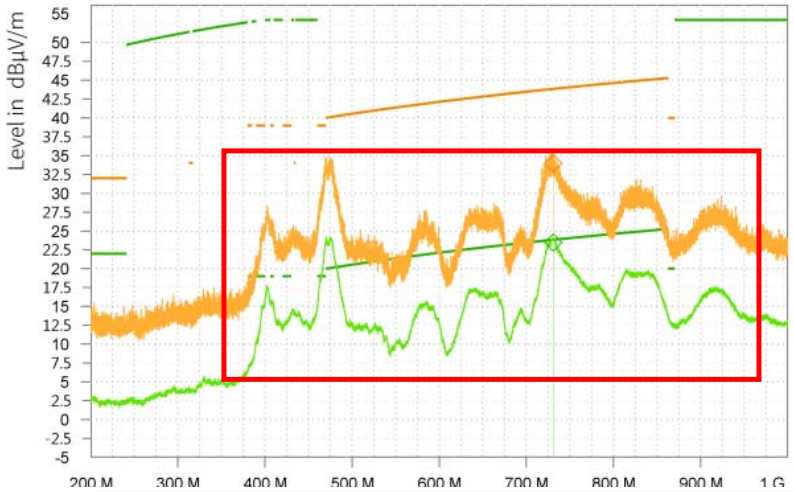
Optimization 6: Add CM output filter for RE 200M-1G

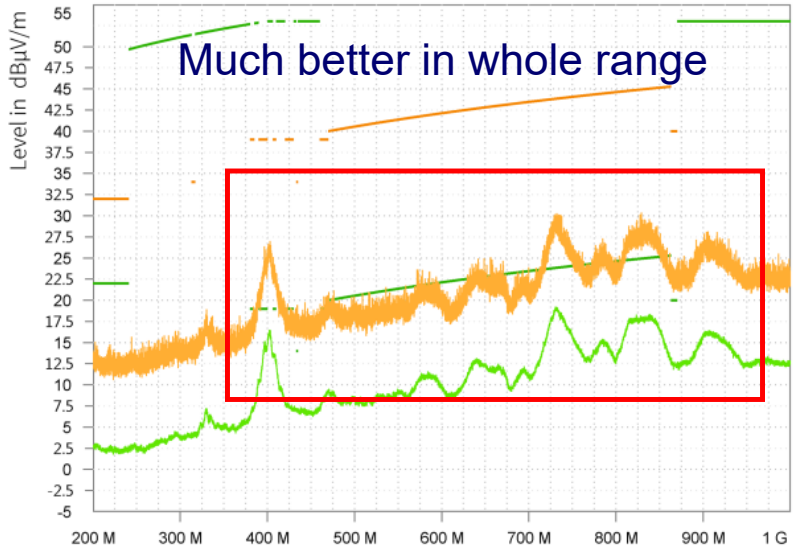
Only 330nH+100nF
LED- fitler



330nH on LED- and
330nH on LED+ and
100nF between LED+
and LED-







Conclusion

- **Learn background**

  Such as setup, standard, initial test result

- **Review schematic, layout, board**

  Focus on filter, high di/dt loop and dV/dt area

- **Issue identification**

  An appropriate filter, good inductor, Cu-foil shielding, snap-on ferrite, field probe can help

- **Performance optimization**

  According to theory and experience, following steps, try more times