Myth-busting for commonly used EMI reduction techniques in power converter design

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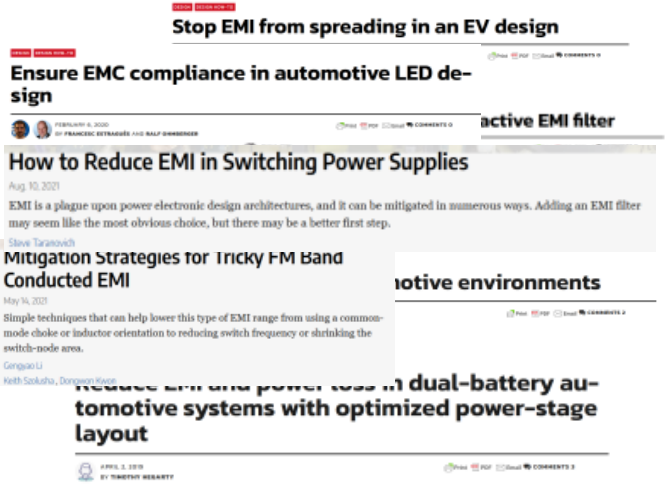
Introduction

In many seminars we are presented with a suite of techniques to improve the Electro-Magnetic Compatibility (EMC) of our designs.

These techniques don't often come with accurate A to B comparisons to evaluate if they are true, or "quantify" the impact of a particular implementation.

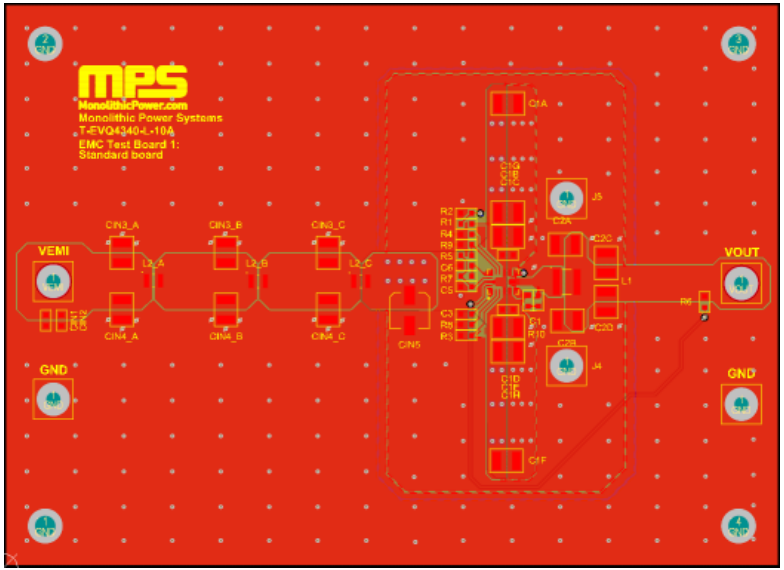
EMC is a very "design specific" topic, there are general physics laws that always apply, but things that are good for a particular design may not be optimal for a different one.

This presentation shows our efforts at trying to myth bust some of the most common EMC tips given in seminars.

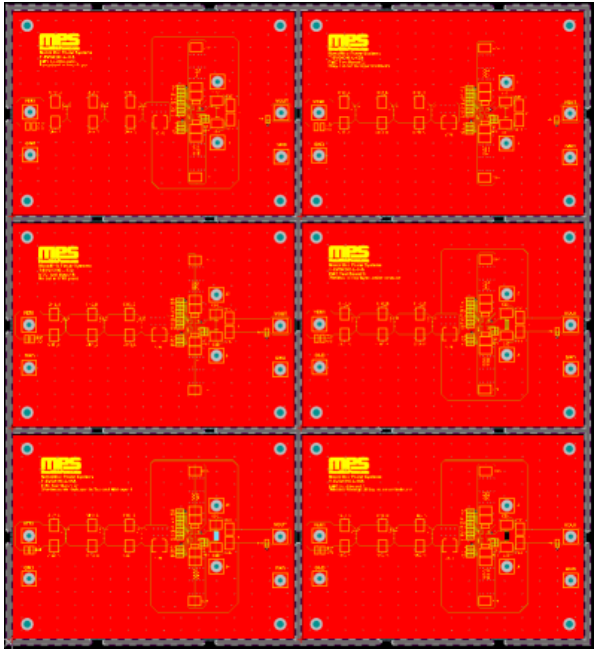


Methodology

In order to accurately study the effect of each individual design technique we have designed a set of PCBs that share a similar layout but each featuring a specific change.



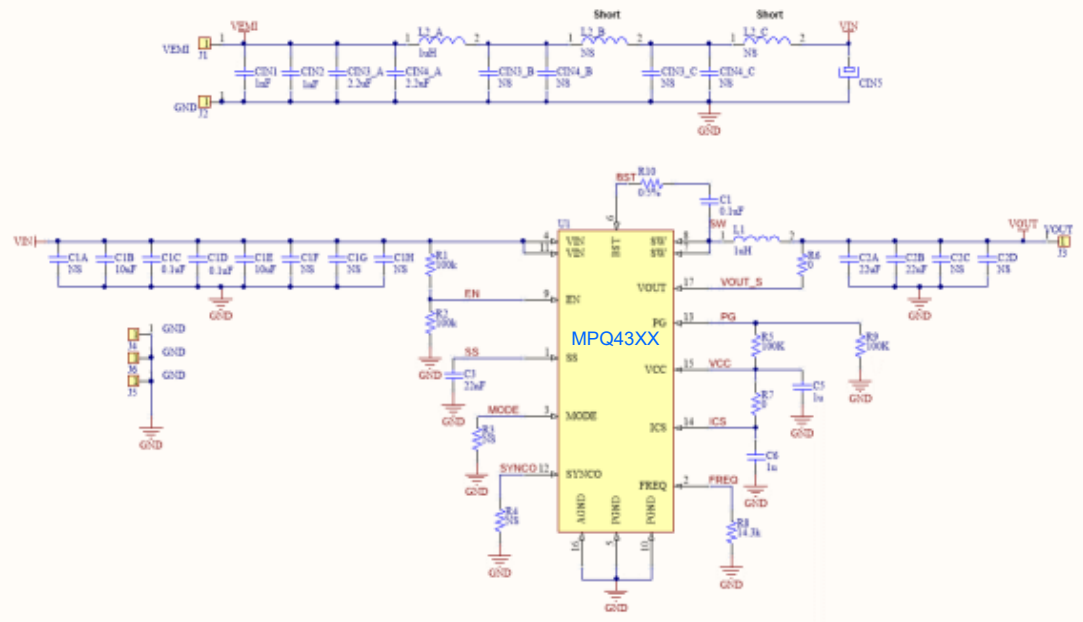
Standard Reference PCB



Layout variants

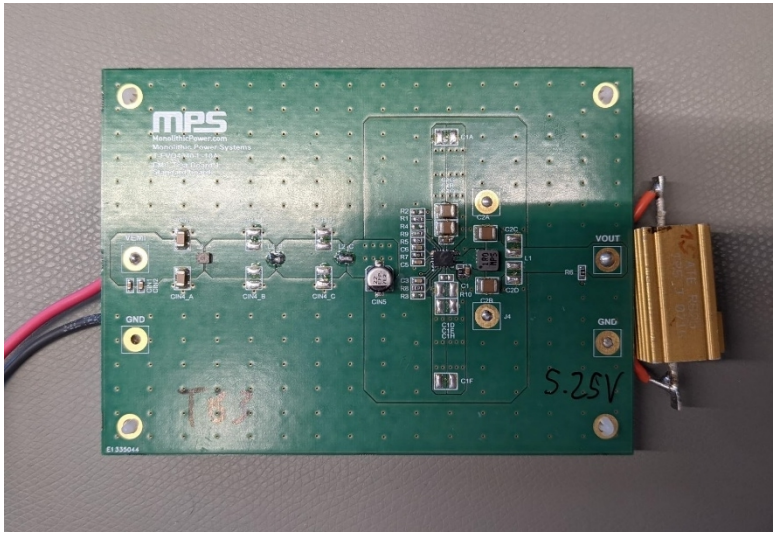
Methodology

All PCB variants share the same schematics, in some cases the components were populated in different positions for the comparison.



Methodology

The input harness follows CISPR25 standard. The output resistor is connected with short cables to the PCB. All test procedures follow CISPR25.

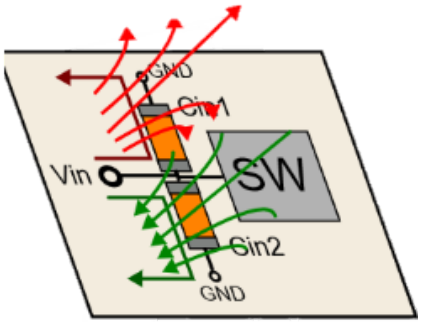


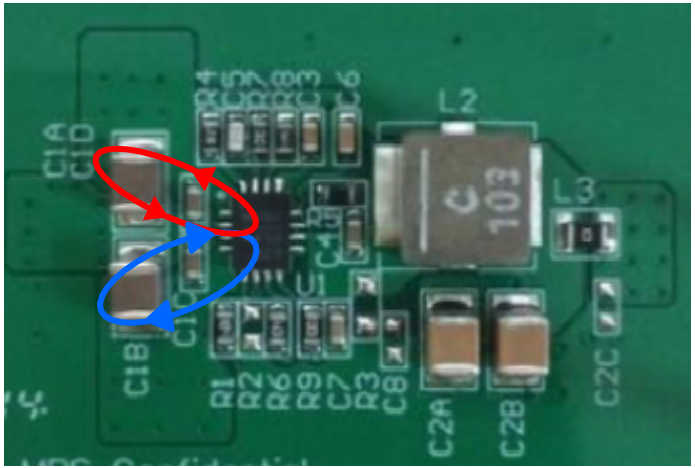
PCB test setup

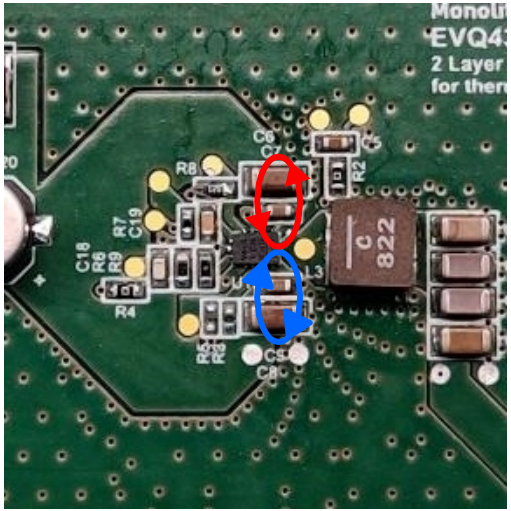
Case 1: Symmetrical Input Capacitors

What is the *myth* about?

When placing the input capacitors symmetrically, creating 2 opposing current loops, the magnetic fields created by the dI/dt cancel each other as they have opposite directions.

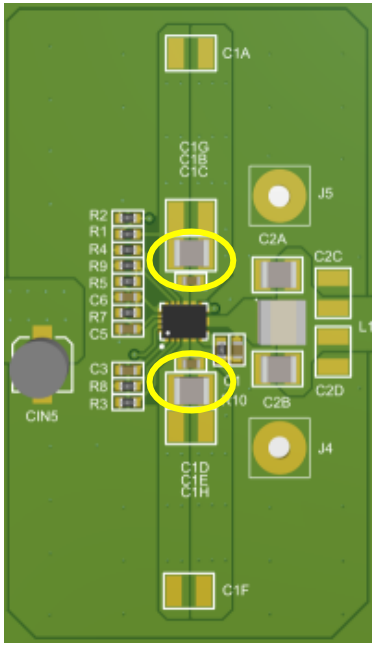






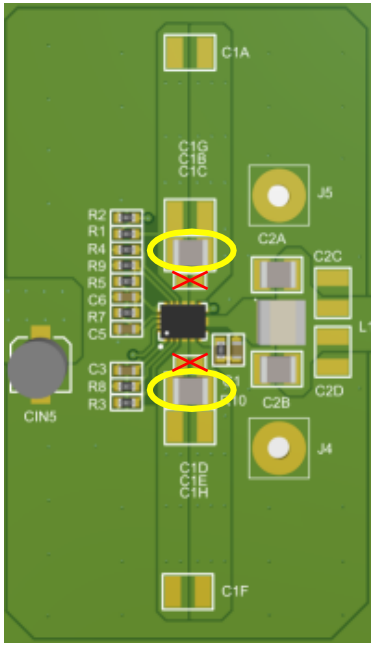
Case 1: Symmetrical Input Capacitors

How it was tested



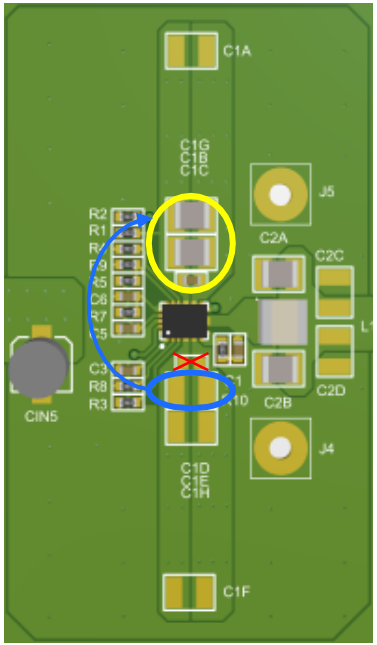
Symmetric Cin

TB6



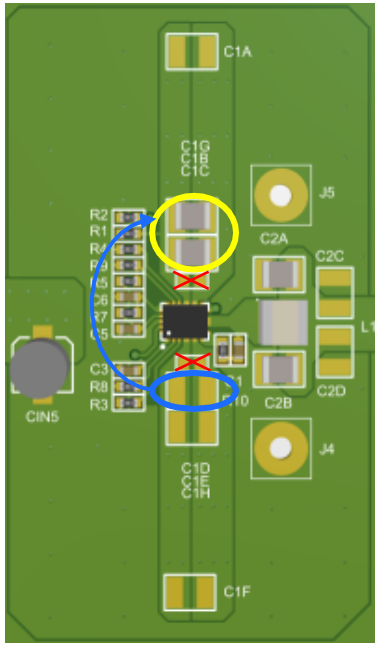
Symmetric Cin w/o small cap

TB6’



Non-symmetric Cin w/ small cap

TB3



Non-symmetric Cin w/o small cap

TB3’

Case 1: Symmetrical Input Capacitors

Test results

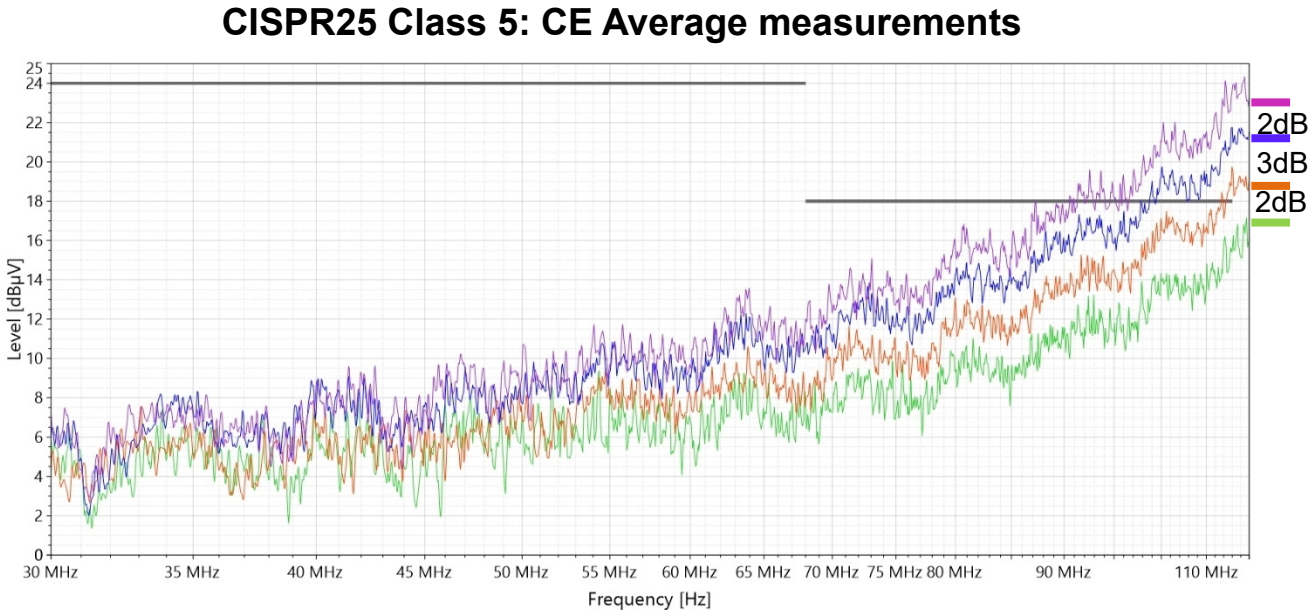
In the FM band Symmetric Cin is always better. Having the 100nF capacitor is always better.

TB6: Symmetric Cin with 100nF

TB6': Symmetric Cin removing 100nF

TB3: Asymmetric Cin with 100nF

TB3': Asymmetric Cin removing 100nF



Case 1: Symmetrical Input Capacitors

Test results

In 1 and 3 the symmetric Cin is ~8dB better. In 2 the symmetric Cin is ~8dB worse. In 4 it is ~3dB worse.

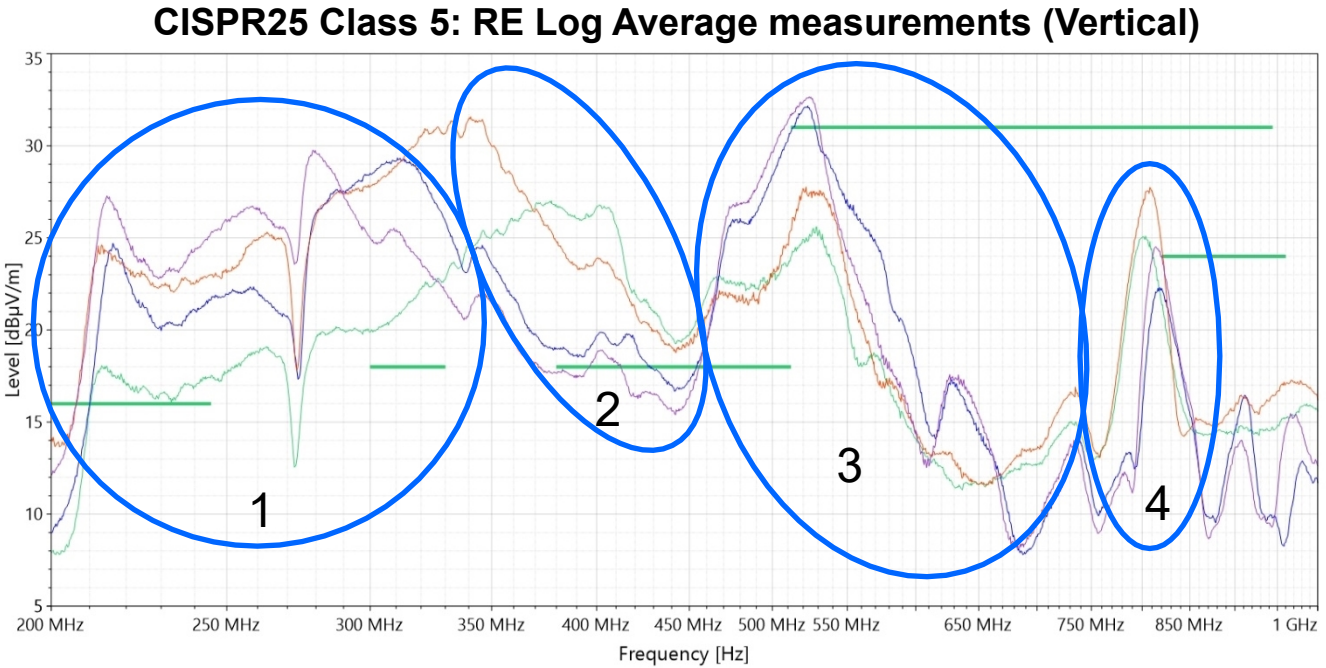
The 100nF capacitor is always an improvement.

TB6: Symmetric Cin with 100nF

TB6': Symmetric Cin removing 100nF

TB3: Asymmetric Cin with 100nF

TB3': Asymmetric Cin removing 100nF



Case 1: Symmetrical Input Capacitors

Myth-busting

The symmetrical input capacitors help improve the EMI in the critical FM band for the Conducted Emissions test.

The 100nF capacitors are helpful in almost all frequencies.

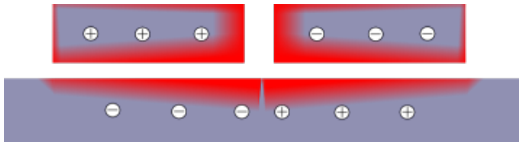
In the Radiated Emissions test, the symmetrical CIN improve the emissions in most bands, while in others they degrade the performance.

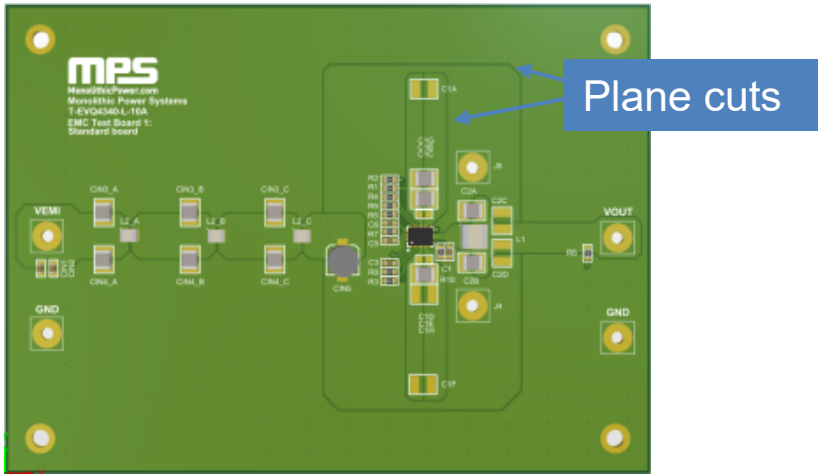
Confirmed

Case 2: Ground plane splitting

What is the *myth* about?

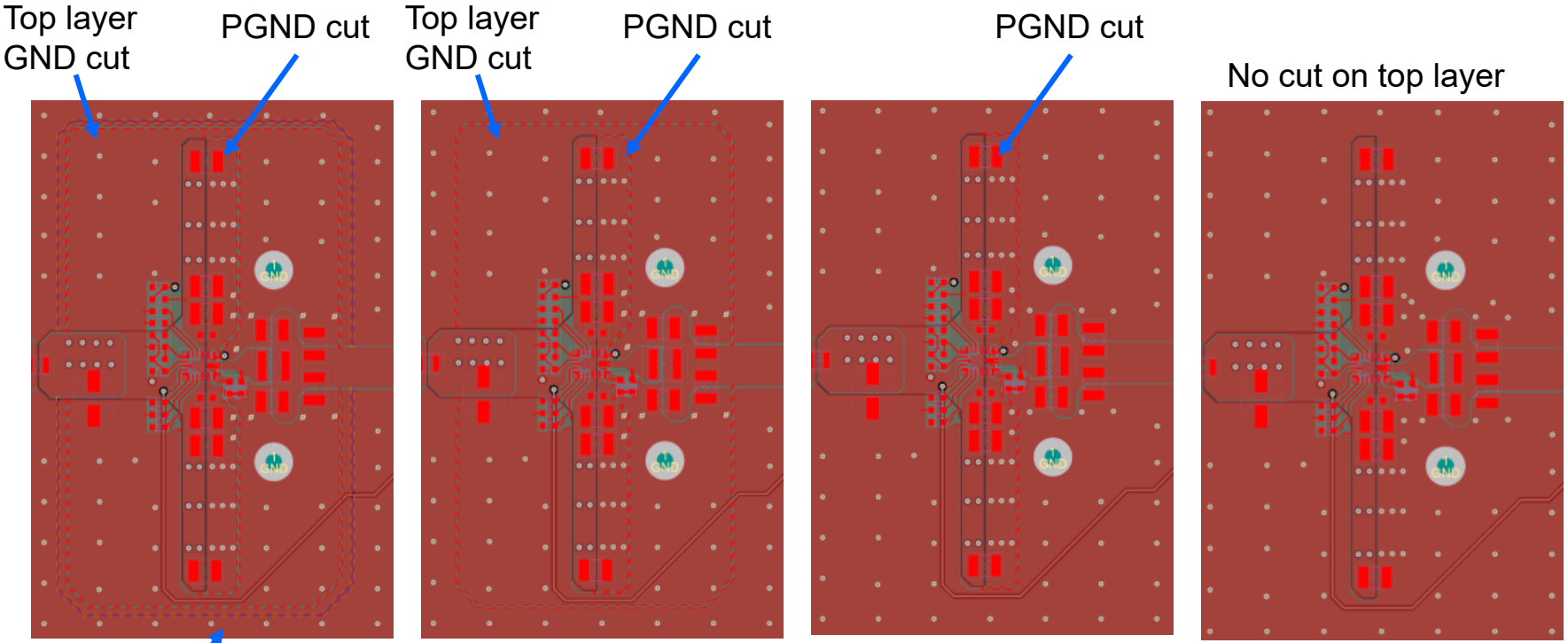
Return currents in the GND plane are mostly concentrated next to their source conductor, but part of them is spread over a wider surface of the plane. These larger current loops form a magnetic antenna and will radiate. By cutting the GND portion of the hot loop from the rest of the board's GND, these current loops are forced to be smaller and thus, the emission will be lower.





Case 2: Ground plane splitting

How it was tested



TB6 TB11 TB12 TB13

Case 2: Ground plane splitting

Test results

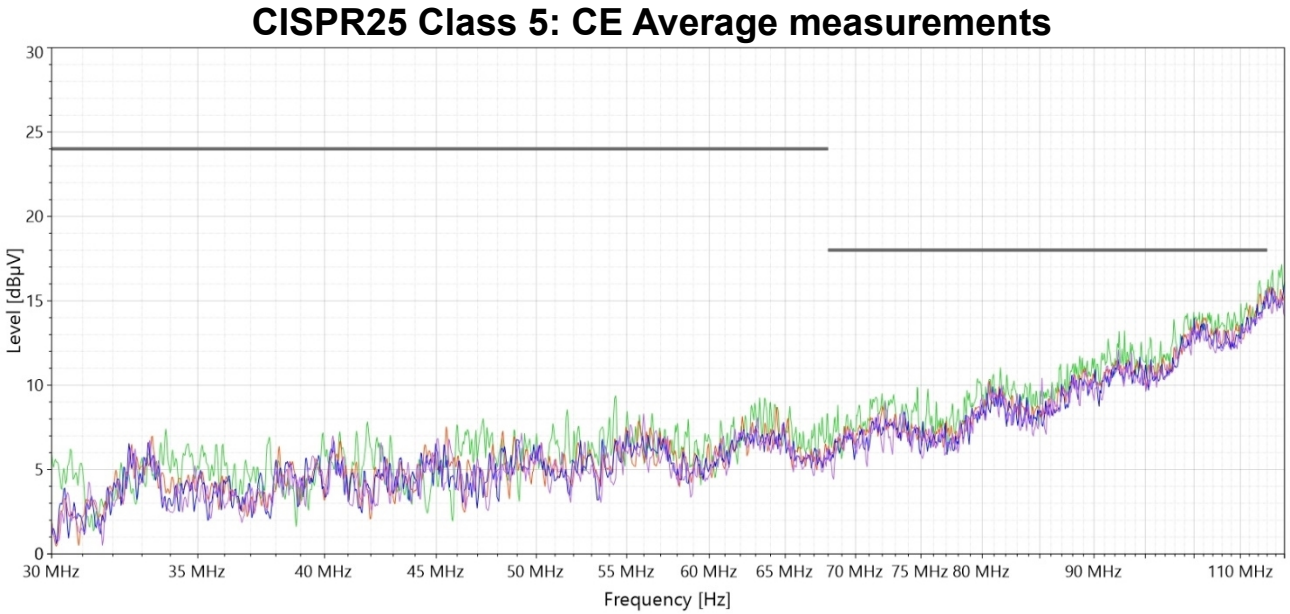
There is not too much difference

TB6: All GND cuts

TB11: Removing Internal GND cut

TB12: Removing Internal and Top GND cut

TB13: Removing all cuts



Case 2: Ground plane splitting

Test results

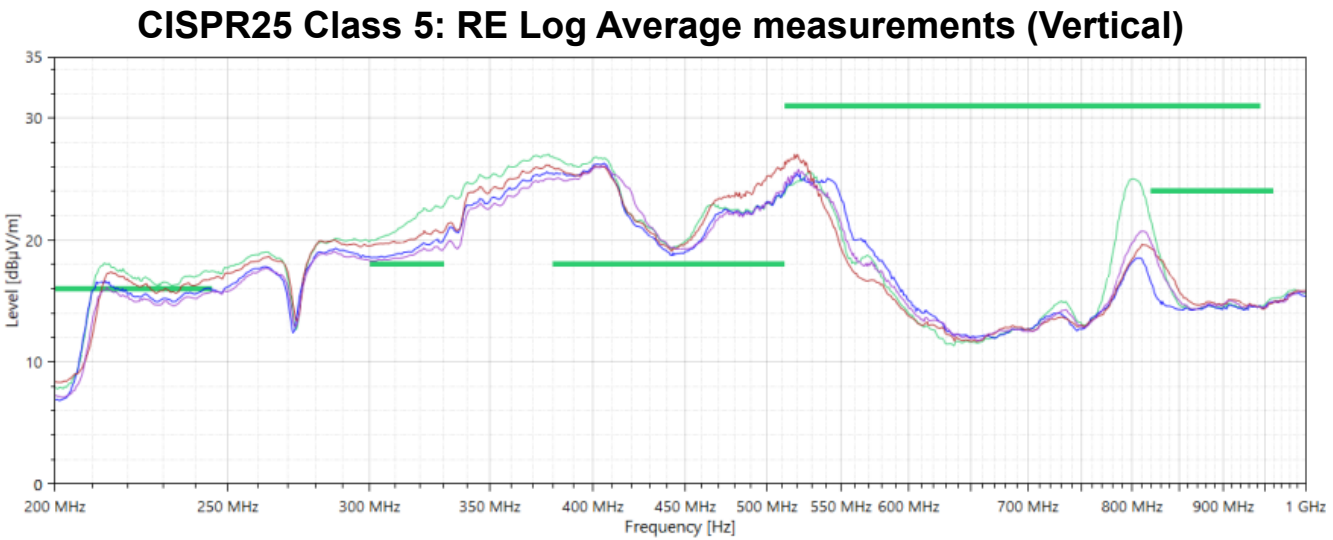
Cutting the GND in several locations makes things worse. The best case is when making a local cut to the PGND.

TB6: All GND cuts

TB11: Removing Internal GND cut

TB12: Removing Internal and Top GND cut

TB13: Removing all cuts



Case 2: Ground plane splitting

Mythbusting

Splitting the GND plane does not have a significant impact on EMI (<1 dBµV/m).

Cutting the GND plane in multiple areas degrades the GND impedance, making the board worse.

Conclusions

- Many EMC recommendations given in seminars are not valid across all designs. There are several variables at play (PCB size, load type, harnesses…).
- The way to ensure if a design is going in the right direction is through testing or simulating in the early stages of development.
- Start the design following the typical EMC good practices
- Simulate or test the initial design and see what are the shortcomings. Then come up with a plan.
- Execute the improvement plan, then repeat the simulation or testing.

Q&A