Motor Drivers: Thermal Management

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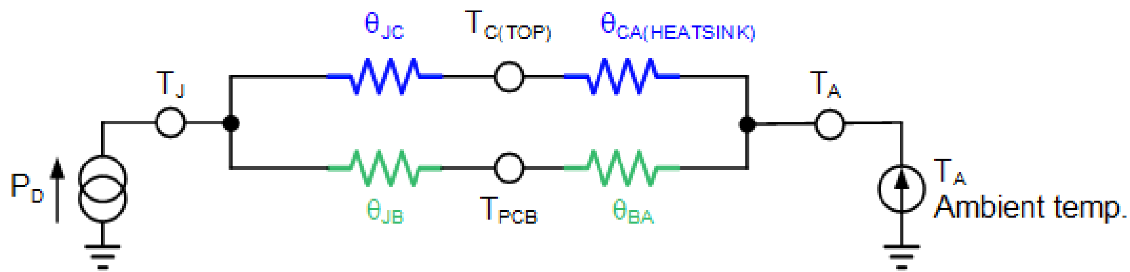
Thermal Resistance and Electrical Analogy

Thermal resistance is a heat property and a measurement of a temperature difference by which material resists a heatflow



Electrical Quantities (1)			Thermal Quantities (2)		
Quantity	**Formula Symbol**	**Unit**	**Quantity**	**Formula Symbol**	**Unit**
Voltage	$U(t)$	V	Temperature difference	$\Delta T(t)$	K
Current	$I(t) = \frac{dQ_{el}}{dt}$	A	Heat flow	$\Phi(t) = \frac{dQ_{th}}{dt}$	W
Charge	$Q_{el}(t) = \int I\,dt$	A x s	Heat quantity	$Q_{th}(t) = \int \Phi\,dt$	W x s
Capacitance	C_{el}	$\frac{A \times s}{V}$	Heat capacity	$C_{th} = c \times \rho \times V$	$\frac{W \times s}{K}$
Resistance	$R_{el} = \frac{L}{\varkappa \times A}$	$\Omega = \frac{V}{A}$	Thermal resistance	$R_{th} = \frac{L}{\lambda \times A}$	$\frac{K}{W}$
Conductance	$G_{el} = \frac{I}{R_{el}}$	$S = \frac{A}{V}$	Thermal conductivity	$G_{th} = \frac{I}{R_{th}}$	$\frac{W}{K}$
Electric conductivity	$\varkappa$	$\frac{A}{V \times m}$	Thermal conductivity	λ	$\frac{W}{m \times K}$

1. The contents of this table are from Technische Temperaturmessung: Volume I, Frank Bernhard, ISBN 978-3-642-62344-8.
2. el refers to electrical values, and th refers to thermal values.

Source: https://www.monolithicpower.com/en/understanding-datasheet-thermal-parameters-and-ic-junction-temperatures

Thermal Theory

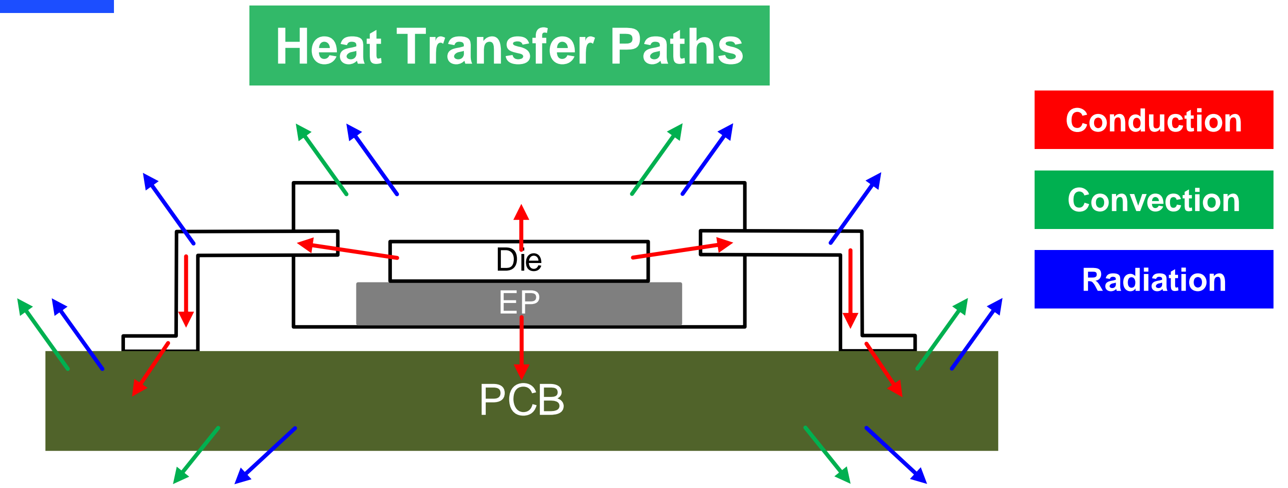
Heat transfer mechanisms:

- Conduction: $Q = \frac{k \cdot A \cdot \Delta T}{L}$
- Convection: $Q = k \cdot A \cdot \Delta T$
- Radiation: $Q = \varepsilon \cdot \sigma \cdot A \cdot ({T_{PCB}}^4 - {T_{AMB}}^4)$

Where:

$Q = heat$
$\mathrm{k} = material\ conductivity$
$A = area$
$L = thickness$

$h = convection\ coefficient$
$\Delta\mathrm{T} = temperature\ delta$
$\varepsilon = emisivity$
$\sigma = Boltzman\ constant$



For natural convection heat transfer,
>90% of the heat is dissipated by the board and not from the package surfaces

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Thermal Resistance Definitions

(1) $R_{\theta JA}$ junction-to-ambient thermal resistance:

$$R_{\theta JA} = (T_J - T_A) / P_H$$

Where $R_{\theta JA}$ = thermal resistance from junction-to-ambient (°C/W)
T_J = junction temperature (°C)
T_A = ambient temperature (°C)
P_H = power loss that produced change in the junction temperature (W)

(2) $R_{\theta JB}$ junction-to-board thermal resistance:

$$R_{\theta JB} = (T_J - T_B) / P_{HB}$$

Where $R_{\theta JB}$ = thermal resistance from junction-to-board (°C/W)
T_J = junction temperature (°C)
T_b = board temperature at steady state (°C)
P_{HB} = power loss of heatflows through the board (W)

(3) $R_{\theta JC_TOP}$ junction-to-case top thermal resistance:

$$R_{\theta JC_TOP} = (T_J - T_{C_TOP}) / P_{HCTOP}$$

Where $R_{\theta JC_TOP}$ = thermal resistance from junction-to-case top
T_{C_TOP} = package top temperature (°C)
T_J = junction temperature (°C)
P_{HCTOP} = power loss of heatflows through the package top (W)

(4) $R_{\theta JC_BOT}$ junction-to-case bottom thermal resistance:

$$R_{\theta JC_BOT} = (T_J - T_{C_BOT}) / P_{HCBOT}$$

Where $R_{\theta JC_BOT}$ = thermal resistance from junction-to-case bottom
T_{C_BOT} = package bot temperature (°C)
T_J = junction temperature (°C)
P_{HCBOT} = power loss of heatflows through the package bottom (W)

(5) Ψ_{JT} junction-to-case thermal characterization parameter:

$$\Psi_{jt} = (T_J - T_{C_TOP}) / P_H$$

Where Ψ_{JT} = thermal characterization parameter from junction-to-case
T_{C_TOP} = package top temperature (°C)
T_J = junction temperature (°C)
P_H = power loss that produced change in the junction temperature (W)

(6) Ψ_{JB} junction-to-board thermal characterization parameter:

$$\Psi_{jb} = (T_J - T_B) / P_H$$

Where Ψ_{JB} = thermal characterization parameter from junction-to-case
T_B = board temperature (°C)
T_J = board temperature at steady state (°C)
P_H = power loss that produced change in the junction temperature (W)

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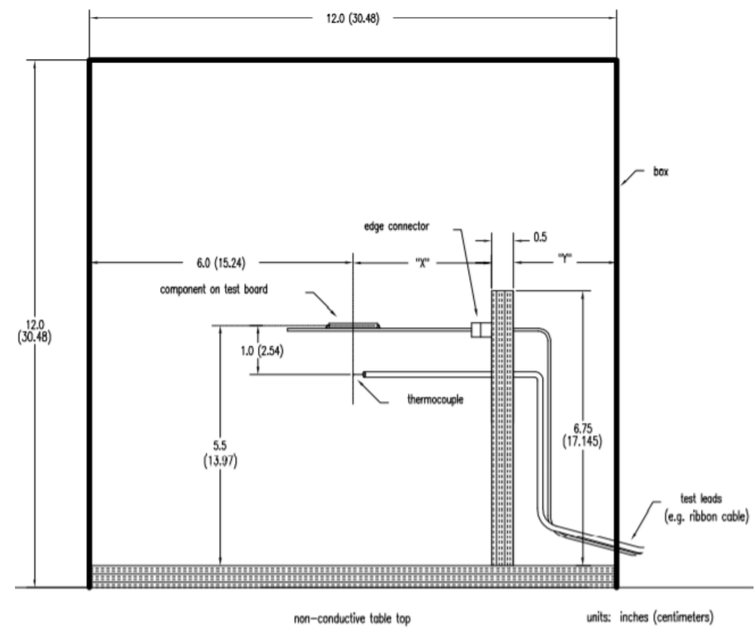
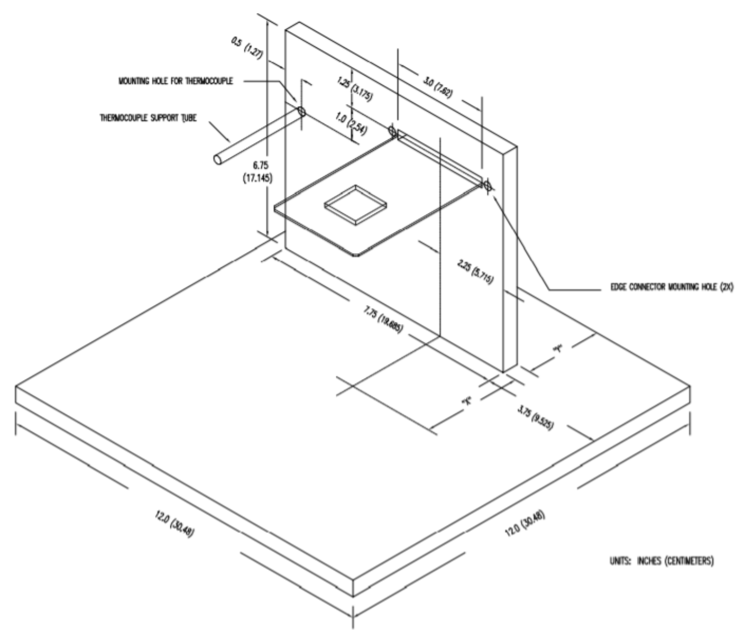
JESD51 Test Setup ($R_{\theta JA}$, Ψ_{JT}, Ψ_{JB})

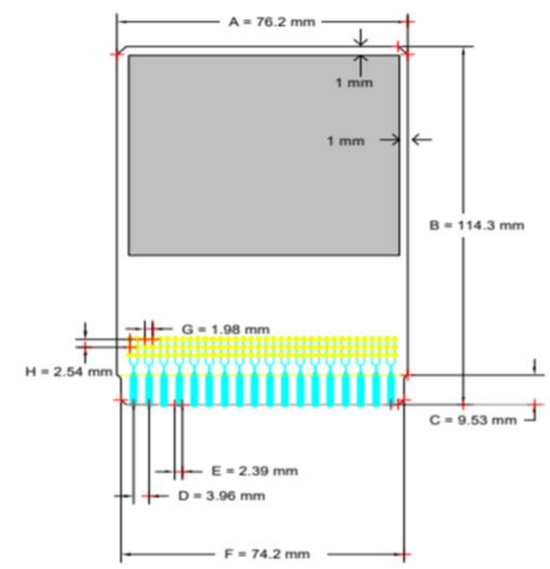
$R_{\theta JA}$, Ψ_{JT}, and Ψ_{JB} thermal resistances are based on JESD51-2 (Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)).

The device is attached to the PCB and placed in a closed environment. The enclosure shall be a box with an inside dimension of $1ft^3$ ($0.0283m^3$). All seams should be thoroughly sealed to ensure no airflow through the enclosure.

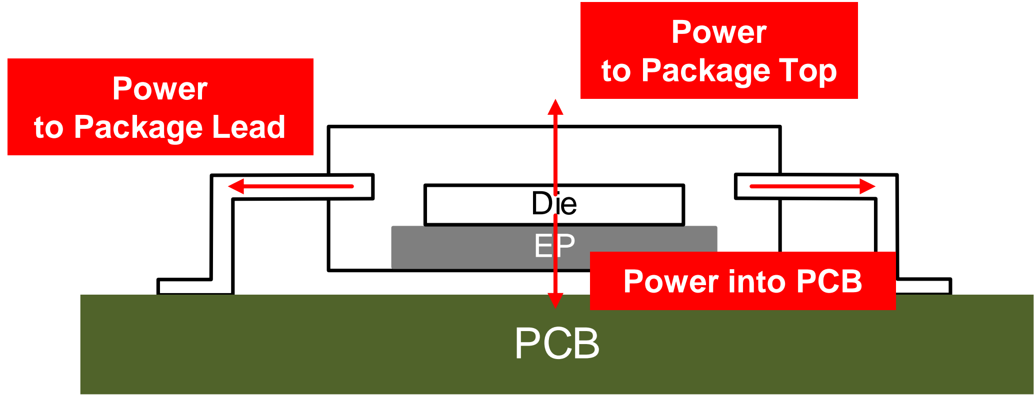
The PCB board (high-K) has 4 metal layers, 1.6mm thickness.

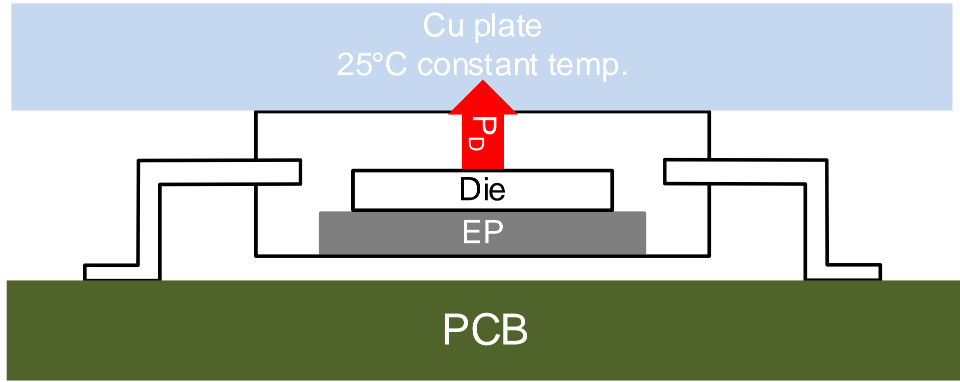


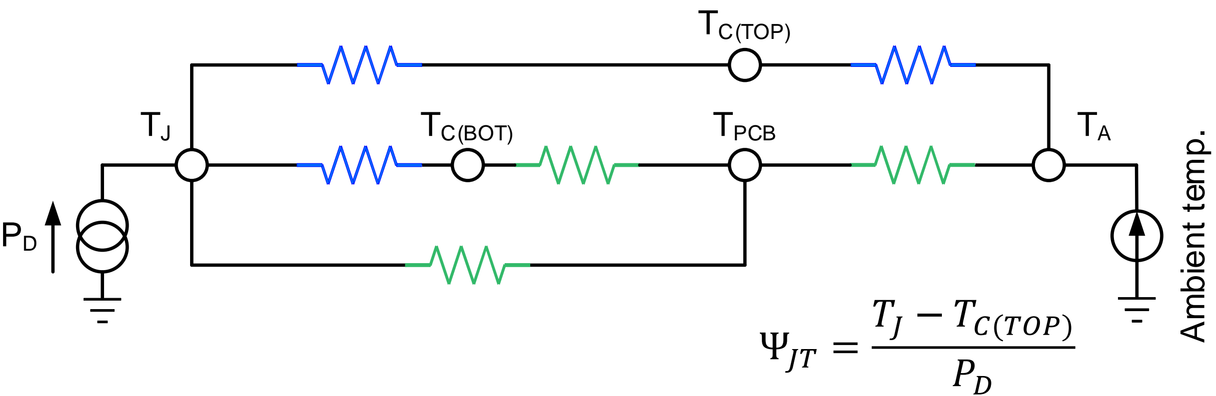




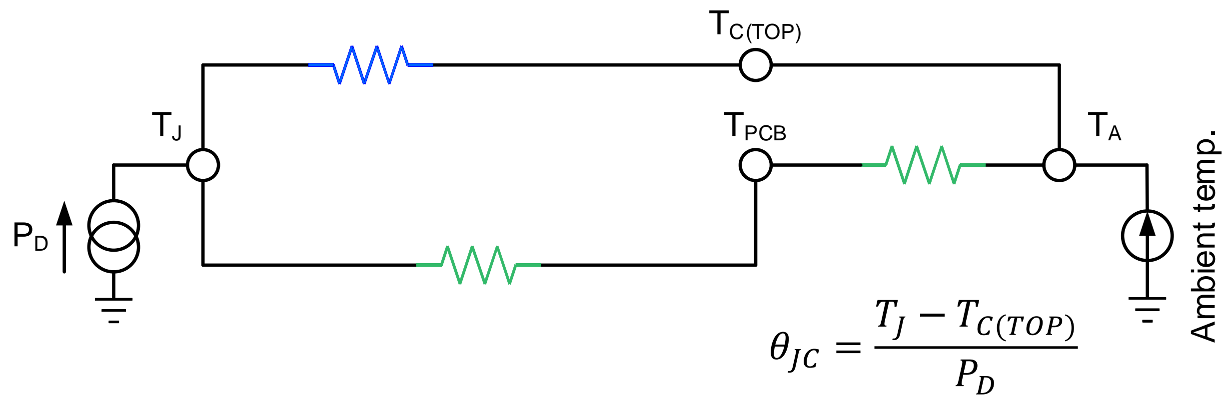
PSI Junction-Top (Ψ_{JT}) vs. Theta Junction-Case (θ_{JC})







$$\Psi_{JT} = \frac{T_J - T_{C(TOP)}}{P_D}$$

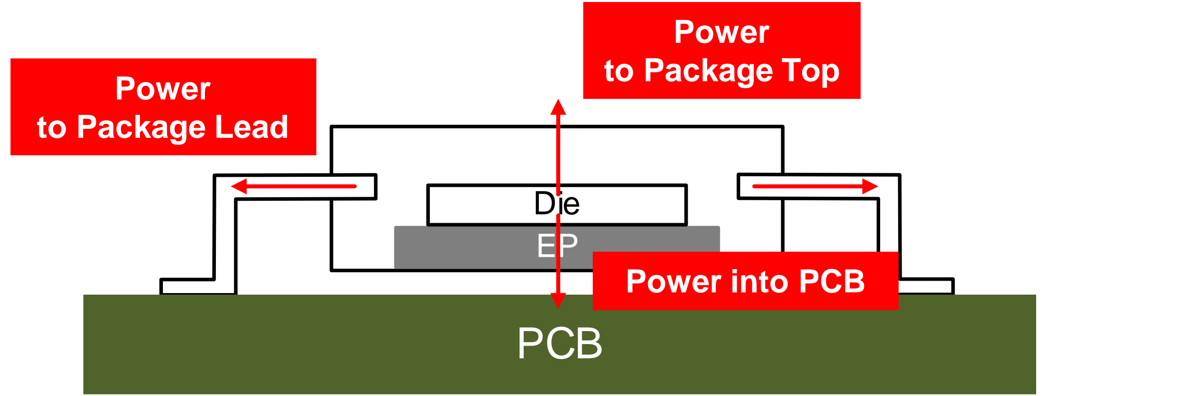


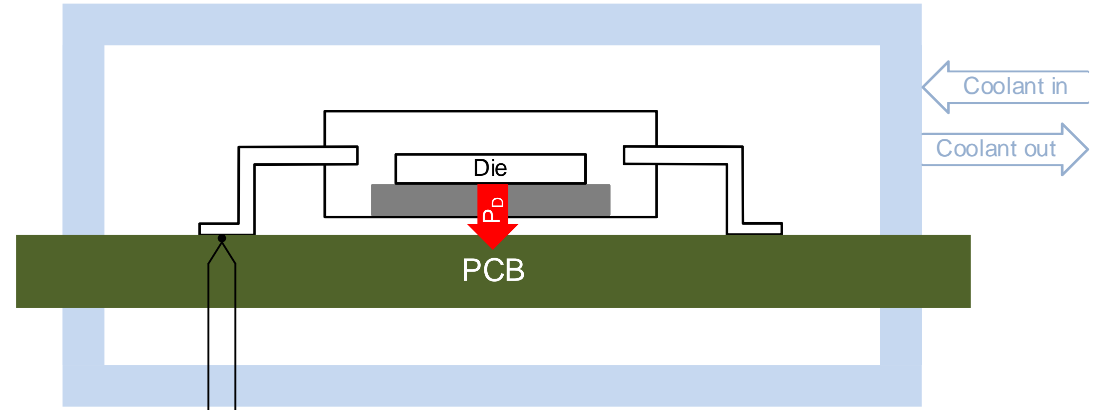
$$\theta_{JC} = \frac{T_J - T_{C(TOP)}}{P_D}$$

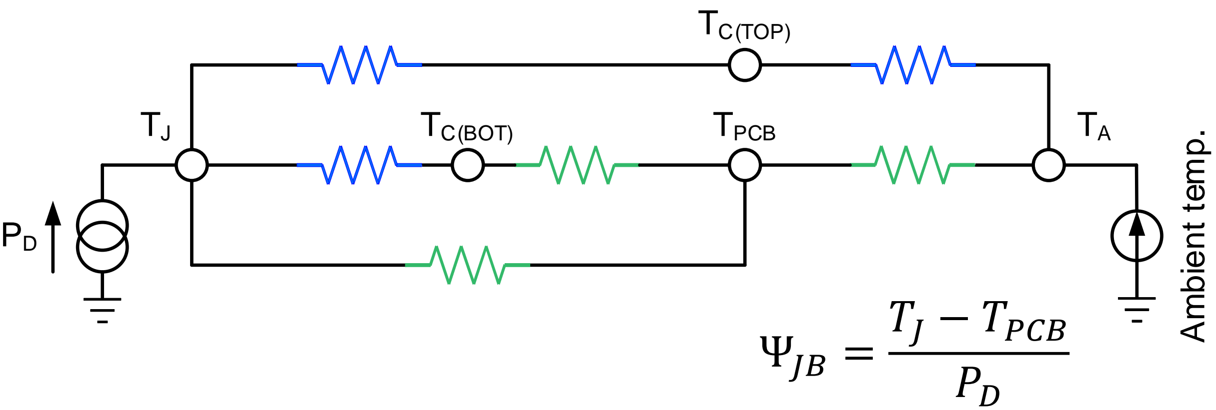
PSI Junction-Top (Ψ_{JT})
Power is dissipated in all directions

Theta Junction-Case (θ_{JC})
All power is forced to dissipate in only one direction (upward)

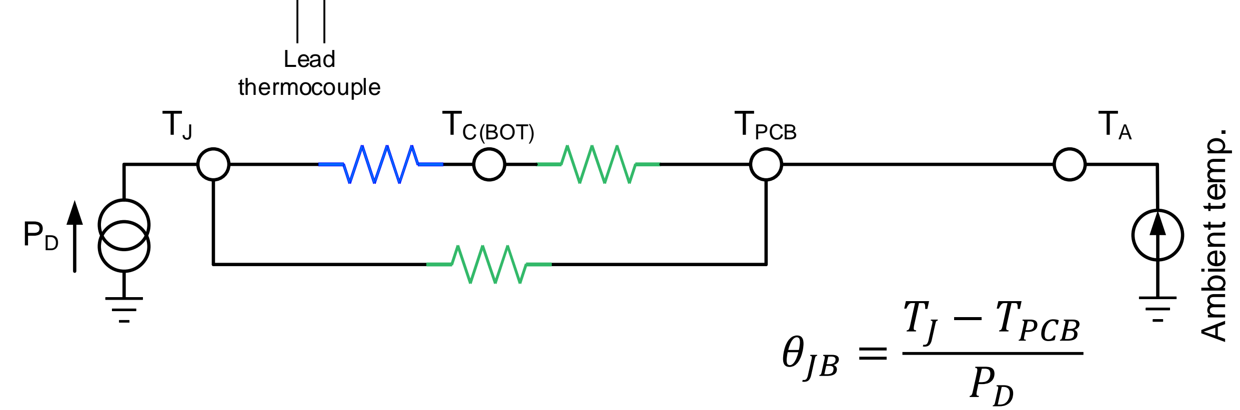
PSI Junction-Board (Ψ_{JB}) vs. Theta Junction-Board (θ_{JB})







$$\Psi_{JB} = \frac{T_J - T_{PCB}}{P_D}$$



$$\theta_{JB} = \frac{T_J - T_{PCB}}{P_D}$$

PSI Junction-Board (Ψ_{JB})
Power is dissipated in all directions

Theta Junction-Case (θ_{JB})
All power is forced to dissipate into the board

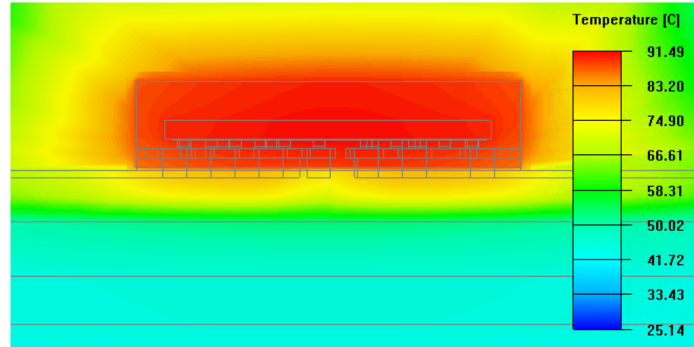
MPQ6612 Simulated Thermal Parameters

Theta JA (Junction-to-Air)

$R_{\theta JA} = (T_J - T_A) / P_H$

T_J = 91.5°C, T_A = 25.1°C

$R_{\theta JA}$ = 44.3°C/W

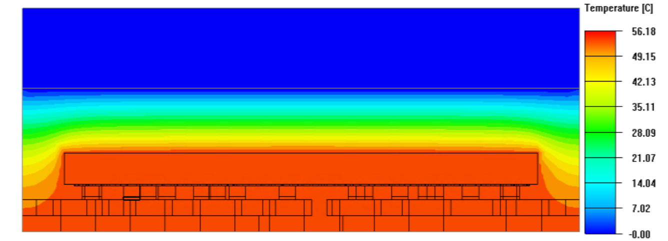


Theta JC_TOP (Junction-to-Case Top)

$R_{\theta JC_TOP} = (T_J - T_C) / P_H$

T_J = 56.2°C, T_{C_TOP} = 0°C

$R_{\theta JC_TOP}$ = 37.5°C/W

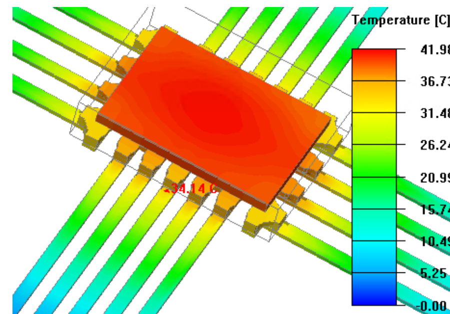


Theta JB (Junction-to-Coard)

$R_{\theta JB} = (T_J - T_B) / P_H$

T_J = 42°C, T_A = 34.1°C

$R_{\theta JB}$ = 5.3°C/W

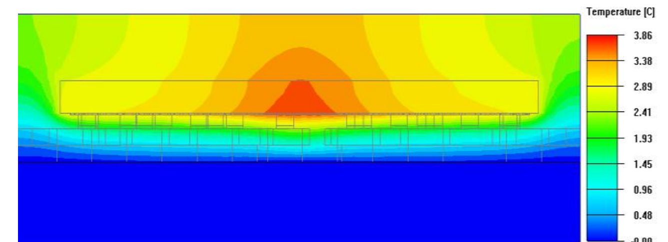


Theta JC_BOT (Junction-to-Case Bottom)

$R_{\theta JC_BOT} = (T_J - T_C) / P_H$

T_J = 3.9°C, T_{C_BOT} = 0°C

$R_{\theta JA}$ = 2.6°C/W



	$R_{\theta JA}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JB}$	$R_{\theta JC_TOP}$	$R_{\theta JC_BOT}$	
MPQ6612A	44.3	1.1	5.1	5.3	37.5	2.6	(°C/W)

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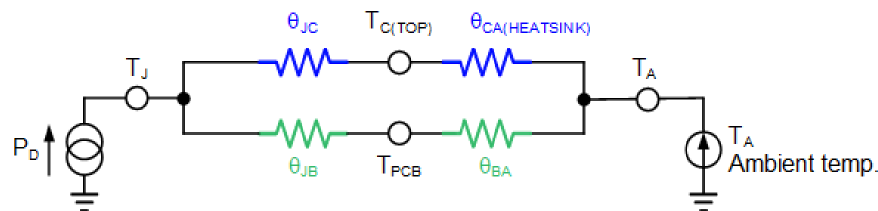
How To Use Thermal Resistance Parameters

- θ_{JA}: Thermal resistance of the entire system from the die to the ambient air. It is a measure of the device's ability to dissipate heat into the ambient air via all heat transfer paths, the sum of copper tracks, vias, and air convention conditions.

- θ_{JB}: Thermal resistance from the die to the board. θ_{JB} includes some of the board characteristics and their coupling with the package.

- $\theta_{JC(TOP)}$: Thermal resistance from the die (junction) to the top of the package.

- θ_{CA} or θ_{BA}: Thermal resistance of convection from the surface to ambient air.



- Ψ_{JB}: Characteristic thermal resistance allowing system designers to calculate the device's junction temperature based on a board temperature measurement. The Ψ_{JB} metric should be close to θ_{JB}, as the PCB dissipates most of the heat of the device.

$$T_J = T_{PCB} + (\Psi_{JB} \times P_D)$$

- Ψ_{JT}: Characteristic thermal resistance reflecting the temperature difference between the die (junction) and the top of the package. Ψ_{JT} is not a true thermal resistance, as the heat flowing from the die to the top of the package is unknown (but assumed to be the total power of the device). This assumption is clearly not valid, but when calculated this way, Ψ_{JT} becomes a very useful number as its characteristics are much like the application environment of the IC package.

$$\Psi_{JT} = \frac{T_J - T_C}{P_D}$$

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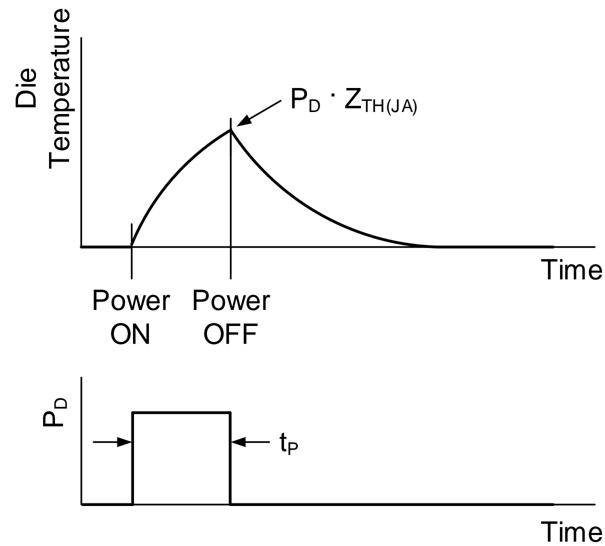
Pulsed Operation

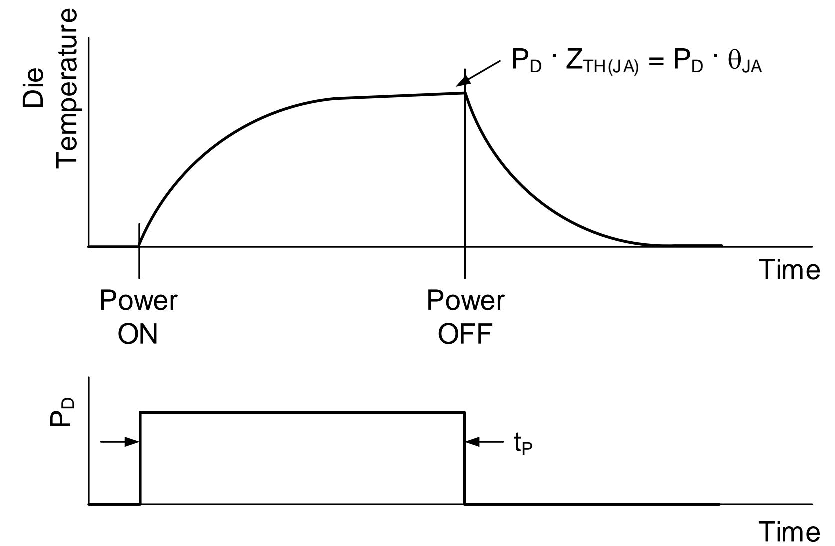
When a motor driver is subjected to a pulsed load, higher peak power dissipation must be tolerable. The materials in power packages have a definite thermal capacity; thus the critical junction temperature is not reached instantaneously, even when excessive power is being dissipated in the device.

Thermal capacitance (C_{TH}) is a measure of the capability to accumulate heat, like a capacitor accumulates a charge. For a given structural element, C_{TH} depends on the specific heat capacity (c), volume (V), and density (ρ), according to the following relationship:

$$C_{TH} = c \cdot \rho \cdot V \quad \text{expressed in J/K}$$



Short Single-Pulse Power



Long Single-Pulse Power

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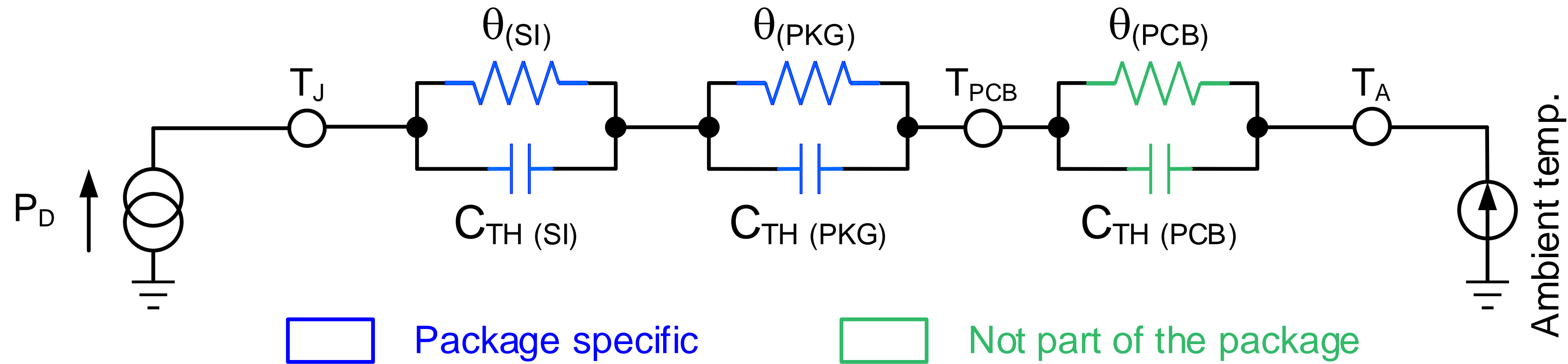
First Order Transient Thermal Model



The first cell represents the thermal characteristics of the silicon itself, and is characterized by the small volume with a correspondingly low thermal capacitance.

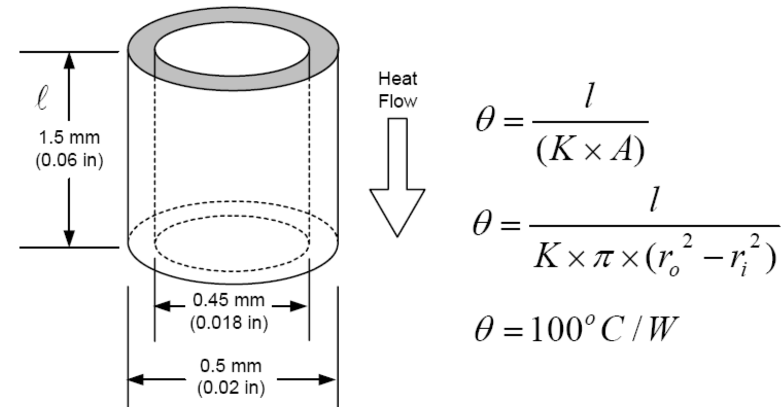
The second cell represents the package. The thermal resistance between the junction and the lead frame depends on die size and the interconnect type (wirebond or MeshConnect™). The thermal capacitance is typically small.

After the device itself has heated, convection and radiation to the ambient air starts. Depending on the PCB's thermal capacitance associated with this phase, it can represent anything from a purely resistive element (not desired) to a fairly large capacitance.

Thermally Enhanced PCB: Basic Rules

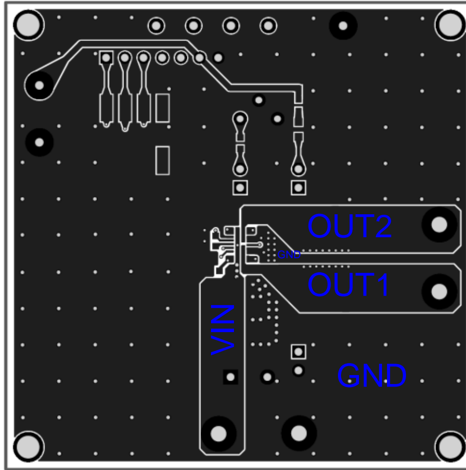
- Copper is nearly perfect in perpendicular direction — thickness is irrelevant!
- It is more efficient to conduct heat through the plane rather than along its length.
- Thicker copper layers improve the heat transfer along the PCB.
- FR4 is a poor conductor along the length of the plane’s layer.
- Multiple thermal vias should be used to conduct heat through the PCB.

Use thick layers of copper
Use thin layers of FR4

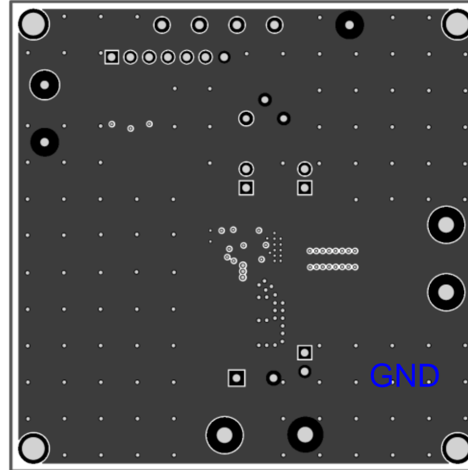


A typical via has about 100°C/W thermal resistance

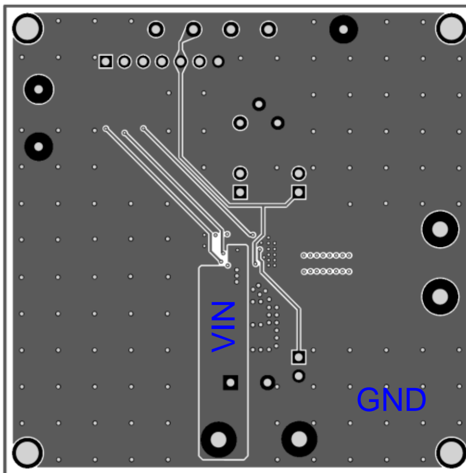
MPQ6612: 4-Layer Evaluation Board



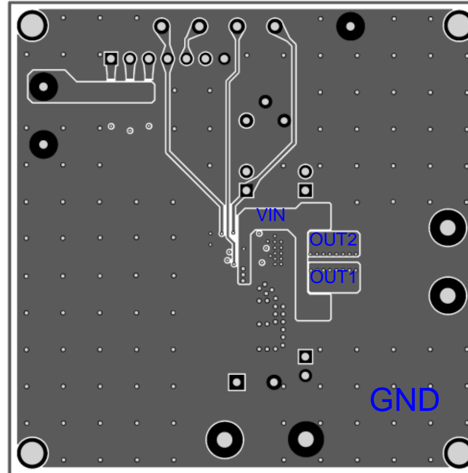
Top Layer



Mid-Layer 1



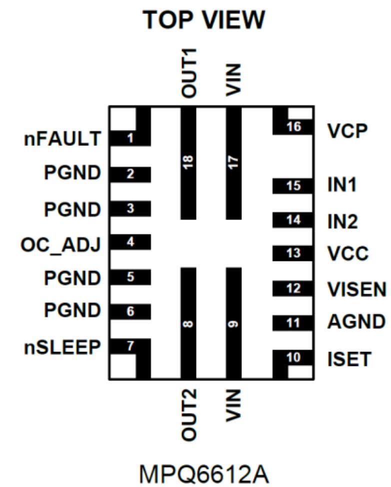
Mid-Layer 2



Bottom Layer

PCB Characteristics:

- 4-layer board (63.5mmx63.5mm)
- 70μm copper on all layers
- 1.6mm total thickness



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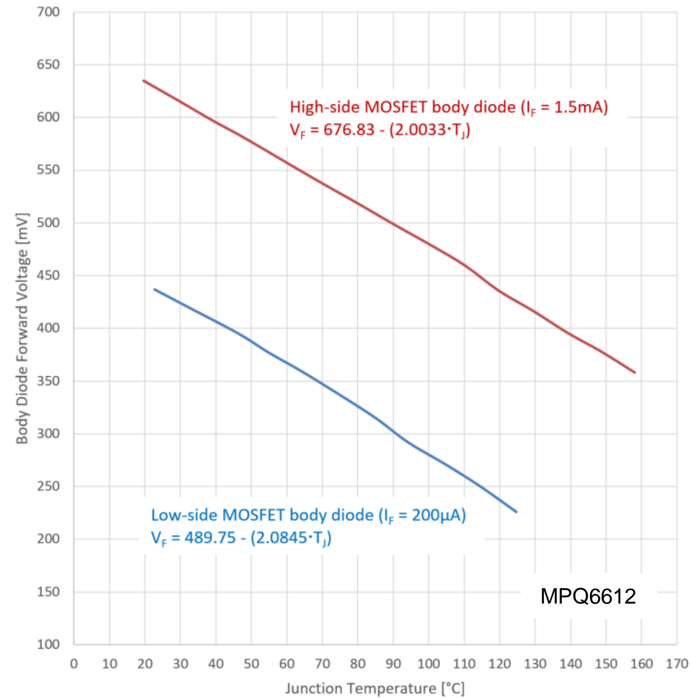
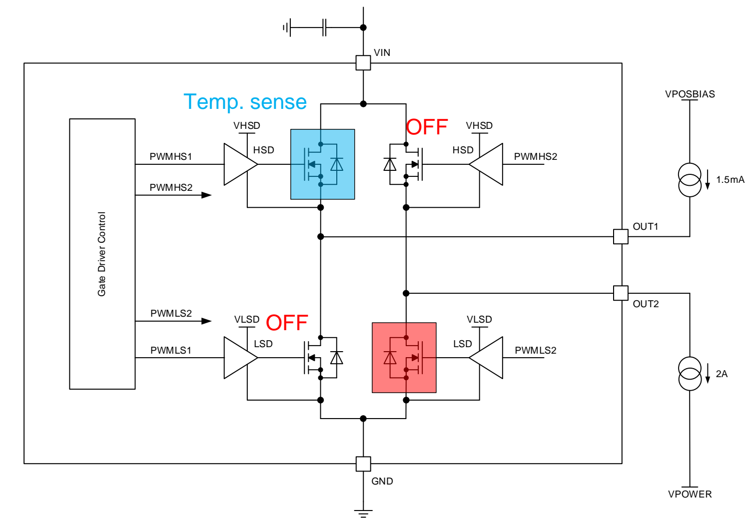
Monitoring IC Junction Temperature

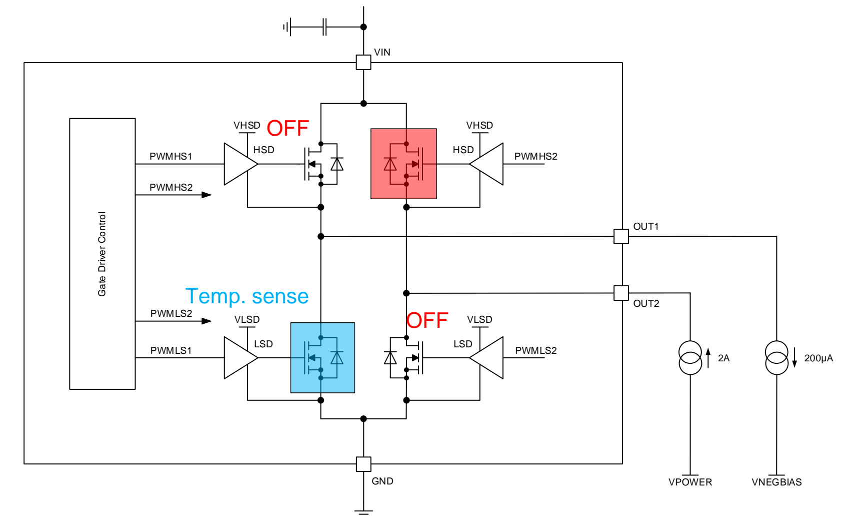
One method to measure the temperature of the power FETs is to employ the junction itself as a temperature sensor, since there is a strong correlation between the forward voltage drop of a junction and the temperature of that junction.



Body Diode Voltage vs. Junction Temperature

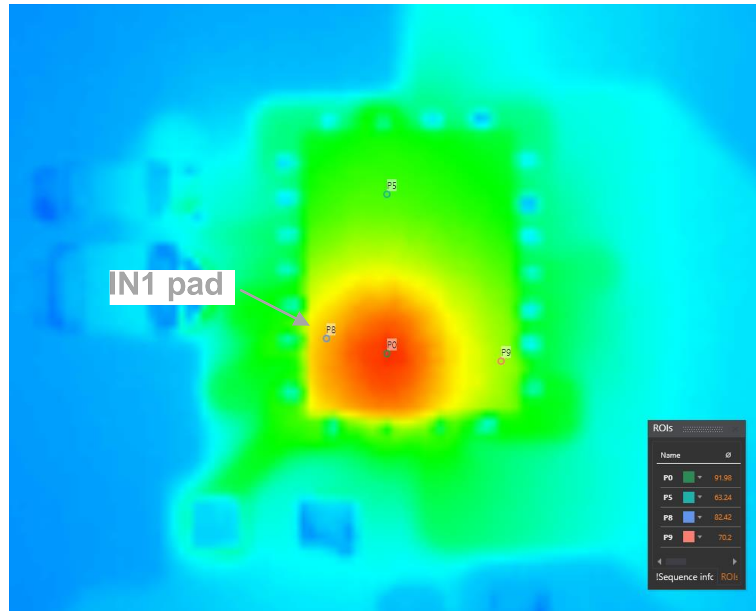


HS-FET Temperature Measurement

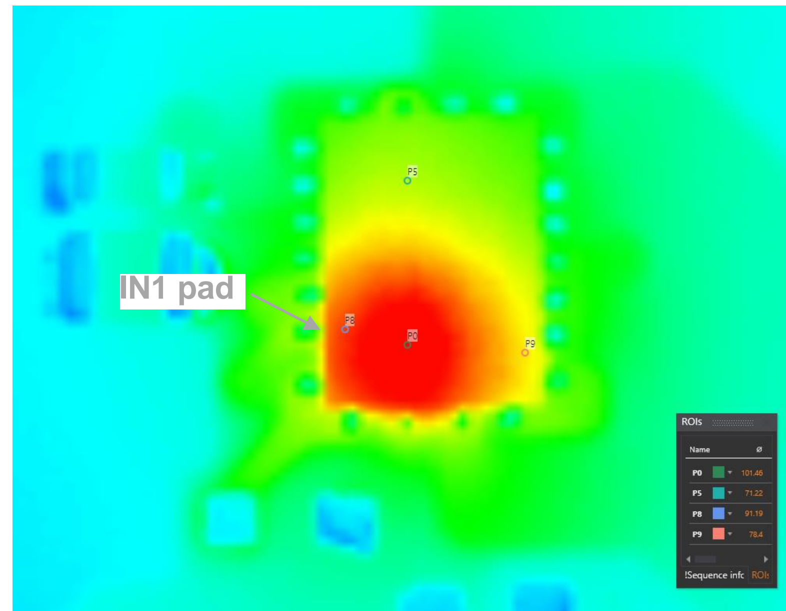


LS-FET Temperature Measurement

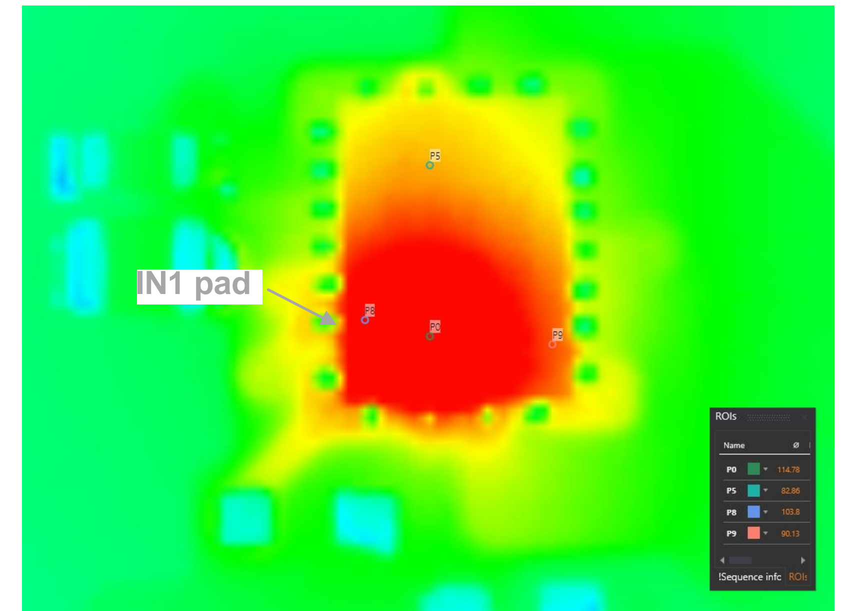
Monitoring IC Junction Temperature (contd.)



Output 1 (3.3W, t = 10s)



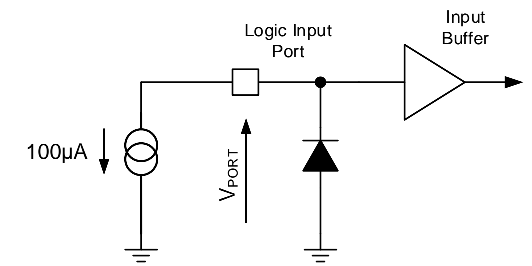
Output 1 (3.3W, t = 60s)



Output 1 (3.3W, t = 1000s)

Temperature gradient across the power stage (ca. 2000µm): ca. 30°C

Temperature gradient power stage to I/O pad: ca. 10°C



Note: A 10°C temperature offset translates to about a 10% to 20% measurement error (too optimistic).

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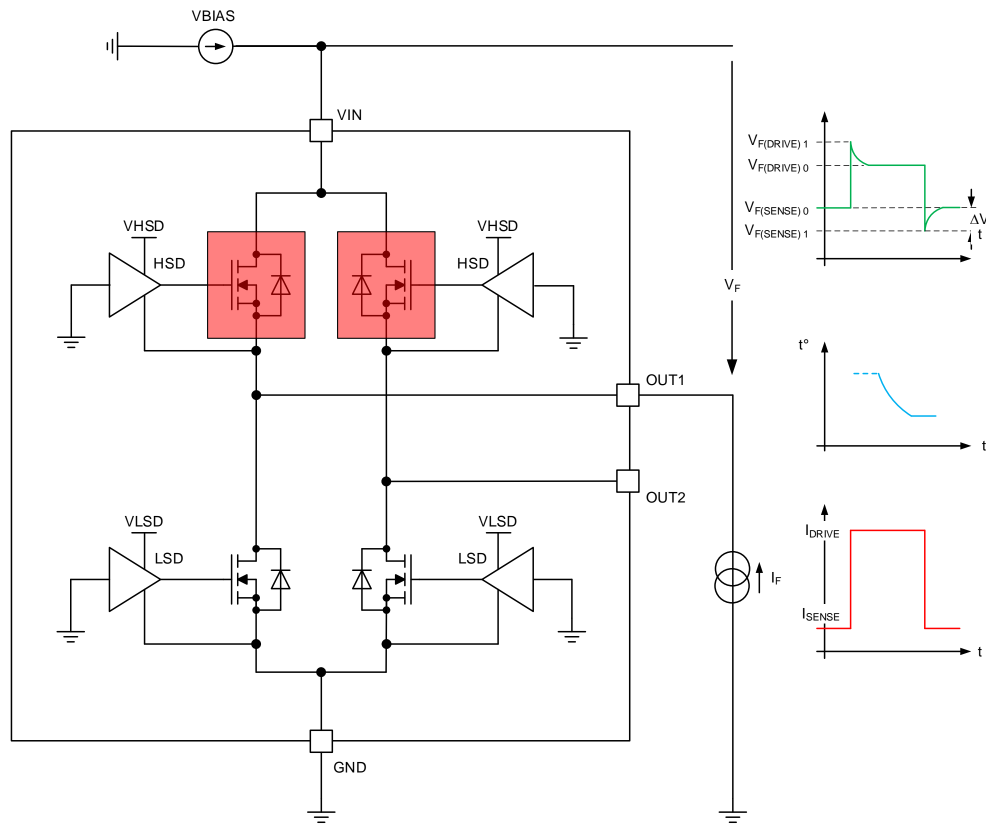
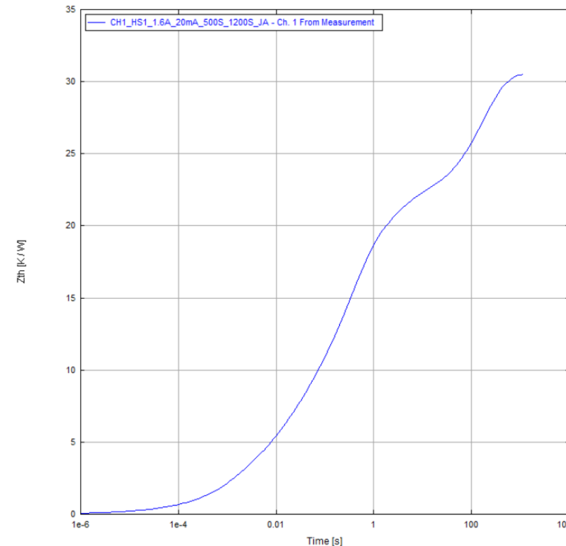
Characteristic Thermal Impedance

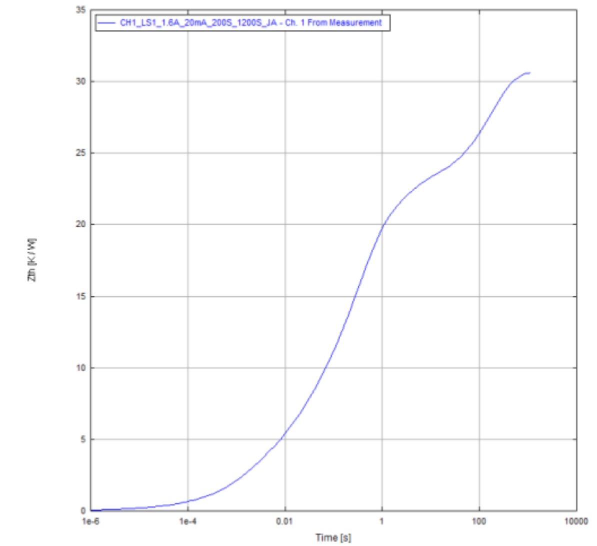
The transient thermal impedance is measured using the same MOSFET body diode for heating and monitoring the temperature. A pulsed current (I_{SENSE}, I_{DRIVE}) is applied to the device. The change in the diode's forward voltage is monitored before and after the pulse.

$$Z_{TH(JA)} = \frac{T_J - T_A}{P_D}$$





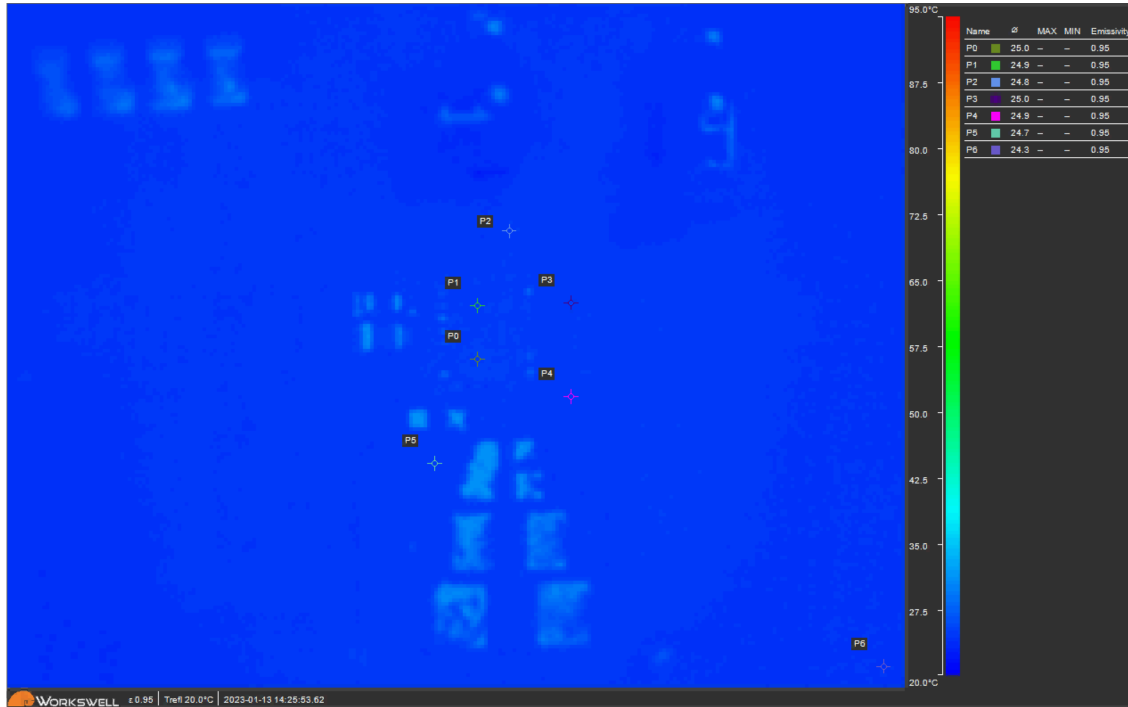
Thermal Impedance (θ_{JA})
Output 1 High-Side Diode



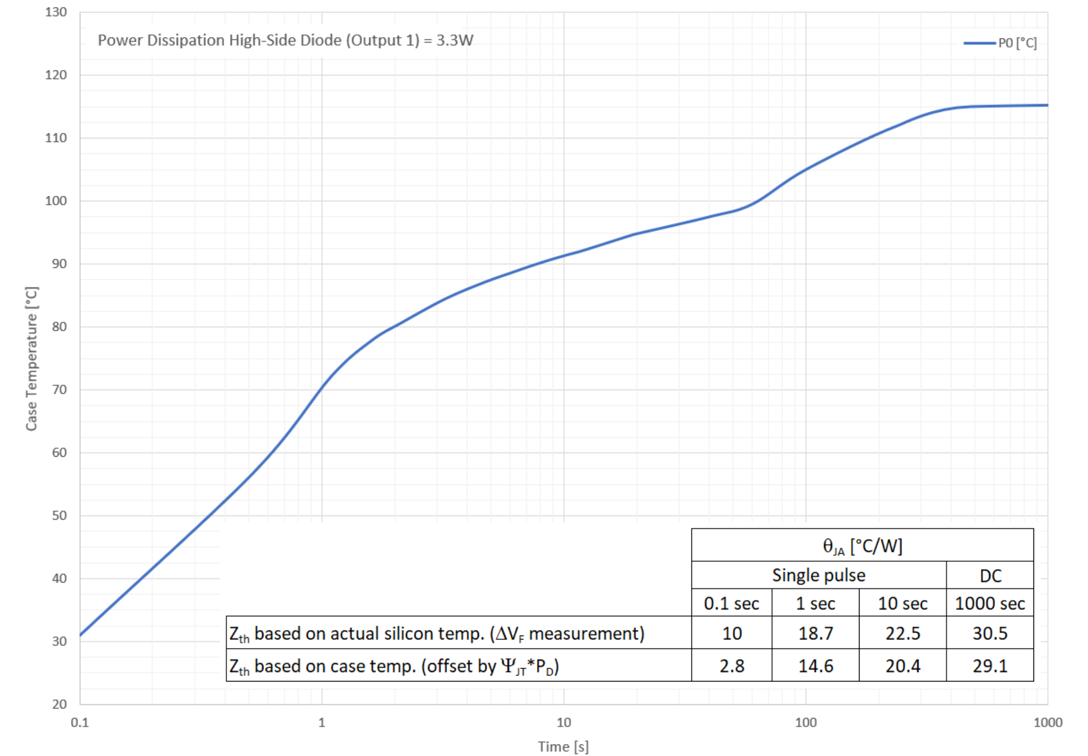
Thermal Impedance (θ_{JA})
Output 2 High-Side Diode

Measurement equipment: Mentor Graphics T3Ster thermal transient tester

High-Side Diode Output 1 Power Dissipation (EVQ6612A-L-00A)



Single-Pulse (20s) Thermal Response (Heating, Cooling)



	θ_{JA} [°C/W]			
	Single pulse			DC
	0.1 sec	1 sec	10 sec	1000 sec
Z_{th} based on actual silicon temp. (ΔV_F measurement)	10	18.7	22.5	30.5
Z_{th} based on case temp. (offset by Ψ_{JT}*P_D)	2.8	14.6	20.4	29.1

Time [ms]	PSI_JT [K/W]
0.1	0.73
1	2.13
10	5.31
100	7.78
1000	3.83
10000	2.1
100000	1.7
1000000	1.51

- Large thermal gradient over the chip area
- The junction temperature can be estimated accurately based on a package case temperature measurements
- Thermal steady state is reached after several minutes

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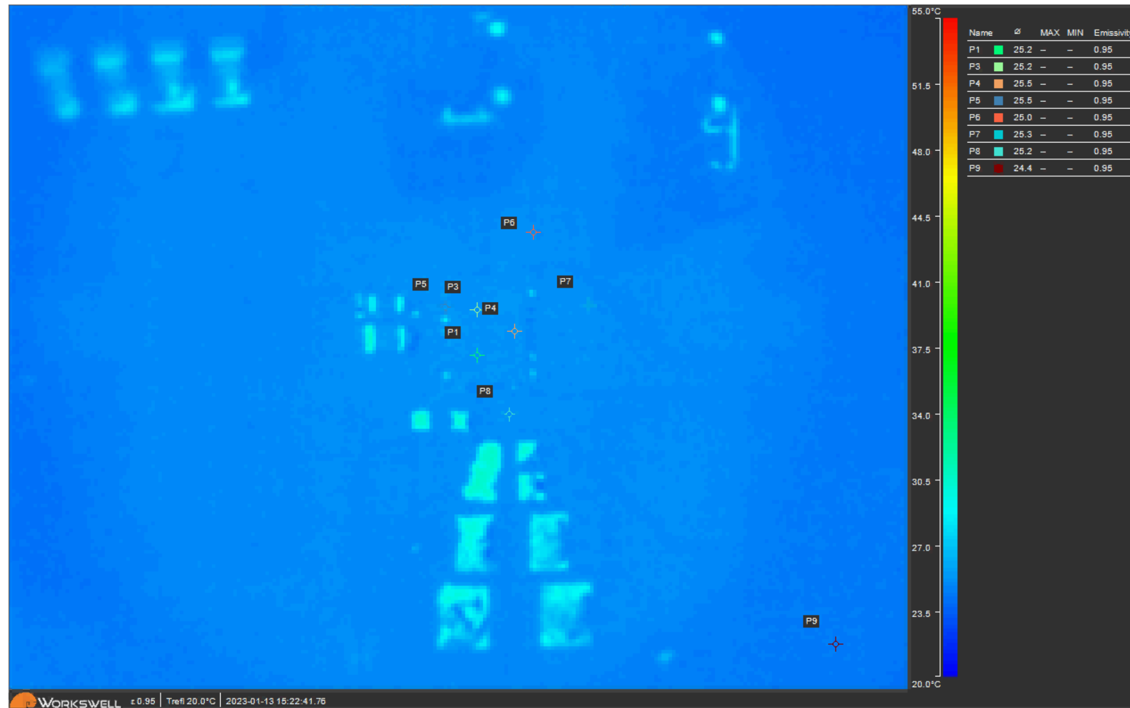
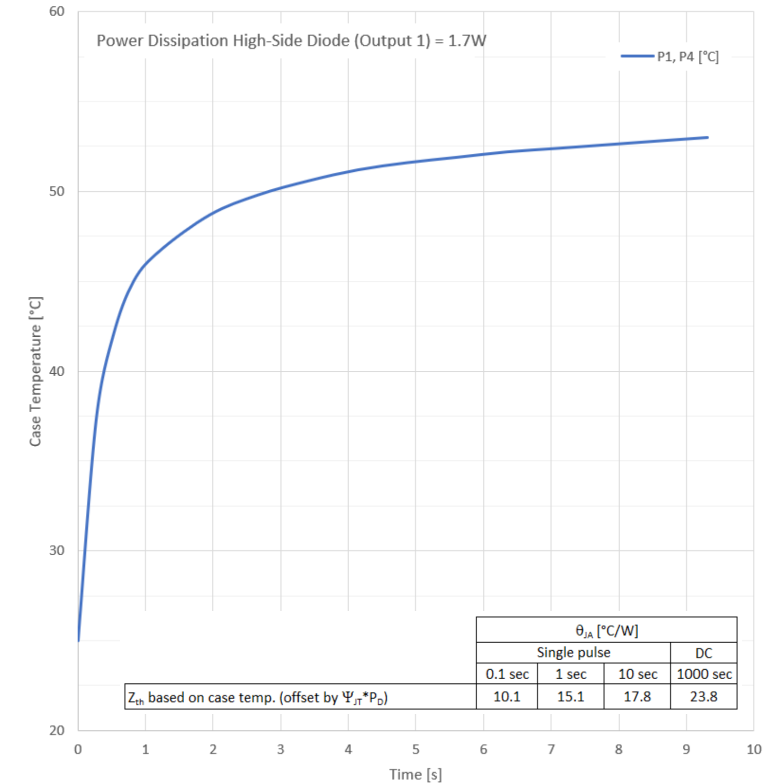
High-Side Diode Output 1+2 Power Dissipation (EVQ6612A-L-00A)



Single-Pulse (10s) Thermal Response (Heating, Cooling)



Time [ms]	PSI_JT [K/W]
0.1	0.35
1	1.06
10	2.76
100	5.06
1000	2.12
10000	0.88
100000	0.88
1000000	0.88

The IC's thermal performance is significantly better on an application board vs. a JEDEC board

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Conclusion

Maximize PCB Thermal Performance

- Consider using thick copper for high power designs
- Use multiple layers for ICs in small packages
- Make the PCB as thin as possible by reducing FR4 thickness
- Optimize top layer power trace design
- Use vias in power lines, placed as close as possible to the IC, to tie adjacent layers together
- The baseline temperature is a function of power dissipation and board area, not cooper thickness

In-Situ Thermal Performance Evaluation

- Be sure to sense temperature at the right location. The device may exhibit a large temperature gradient!
- The delta V_F temperature sensing technique, via an I/O port, is handy and is a reasonably accurate die temperature measurement
- The die temperature (thermal characteristic impedance) can also be estimated by measuring the device's case temperature, $T_J = T_C + (\Psi_{JT} \cdot P_D)$

MPS's Thermal Modeling Group Can Provide Additional Support

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COMPLEMENTARY MATERIAL

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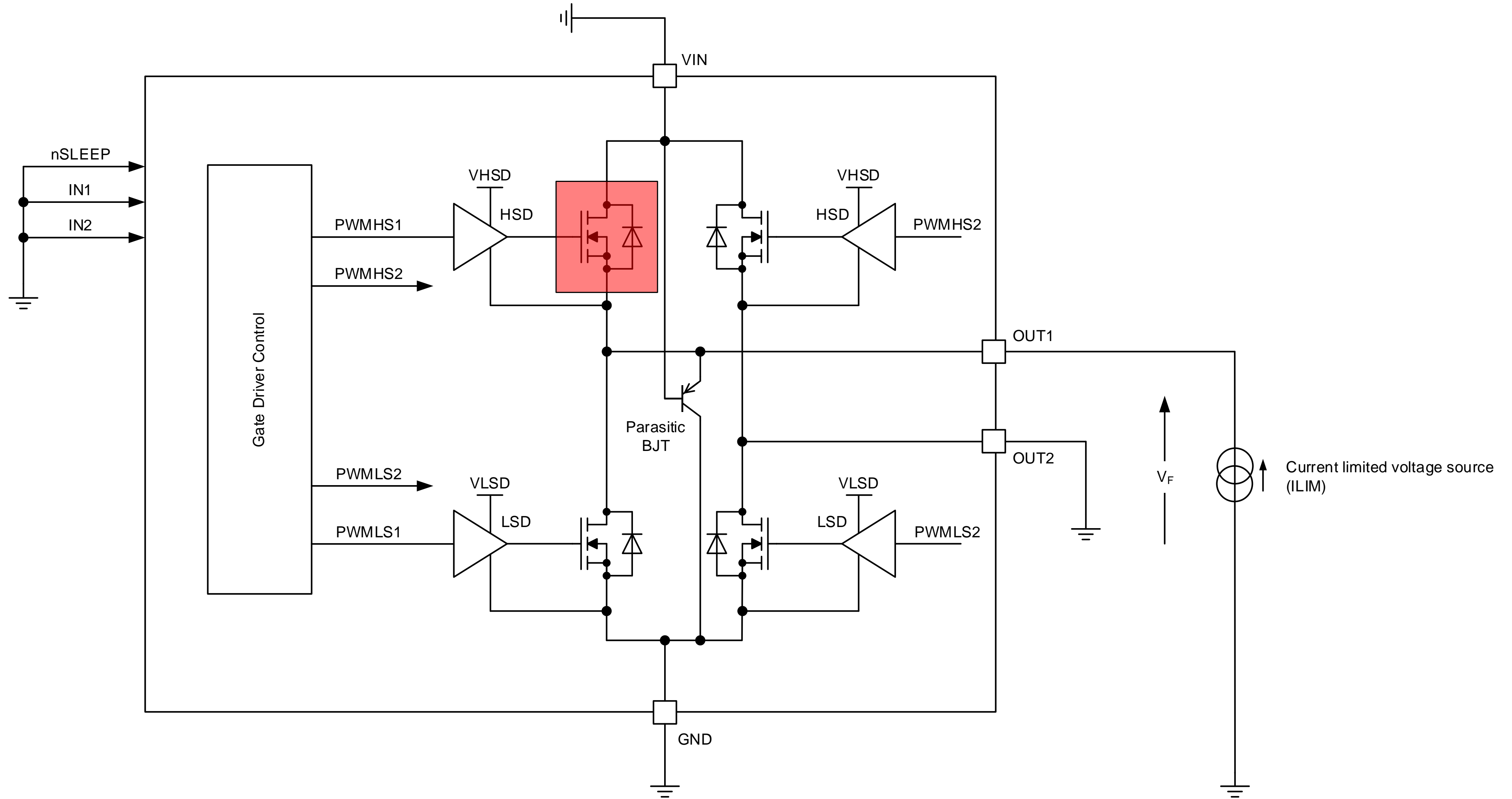
How to Generate Power Dissipation



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