

**Starts at 11AM PDT 8PM CEST Europe
2AM China CST 3AM Japan JST**

**No Compromise Needed:
Cost-Effective, 2-Layer PCBs Deliver Impressive
EMI and Thermal Performance**

March 2021

Ralf Ohmberger, Applications Engineer, MPS

All attendees are muted. Live QA available via chat.



Agenda

Motivation

4-Layer PCB vs. 2-Layer PCB

MPQ4323 – Compact, Low I_Q , 36V/3A, Sync Buck

MPQ4323 – Recommended Schematic

MPQ4323 – Recommended Layout

MPQ4323 – Recommended Placement

MPQ4323 – Recommended DC/DC Layout

MPQ4323 – Recommended Bottom Layer Layout

MPQ4323 – Recommended Filter Layout

MPQ4323 – Thermal Effect of Different Layouts

MPS's MPQ4323 vs. Competitors

EMC Results from Recommended Layout

Conclusions

Motivation

Increasing cost pressure has led to the reintroduction of 2-layer PCB designs, which are a cost-effective alternative to 4-layer PCB ECUs.

Strict EMC limits are difficult to meet in a 4-layer PCB, and are even more difficult to meet in a 2-layer PCB.

Operating T_{AMBIENT} requirements have reached $>100^{\circ}\text{C}$.

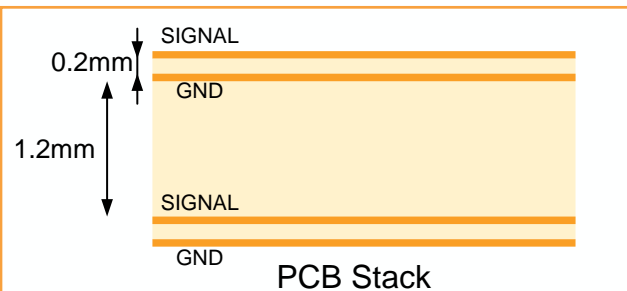
MPS conducted an experiment to determine the best 2-layer PCB layout for buck converters featuring the MPQ4323.



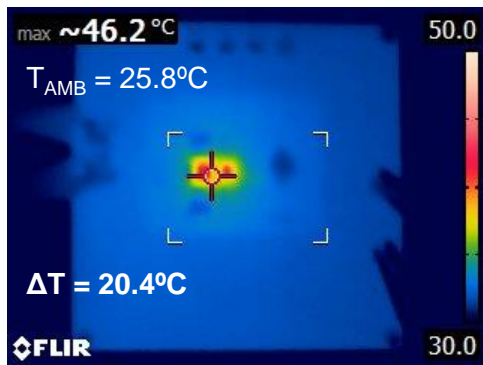
PCB Panel with 9 Different Layouts

4-Layer PCB vs. 2-Layer PCB

4-Layer

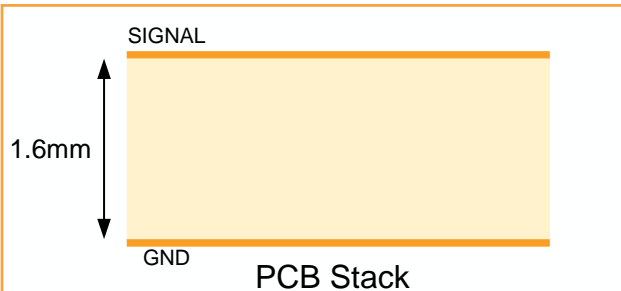


PCB Stack

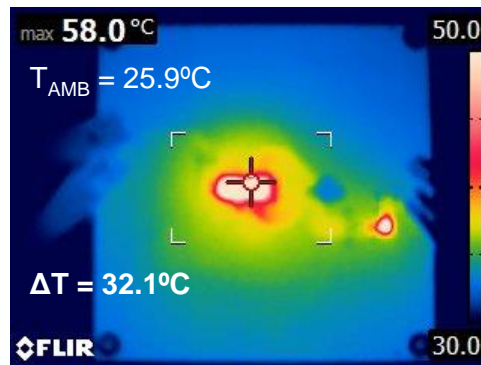


PCB Thermal Image*

2-Layer



PCB Stack



PCB Thermal Image*

The return path is 8 times longer in a 2-layer PCB.

The IC case temperature is 12°C higher with 2-layer PCBs.

*Conditions: $V_{\text{IN}} = 13.5\text{V}$, $V_{\text{OUT}} = 5\text{V}$, $I_{\text{OUT}} = 3\text{A}$, $f_{\text{SW}} = 430\text{kHz}$, 2-hour runtime.

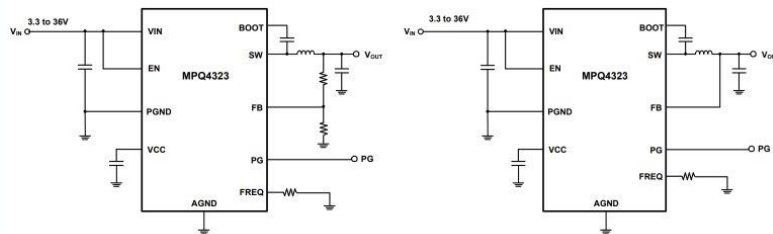
MPQ4323 – Compact, Low I_Q , 36V/3A, Sync Buck

Features:

- Wide 3.3V to 36V Operating Voltage Range
- Supports 42V Load Dump, Cold Crank as Low as 3V
- **MPQ432x: Family of Pin-to-Pin Parts Covers 0.5A to 4A Applications**
- **20 μ A Input Current under No-Load Conditions**
- **Up to 96% Peak Efficiency**
- 350kHz to 2.5MHz Configurable Switching Frequency
- Adjustable Output Voltage
- Fixed-Output Versions: 1V, 1.1V, 1.8V, 2.5V, 3.0V, 3.3V, 3.8V, or 5V
- **Frequency Spread Spectrum for Low EMI**
- **Symmetric V_{IN} for Low EMI**
- Accurate Power Good/RESET Monitors for Over-Voltage and Under-Voltage Conditions
- AAM or Forced CCM Versions
- **250mV Low-Dropout at 2A**
- Available in a Compact QFN (2mmx3mm) Package with Wettable Flanks

Applications:

- Automotive Infotainment, Clusters
- Advanced Driver Assistance Systems (ADAS)
- Industrial Power Systems

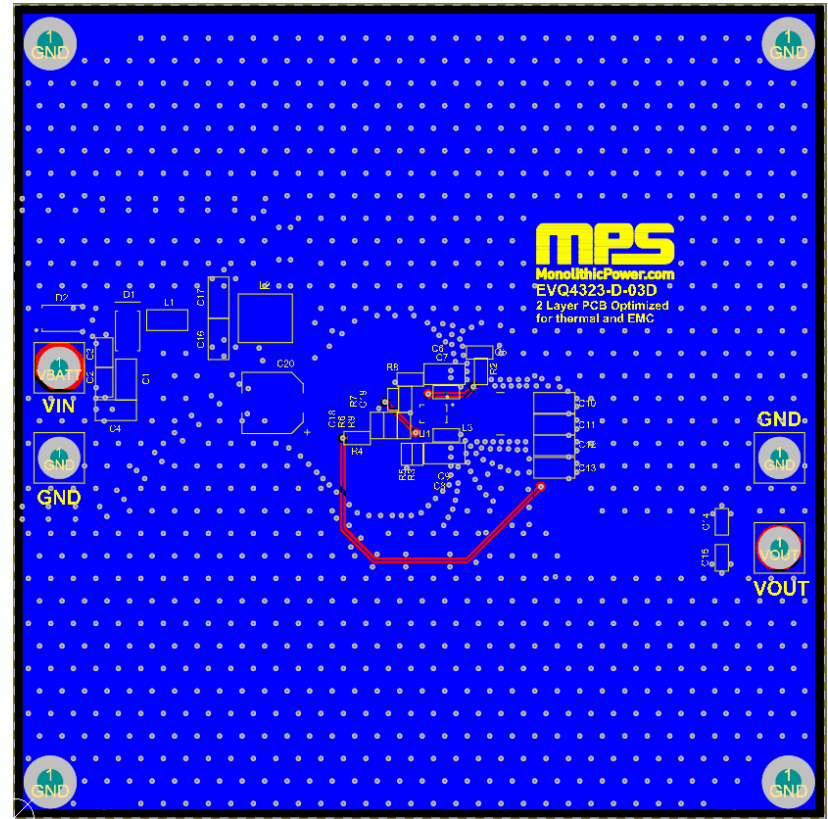
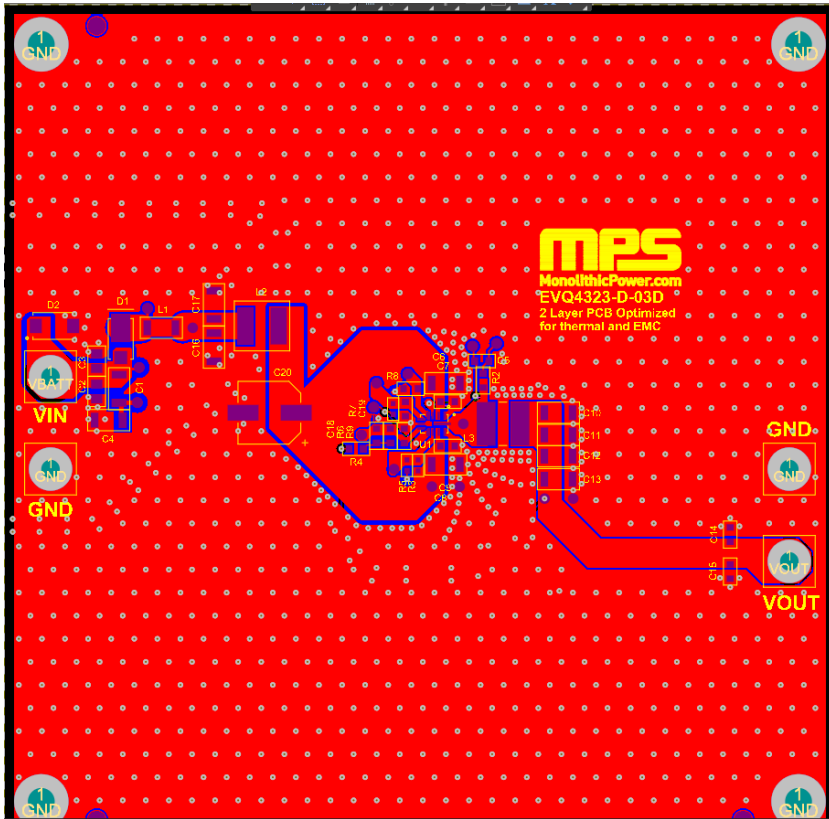


Output Adjustable Version

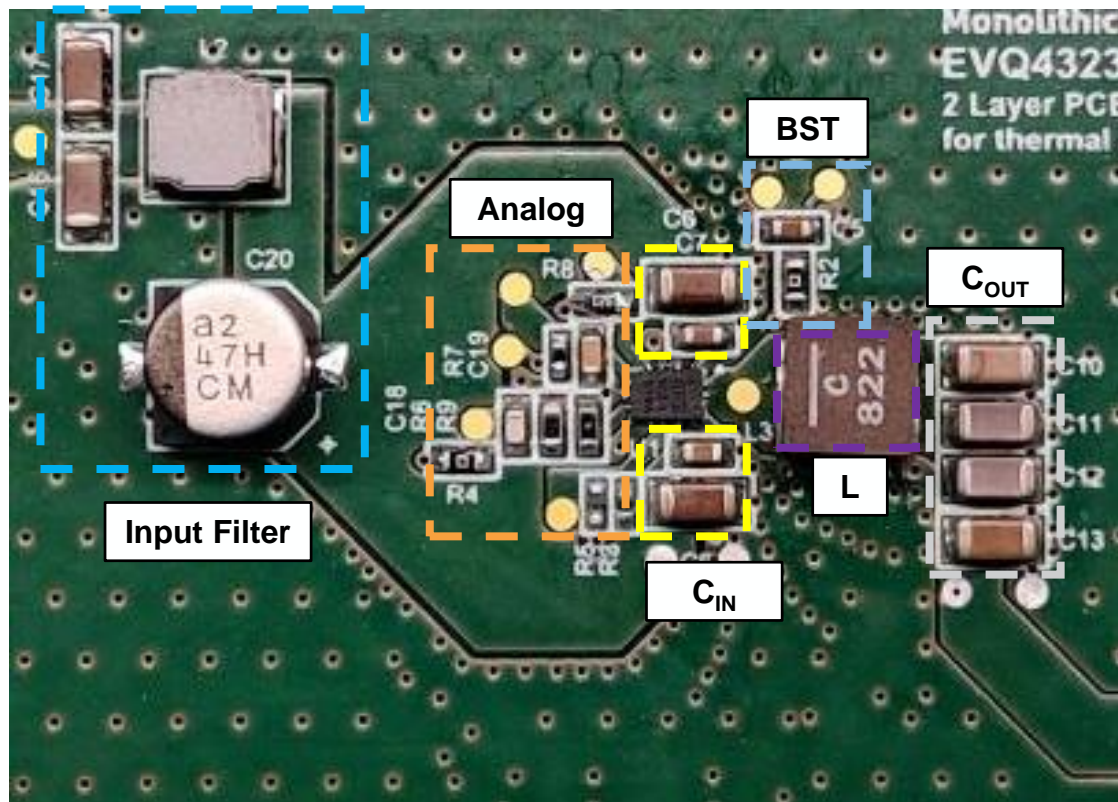
Output Fixed Version

Key Specifications	
Input Voltage	3.3V to 42V load dump
Output Voltage	Adjustable: 5V, 3.8V, 3.3V, or 2.5V
Switching Frequency	350kHz to 2.5MHz
HS-/LS-FET $R_{DS(ON)}$	65m Ω /45m Ω
Package	FCQFN-12 (2mmx3mm)

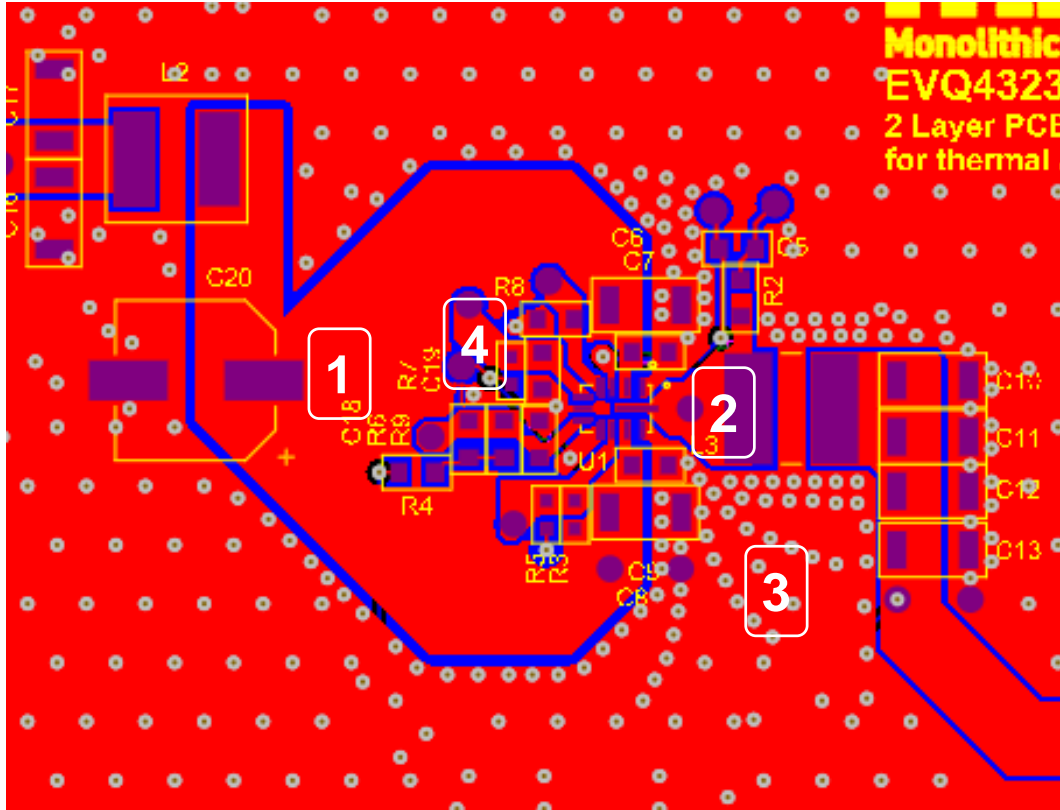
MPQ4323 – Recommended Layout



MPQ4323 – Recommended Placement

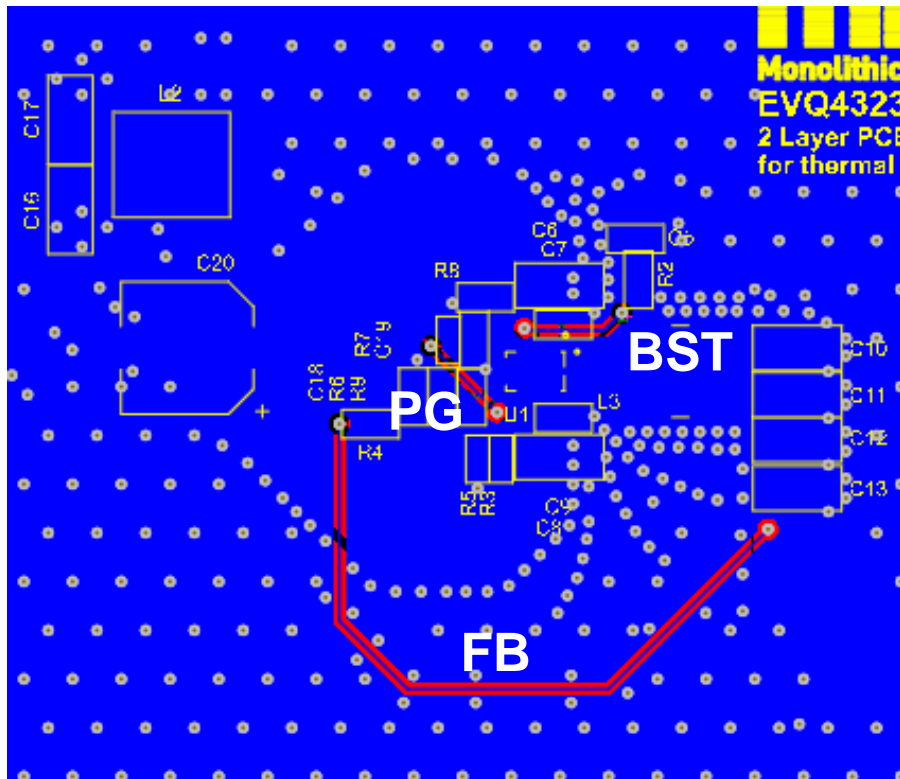


MPQ4323 – Recommended DC/DC Layout



1. Connect VIN to a wide copper polygon to improve heat dissipation. Use a symmetrical VIN input, and wrap it around the analog signals.
2. Keep the SW node small, with just enough area to connect it to the inductor while adding a test point.
3. Connect PGND to a large plane. Avoid making any cuts around it. Place several vias on the bottom-side plane, especially near the inductor.
4. Connect the signal pins using wide traces to improve heat dissipation, as every mm^2 counts.

MPQ4323 – Recommended Bottom Layer Layout

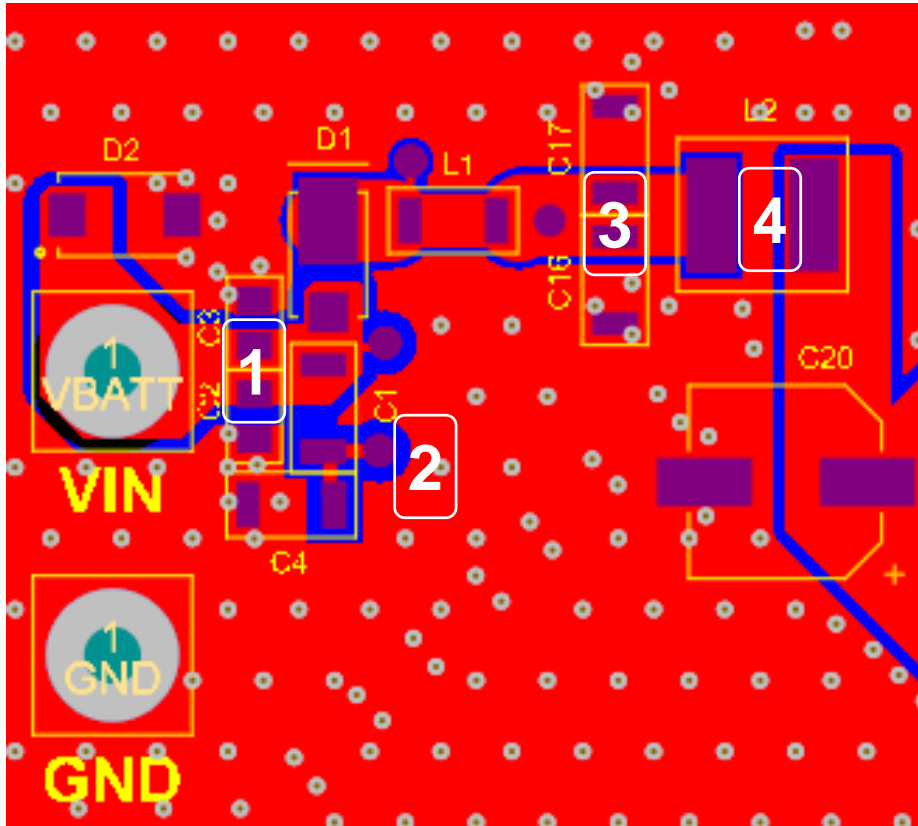


When possible, avoid routing signals in the bottom layer.

Route the FB trace on the bottom layer to avoid interrupting the VIN path. If the trace gets too long, it may be a good idea to alternate between bottom and top layers in a stitching pattern.

The FB resistors must be close to the IC, so that high frequency noise sees a low impedance in the long trace to C_{OUT} .

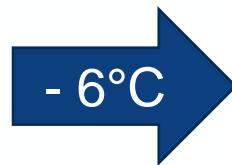
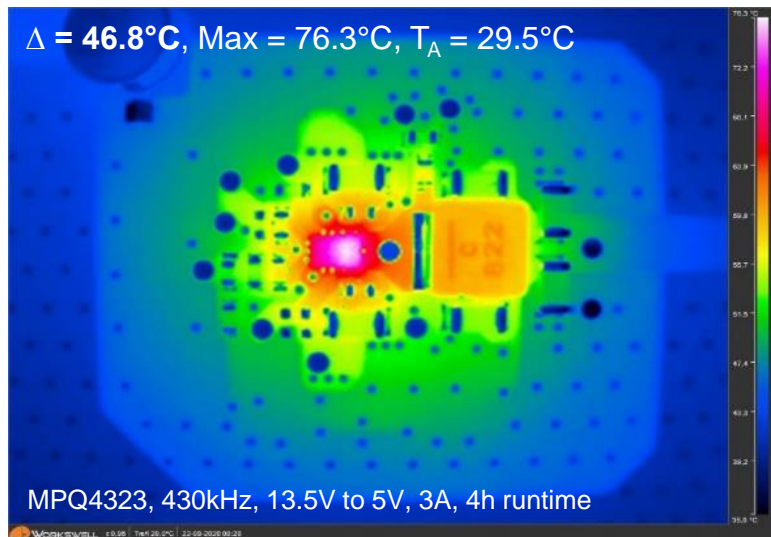
MPQ4323 – Recommended Filter Layout



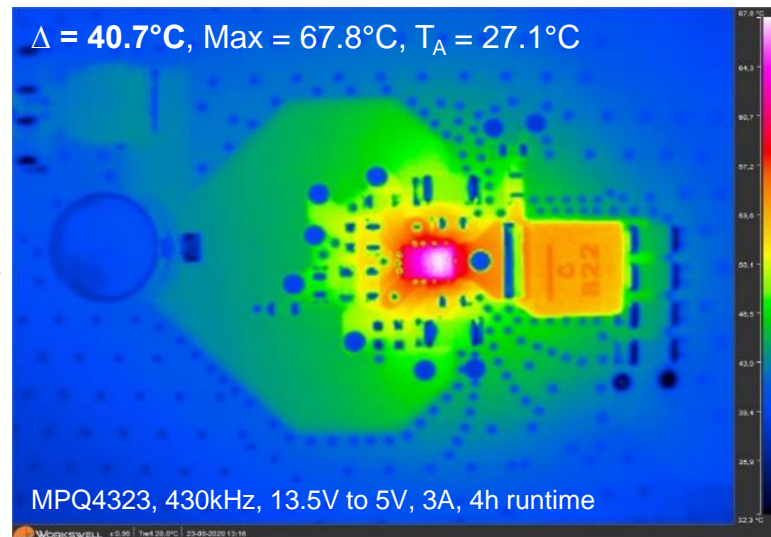
1. Place the small-value capacitors very close to the connector. This helps filter higher frequencies, and is key to passing EMC.
2. Use 2 capacitors in series (connected in a 90° orientation to one other) to avoid fire if one of the MLCCs cracks.
3. Place the higher-value capacitors close to the inductor in a symmetrical layout.
4. When looking from the DC/DC converter, the inductor should be the first component of the input filter. This prevents high-frequency noise from getting too close to the connector.

MPQ4323 – Thermal Effect of Different Layouts

Traditional



Recommended



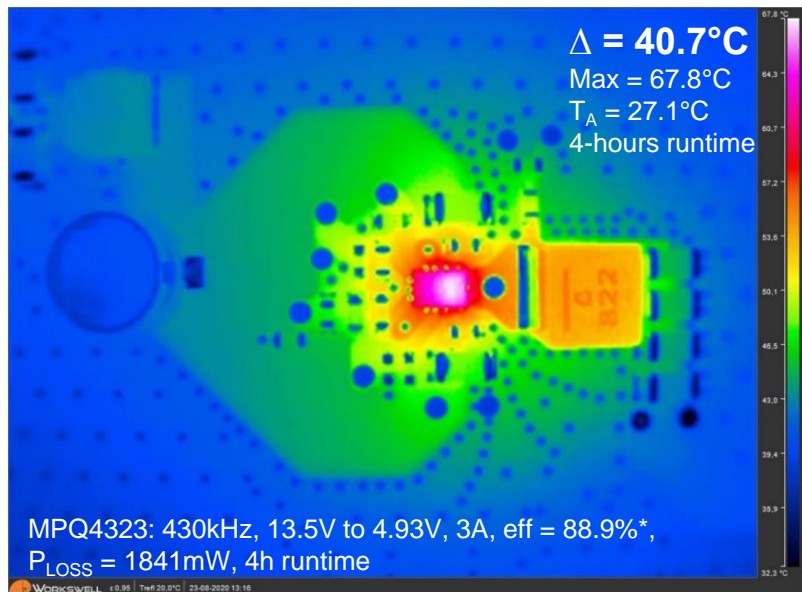
A traditional layout has a cut in GND around the DC/DC converter, and VIN is connected on the bottom layer with a Y shape.

The new, recommended layout has a large VIN polygon to extract heat, as well as a solid GND plane. It also has many more vias connecting the top and bottom.

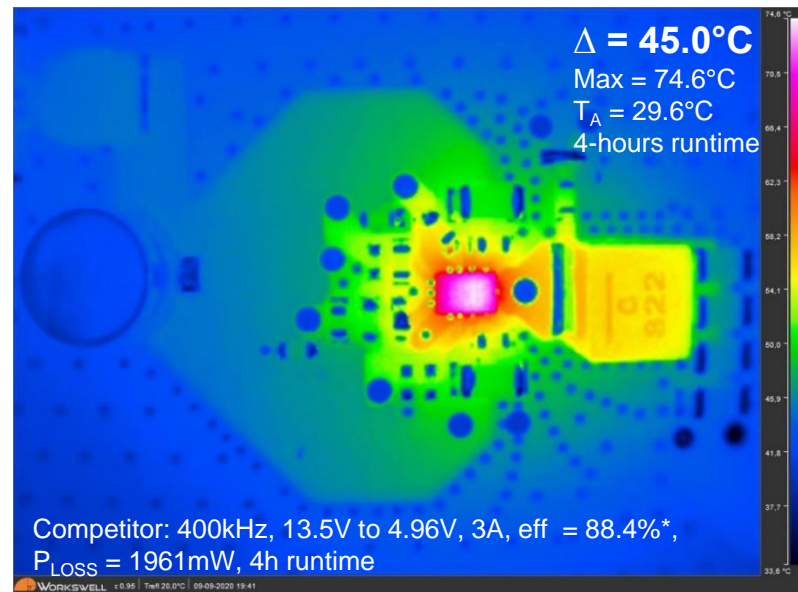
MPS's MPQ4323 vs. Competitors

The MPQ4323 is >4°C cooler. The observed difference was consistent when tested using a variety of PCBs.

MPQ4323

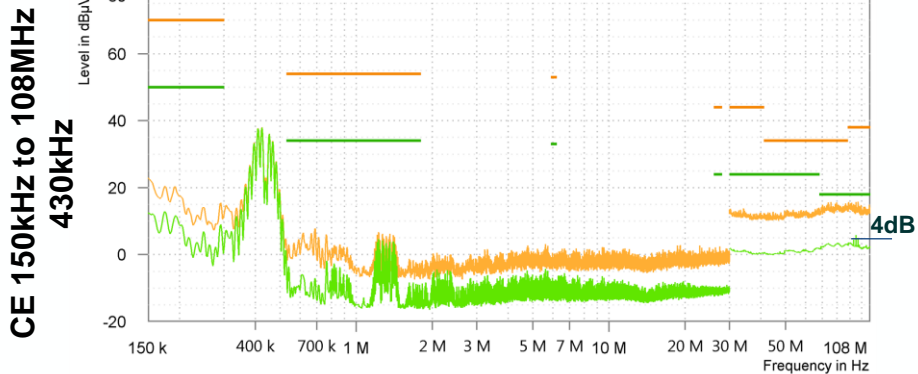


Competitor's Part

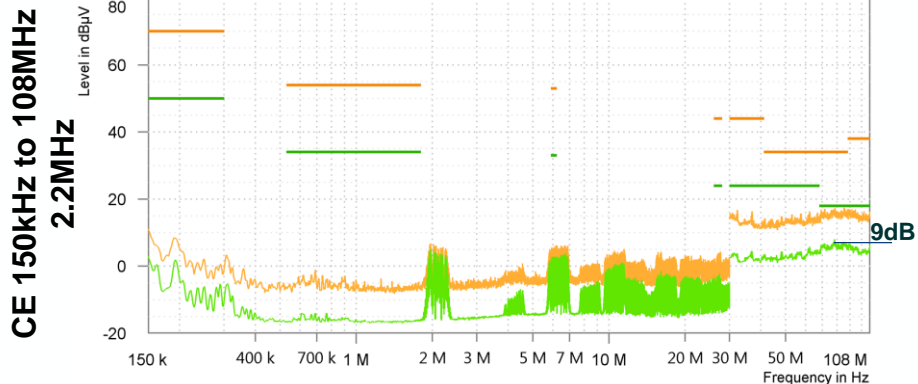


*The efficiency measurement includes the input filter, protection diode, and power inductor losses.

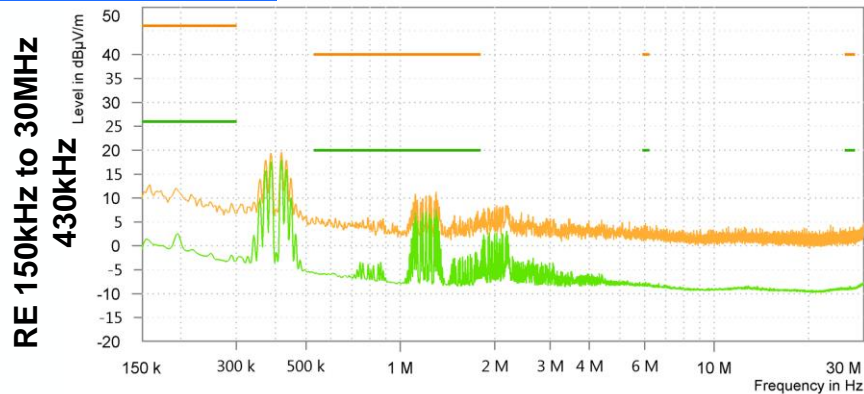
EMC Results from Recommended Layout



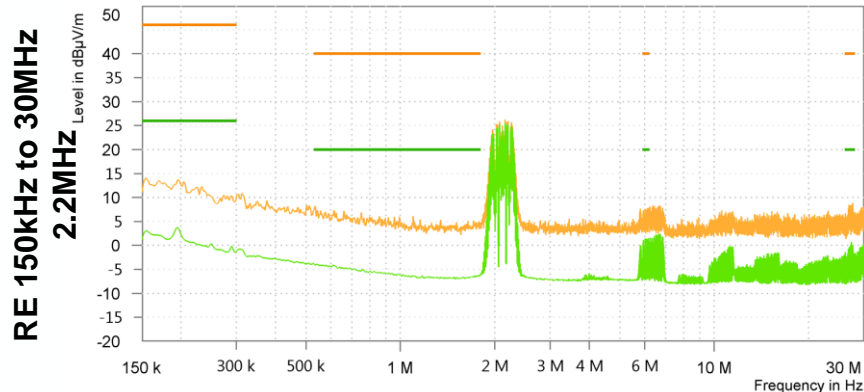
~ AVG Level @Spectrum Overview
~ PK+ Level @Spectrum Overview
~ AVG Limit @CE(150kHz-108MHz) CISRP25 Class5
~ PK+ Limit @CE(150kHz-108MHz) CISRP25 Class5



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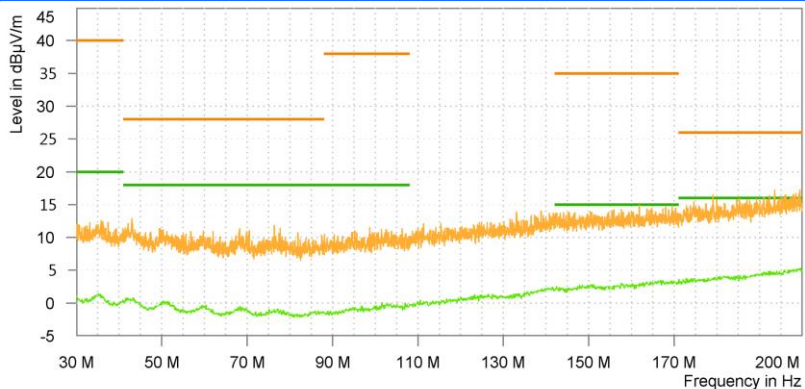
~ AVG Level @Spectrum Overview
~ PK+ Level @Spectrum Overview
~ AVG Limit @RE(150kHz-30MHz) CISRP25 Class5
~ PK+ Limit @RE(150kHz-30MHz) CISRP25 Class5



~ AVG Level @Spectrum Overview
~ PK+ Level @Spectrum Overview
~ AVG Limit @RE(150kHz-30MHz) CISRP25 Class5
~ PK+ Limit @RE(150kHz-30MHz) CISRP25 Class5

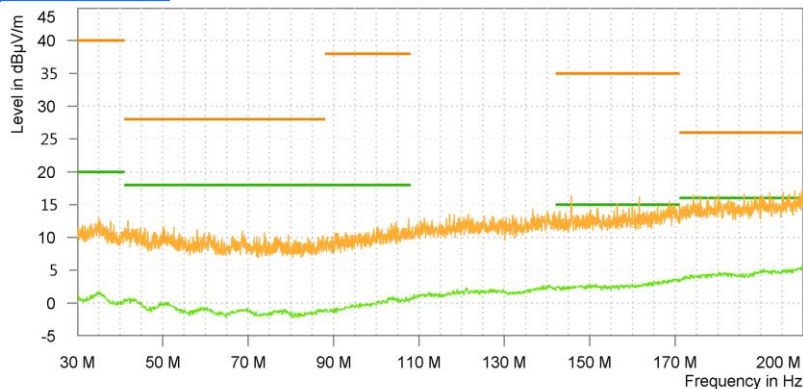
EMC Results from Recommended Layout

RE H 30MHz to 200MHz
430kHz



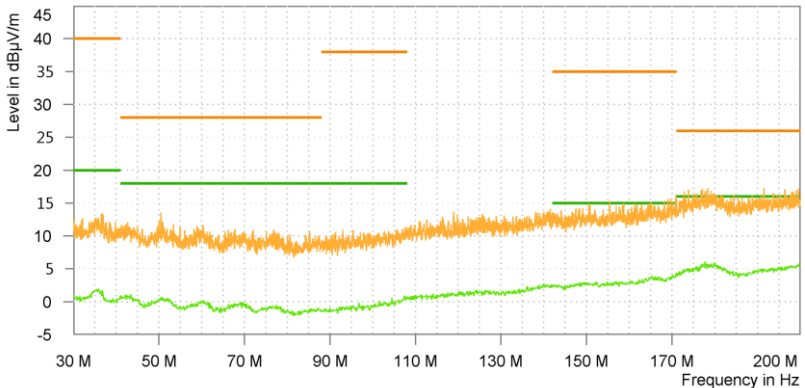
~ AVG Level @Spectrum Overview
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~ AVG Limit @RE(30MHz-200MHz) CISPR25 Class
~ PK+ Limit @RE(30MHz-200MHz) CISPR25 Class

RE V 30MHz to 200MHz
430kHz



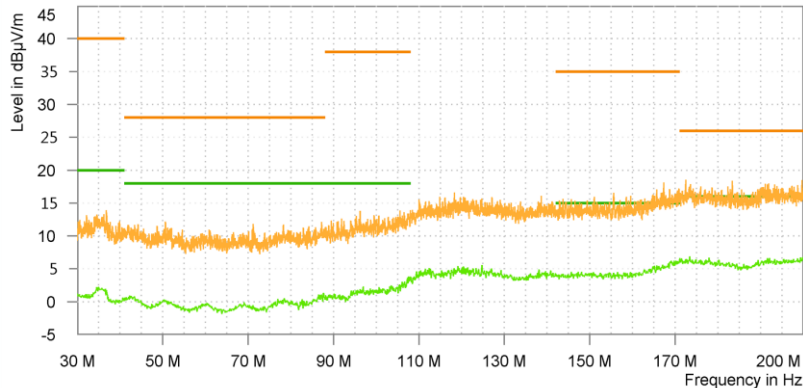
~ AVG Level @Spectrum Overview
~ PK+ Level @Spectrum Overview
~ AVG Limit @RE(30MHz-200MHz) CISPR25 Class
~ PK+ Limit @RE(30MHz-200MHz) CISPR25 Class

RE H 30MHz to 200MHz
2.2MHz



~ AVG Level @Spectrum Overview
~ PK+ Level @Spectrum Overview
~ AVG Limit @RE(30MHz-200MHz) CISPR25 Class
~ PK+ Limit @RE(30MHz-200MHz) CISPR25 Class

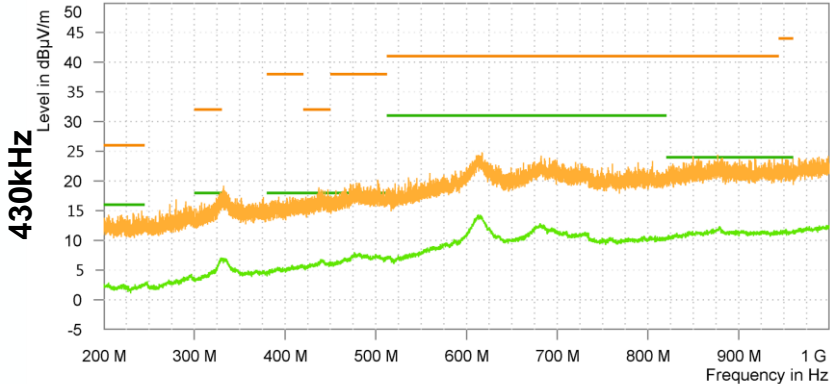
RE V 30MHz to 200MHz
2.2MHz



~ AVG Level @Spectrum Overview
~ PK+ Level @Spectrum Overview
~ AVG Limit @RE(30MHz-200MHz) CISPR25 Class
~ PK+ Limit @RE(30MHz-200MHz) CISPR25 Class

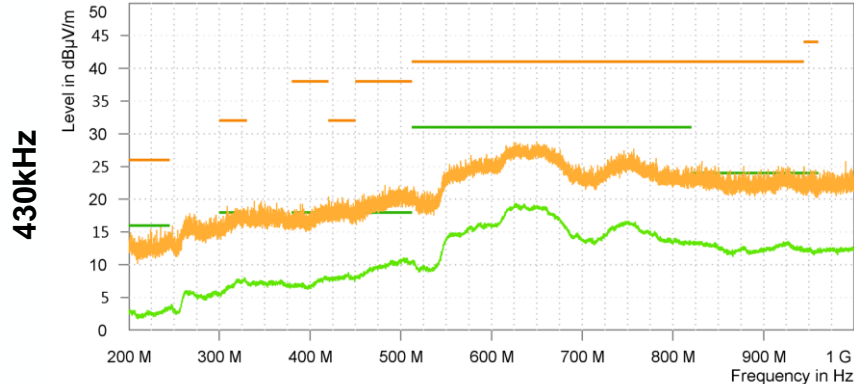
EMC Results from Recommended Layout

RE H 200MHz to 1GHz



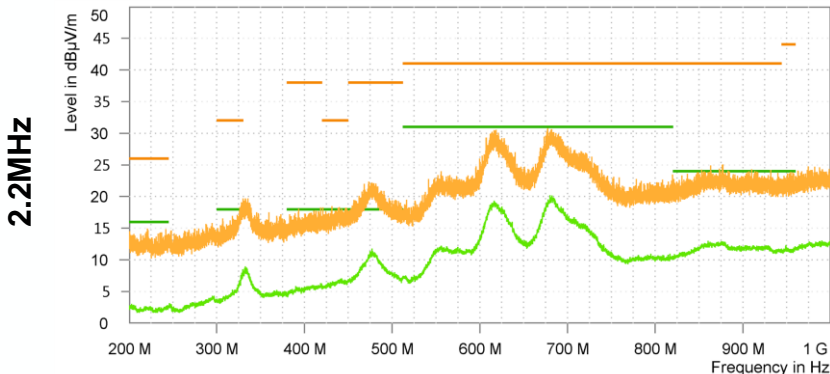
~ AVG Level @Spectrum Overview ~ AVG Limit @RE(200MHz-1GHz) CISRP25 Class
~ PK+ Level @Spectrum Overview ~ PK+ Limit @RE(200MHz-1GHz) CISRP25 Class

RE V 200MHz to 1GHz



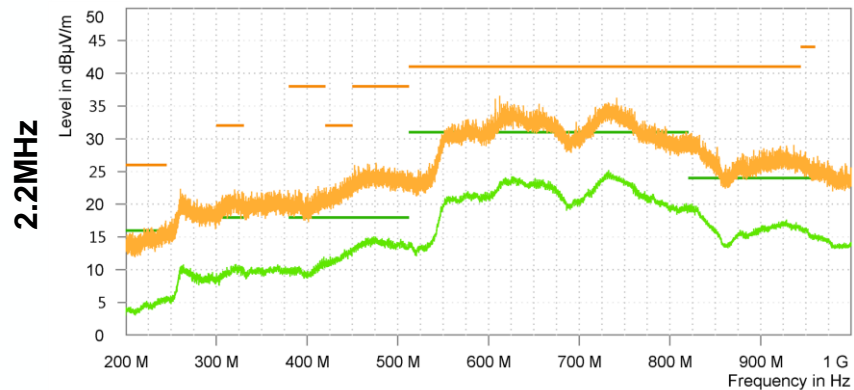
~ AVG Level @Spectrum Overview ~ AVG Limit @RE(200MHz-1GHz) CISRP25 Class
~ PK+ Level @Spectrum Overview ~ PK+ Limit @RE(200MHz-1GHz) CISRP25 Class

RE H 200MHz to 1GHz



~ AVG Level @Spectrum Overview ~ AVG Limit @RE(200MHz-1GHz) CISRP25 Class
~ PK+ Level @Spectrum Overview ~ PK+ Limit @RE(200MHz-1GHz) CISRP25 Class

RE V 200MHz to 1GHz



~ AVG Level @Spectrum Overview ~ AVG Limit @RE(200MHz-1GHz) CISRP25 Class
~ PK+ Level @Spectrum Overview ~ PK+ Limit @RE(200MHz-1GHz) CISRP25 Class

Conclusion

- The MPQ4323 allows cost-effective, 2-layer PCB designs to perform well in harsh environments.
- The IC can achieve close to full output operation in ambient temperatures that are approximately 100°C when operating at 400kHz, and approximately 80°C when operating at 2.2MHz*.
- The MPQ4323 is thermally superior to our direct competitor's part due to a larger bump connection to the lead frame and higher efficiency.
- A low-cost design can pass the EMI test with CISPR25 and OEM limits with sufficient margin. Customers' boards may have design constraints, but we are confident that these tests can be passed with the space-saving MPQ4323.

* When given a sufficient copper area for dissipation.

Q&A

Let us know your questions

For Customer Use Only

Thank You – Q&A

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