# Motor Drivers: Thermal Management

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# Agenda

- Introduction to the thermal theory and definitions

- JEDEC test setup review, Measurement methods and MPQ6612A thermal experimental results

- Transient thermal resistance, Zth

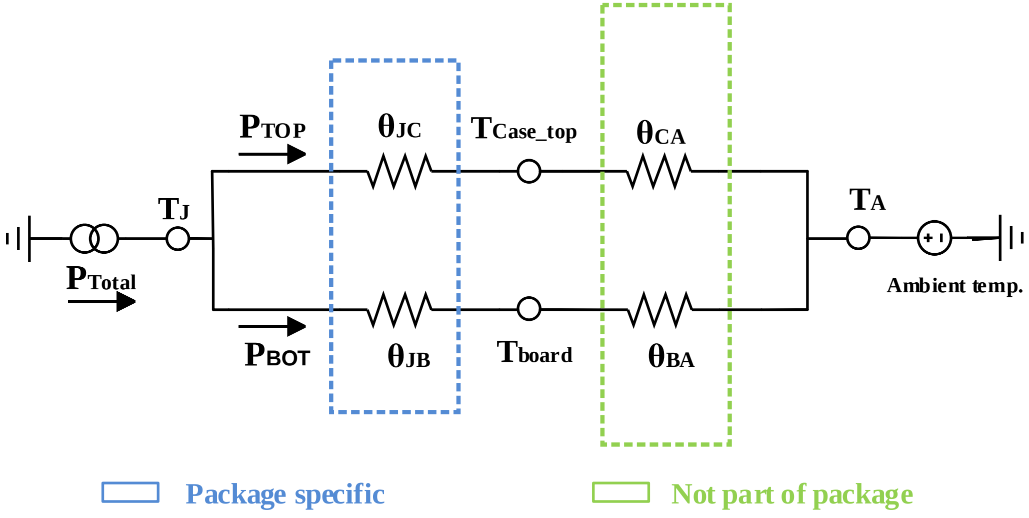
  MPQ6612A thermal experimental results

- Simple guidelines to a thermally enhanced PCB design

- Conclusion

# Thermal Resistance and Electrical Analogy

**Thermal resistance is a heat property and a measurement of a temperature difference by which material resists a heatflow**



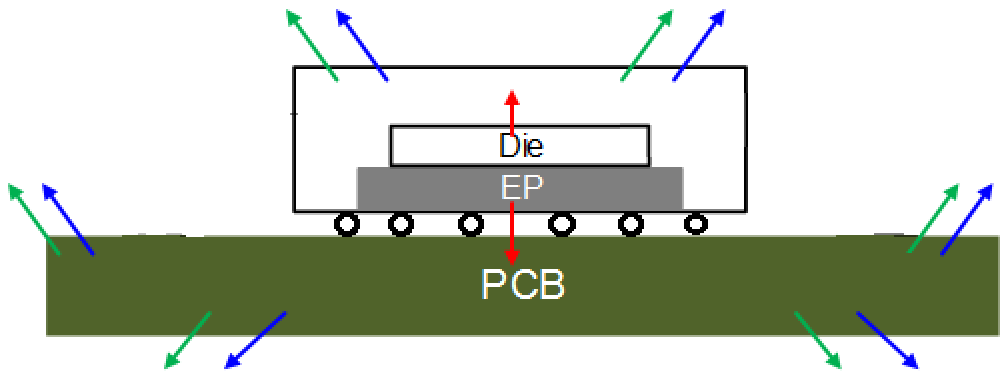

| Electrical Quantities (1) | | | Thermal Quantities (2) | | |
|---|---|---|---|---|---|
| **Quantity** | **Formula Symbol** | **Unit** | **Quantity** | **Formula Symbol** | **Unit** |
| Voltage | $U(t)$ | V | Temperature difference | $\Delta T(t)$ | K |
| Current | $I(t) = \frac{dQ_{el}}{dt}$ | A | Heat flow | $\Phi(t) = \frac{dQ_{th}}{dt}$ | W |
| Charge | $Q_{el}(t) = \int I\,dt$ | A x s | Heat quantity | $Q_{th}(t) = \int \Phi\,dt$ | W x s |
| Capacitance | $C_{el}$ | $\frac{A \times s}{V}$ | Heat capacity | $C_{th} = c \times \rho \times V$ | $\frac{W \times s}{K}$ |
| Resistance | $R_{el} = \frac{L}{\varkappa \times A}$ | $\Omega = \frac{V}{A}$ | Thermal resistance | $R_{th} = \frac{L}{\lambda \times A}$ | $\frac{K}{W}$ |
| Conductance | $G_{el} = \frac{I}{R_{el}}$ | $S = \frac{A}{V}$ | Thermal conductivity | $G_{th} = \frac{I}{R_{th}}$ | $\frac{W}{K}$ |
| Electric conductivity | $\varkappa$ | $\frac{A}{V \times m}$ | Thermal conductivity | $\lambda$ | $\frac{W}{m \times K}$ |

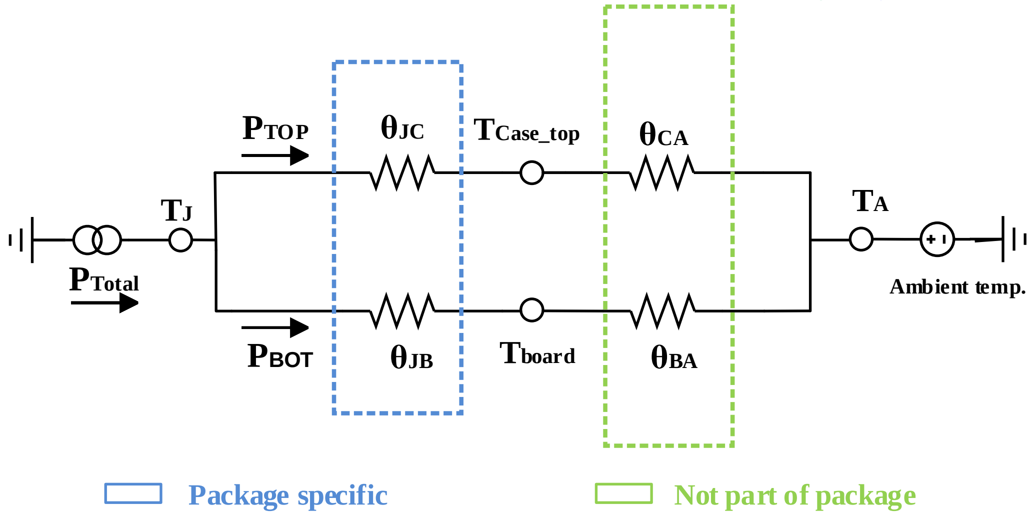
1. The contents of this table are from Technische Temperaturmessung: Volume I, Frank Bernhard, ISBN 978-3-642-62344-8.
2. el refers to electrical values, and th refers to thermal values.

Source: https://www.monolithicpower.com/en/understanding-datasheet-thermal-parameters-and-ic-junction-temperatures

# Thermal Theory

## Heat Transfer Paths




$$\theta_{Jx} = \frac{T_J - T_x}{P_{Jx}}$$

$$\Psi_{Jx} = \frac{T_J - T_x}{P_{total}}$$

$$\theta_{JA} \quad \Psi_{JT}$$

$R_{jx}$=junction-to-x thermal resistance

Tj=junction temperature

Tx=the specific point temperature

$P_{jx}$=the power loss of heat flow through x

$P_{total}$=the total power

**For natural convection heat transfer, >90% of the heat is dissipated by the board and not from the package surfaces**

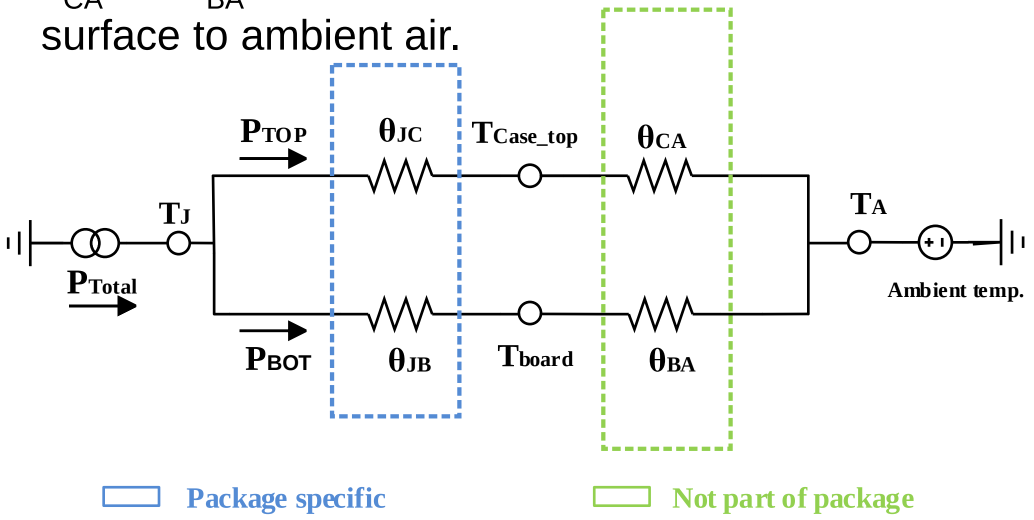
# How To Use Thermal Resistance Parameters

- $\theta_{JA}$: Thermal resistance of the entire system from the die to the ambient air. It is a measure of the device's ability to dissipate heat into the ambient air via all heat transfer paths, the sum of copper tracks, vias, and air convention conditions.

- $\theta_{JB}$: Thermal resistance from the die to the board. $\theta_{JB}$ includes some of the board characteristics and their coupling with the package.

- $\theta_{JC(TOP)}$: Thermal resistance from the die (junction) to the top of the package.

- $\theta_{CA}$ or $\theta_{BA}$: Thermal resistance of convection from the surface to ambient air.




- $\Psi_{JB}$: Characteristic thermal resistance allowing system designers to calculate the device's junction temperature based on a board temperature measurement. The $\Psi_{JB}$ metric should be close to $\theta_{JB}$, as the PCB dissipates most of the heat of the device.

$$T_J = T_{PCB} + (\Psi_{JB} \times P_D)$$

- $\Psi_{JT}$: Characteristic thermal resistance reflecting the temperature difference between the die (junction) and the top of the package. $\Psi_{JT}$ is not a true thermal resistance, as the heat flowing from the die to the top of the package is unknown (but assumed to be the total power of the device). This assumption is clearly not valid, but when calculated this way, $\Psi_{JT}$ becomes a very useful number as its characteristics are much like the application environment of the IC package.

$$\Psi_{JT} = \frac{T_J - T_C}{P_D}$$

$$T_J = T_{case} + (\Psi_{JT} \times P_D)$$

# Thermal Resistance Definitions

| | |
|---|---|
| (1) $R_{\theta JA}$ junction-to-ambient thermal resistance:<br>$R_{\theta JA} = (T_J - T_A) / P_H$<br><br>Where $R_{\theta JA}$ = thermal resistance from junction-to-ambient (°C/W)<br>$T_J$ = junction temperature (°C)<br>**$T_A$ = ambient temperature (°C)**<br>$P_H$ = power loss that produced change in the junction temperature (W) | (2) $R_{\theta JB}$ junction-to-board thermal resistance:<br>$R_{\theta JB} = (T_J - T_B) / P_{HB}$<br><br>Where $R_{\theta JB}$ = thermal resistance from junction-to-board (°C/W)<br>$T_J$ = junction temperature (°C)<br>$T_b$ = board temperature at steady state (°C)<br>$P_{HB}$ = power loss of heatflows through the board (W) |
| (3) $R_{\theta JC\_TOP}$ junction-to-case top thermal resistance:<br>$R_{\theta JC\_TOP} = (T_J - T_{C\_TOP}) / P_{HCTOP}$<br><br>Where $R_{\theta JC\_TOP}$ = thermal resistance from junction-to-case top<br>$T_{C\_TOP}$ = package top temperature (°C)<br>$T_J$ = junction temperature (°C)<br>$P_{HCTOP}$ = power loss of heatflows through the package top (W) | (4) $R_{\theta JC\_BOT}$ junction-to-case bottom thermal resistance:<br>$R_{\theta JC\_BOT} = (T_J - T_{C\_BOT}) / P_{HCBOT}$<br><br>Where $R_{\theta JC\_BOT}$ = thermal resistance from junction-to-case bottom<br>$T_{C\_BOT}$ = package bot temperature (°C)<br>$T_J$ = junction temperature (°C)<br>$P_{HCBOT}$ = power loss of heatflows through the package bottom (W) |
| (5) $\Psi_{JT}$ junction-to-case thermal characterization parameter:<br>$\Psi_{jt} = (T_J - T_{C\_TOP}) / P_H$<br><br>Where $\Psi_{JT}$ = thermal characterization parameter from junction-to-case<br>$T_{C\_TOP}$ = package top temperature (°C)<br>$T_J$ = junction temperature (°C)<br>$P_H$ = power loss that produced change in the junction temperature (W) | (6) $\Psi_{JB}$ junction-to-board thermal characterization parameter:<br>$\Psi_{jb} = (T_J - T_B) / P_H$<br><br>Where $\Psi_{JB}$ = thermal characterization parameter from junction-to-case<br>$T_B$ = board temperature (°C)<br>$T_J$ = board temperature at steady state (°C)<br>$P_H$ = power loss that produced change in the junction temperature (W) |

# JESD51 Test Setup ($R_{\theta JA}$, $\Psi_{JT}$, $\Psi_{JB}$)

- How to test $\theta_{JA}$, $\theta_{JC}$?

$$\theta_{JA} = \frac{T_J - T_A}{P_{JA}} \qquad \theta_{JC} = \frac{T_J - T_C}{P_{JC}}$$

- JESD51 standard noted in datasheet

***Thermal Resistance*** (4) ***$\theta_{JA}$*** ***$\theta_{JC}$***

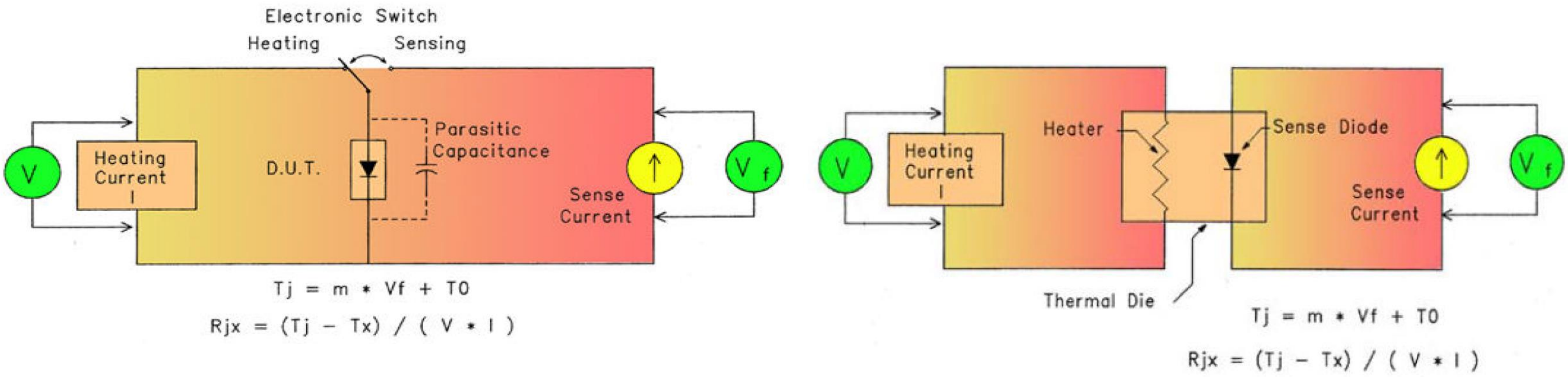
QFN-18 (3mmx4mm)............48.......11...°C/W

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = $(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

# JESD51 Test Setup ($R_{\theta JA}$, $\Psi_{JT}$, $\Psi_{JB}$)

- JESD51-1: Integrated Circuit Thermal Measurement Method-Electrical Test Method

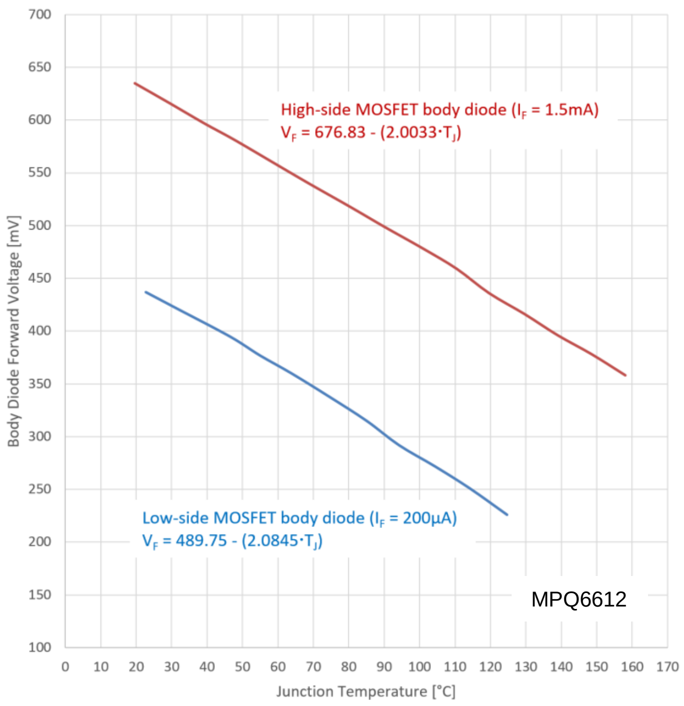



$$\theta_{JA} = \frac{T_J - T_A}{P_{JA}}$$

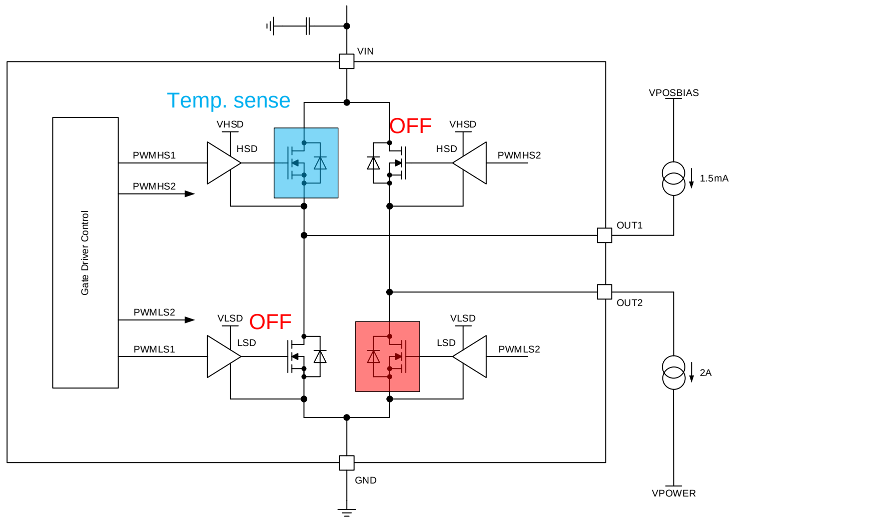
- T3Ster

# Monitoring IC Junction Temperature

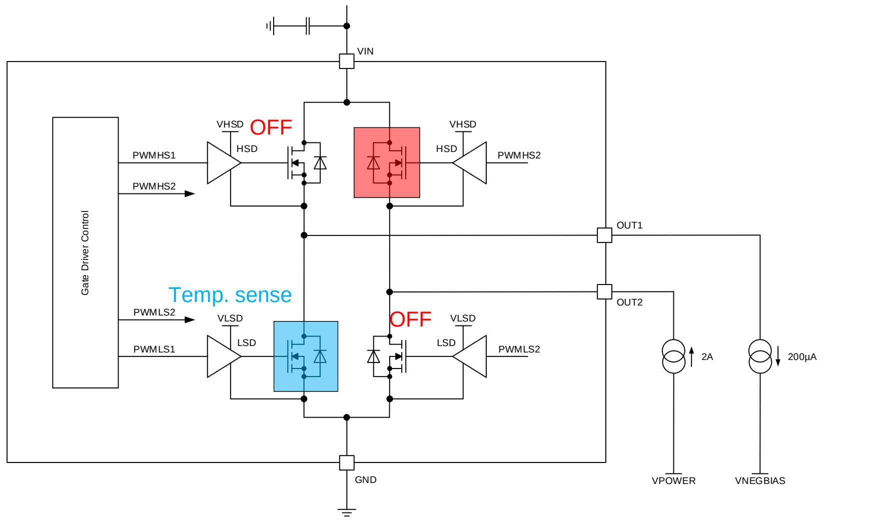
One method to measure the temperature of the power FETs is to employ the junction itself as a temperature sensor, since there is a strong correlation between the forward voltage drop of a junction and the temperature of that junction.




Body Diode Voltage vs. Junction Temperature

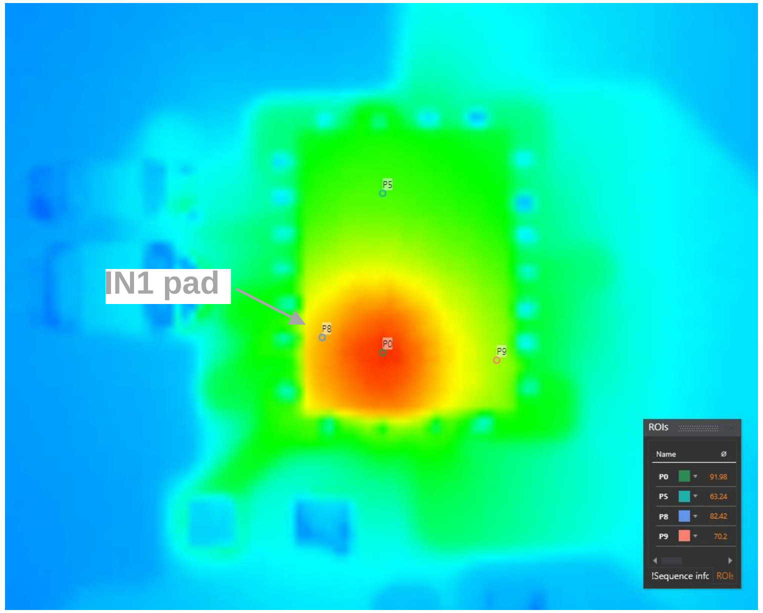



HS-FET Temperature Measurement

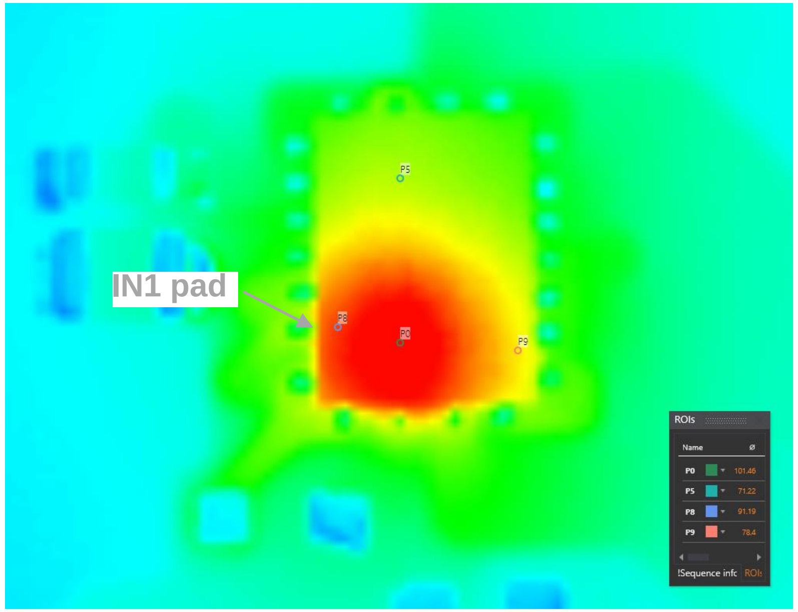



LS-FET Temperature Measurement

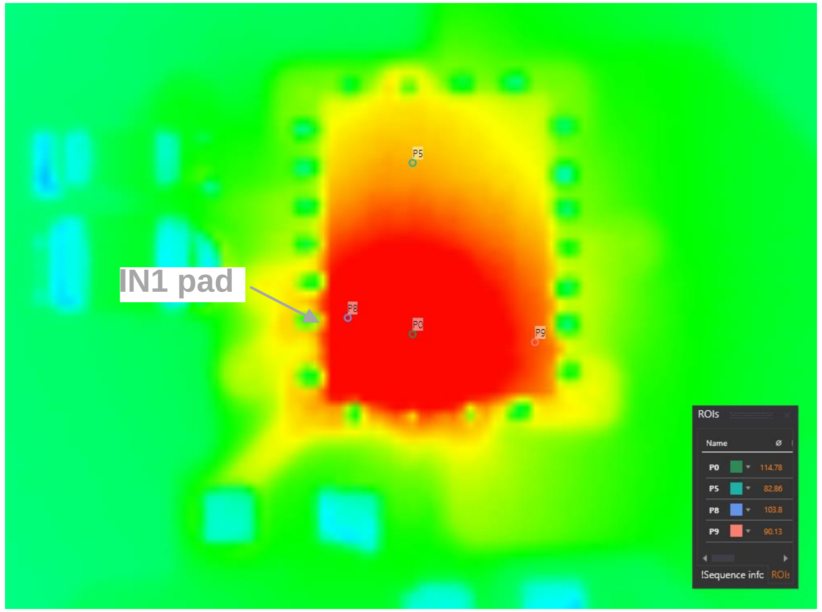
# Monitoring IC Junction Temperature (contd.)




Output 1 (3.3W, t = 10s)




Output 1 (3.3W, t = 60s)

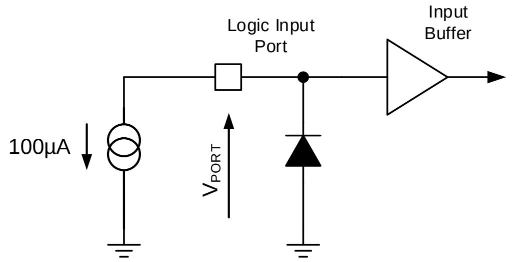



Output 1 (3.3W, t = 1000s)

**Temperature gradient across the power stage (ca. 2000µm): ca. 30°C**

**Temperature gradient power stage to I/O pad: ca. 10°C**

Note: A 10°C temperature offset translates to about a 10% to 20% measurement error (too optimistic).

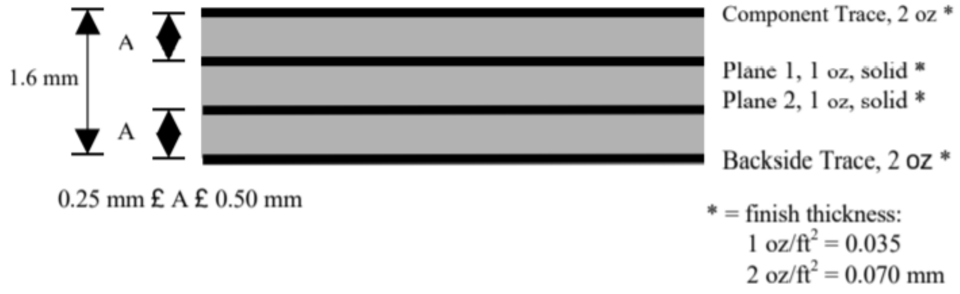


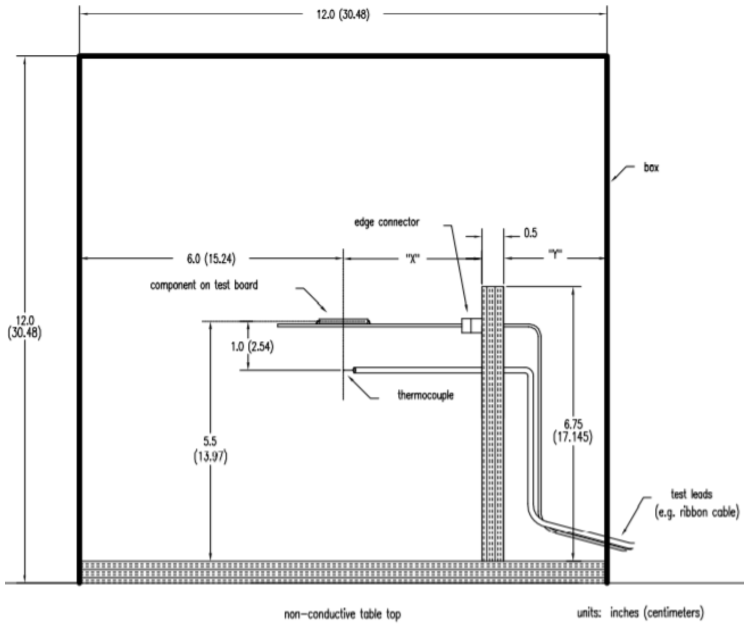
# JESD51 Test Setup ($R_{\theta JA}$, $\Psi_{JT}$, $\Psi_{JB}$)

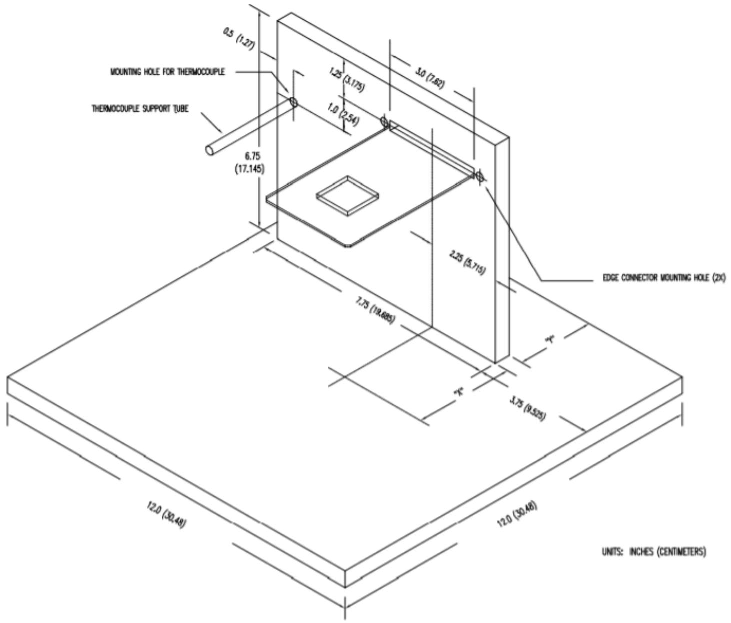
$R_{\theta JA}$, $\Psi_{JT}$, and $\Psi_{JB}$ thermal resistances are based on JESD51-2 (Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)).

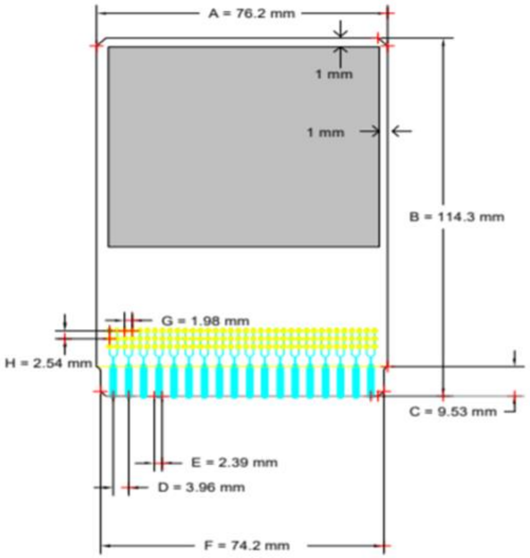
The device is attached to the PCB and placed in a closed environment. The enclosure shall be a box with an inside dimension of 1ft$^3$ (0.0283m$^3$). All seams should be thoroughly sealed to ensure no airflow through the enclosure.

The PCB board (high-K) has 4 metal layers, 1.6mm thickness.

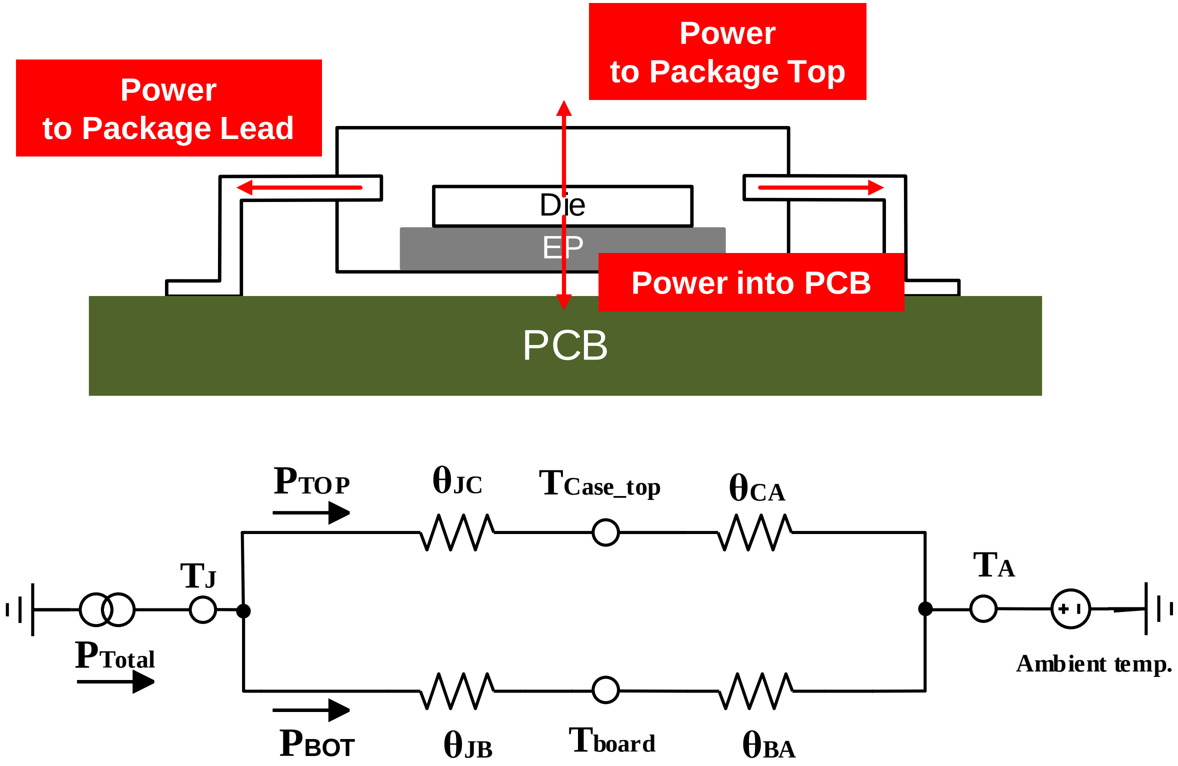


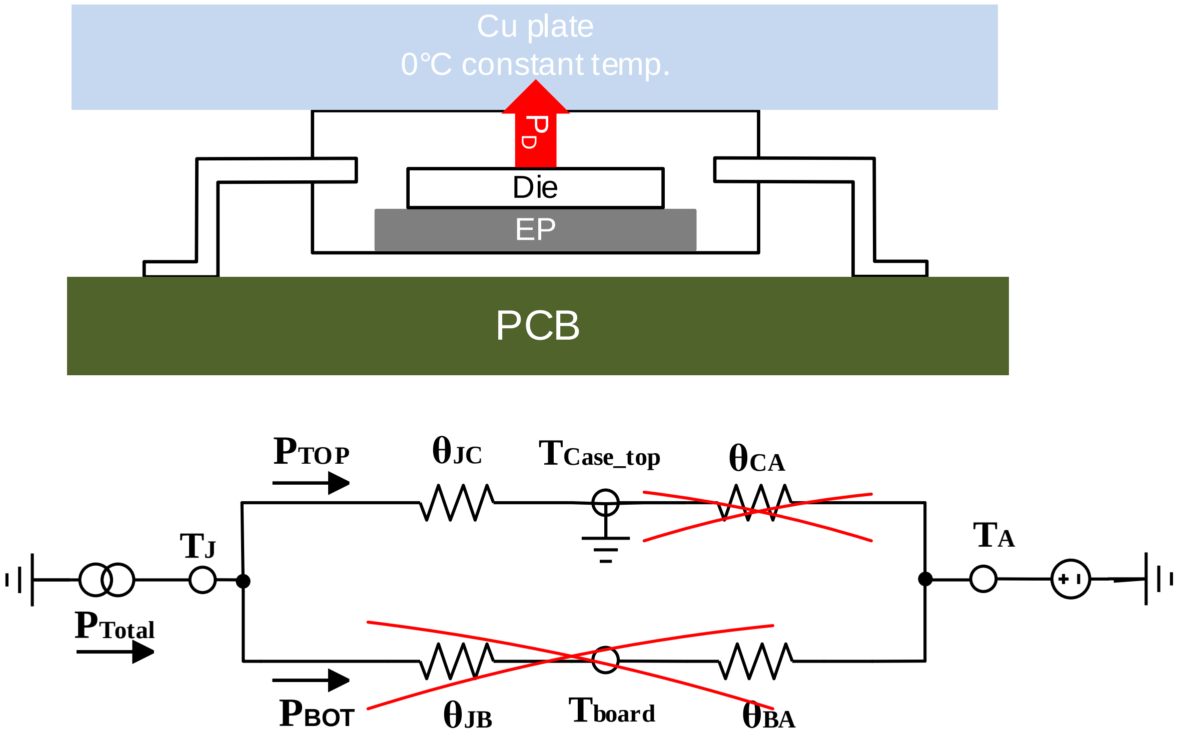



# PSI Junction-Top ($\Psi_{JT}$) vs. Theta Junction-Case ($\theta_{JC}$)




$$\Psi_{JT} = \frac{T_J - T_{C(TOP)}}{P_{Total}}$$

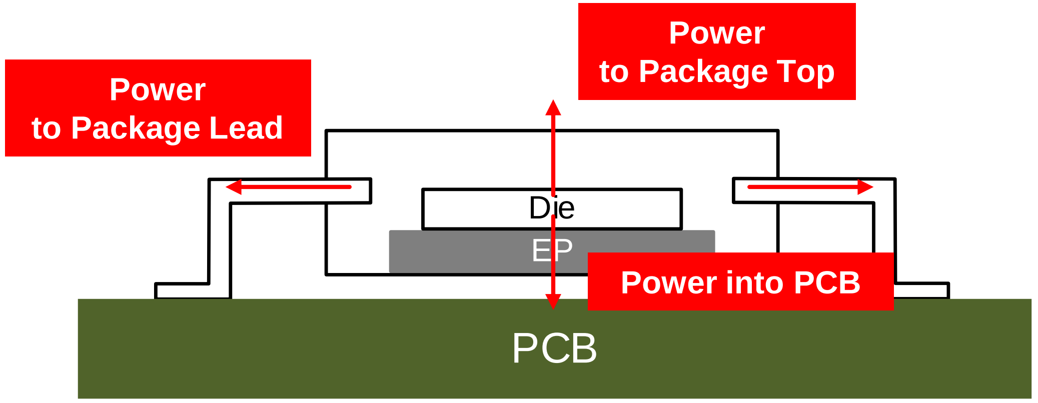
**PSI Junction-Top ($\Psi_{JT}$)**
**Power is dissipated in all directions**

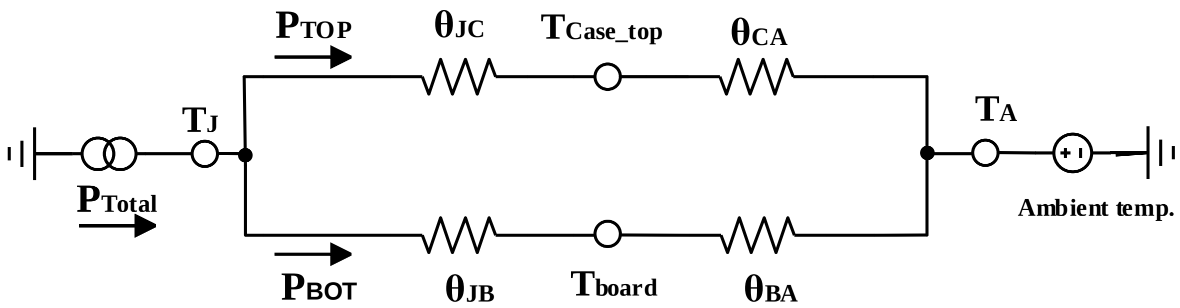



$$\theta_{JC} = \frac{T_J - T_{C(TOP)}}{P_{JC}}$$

**Theta Junction-Case ($\theta_{JC}$)**
**All power is forced to dissipate in only one direction (upward)**

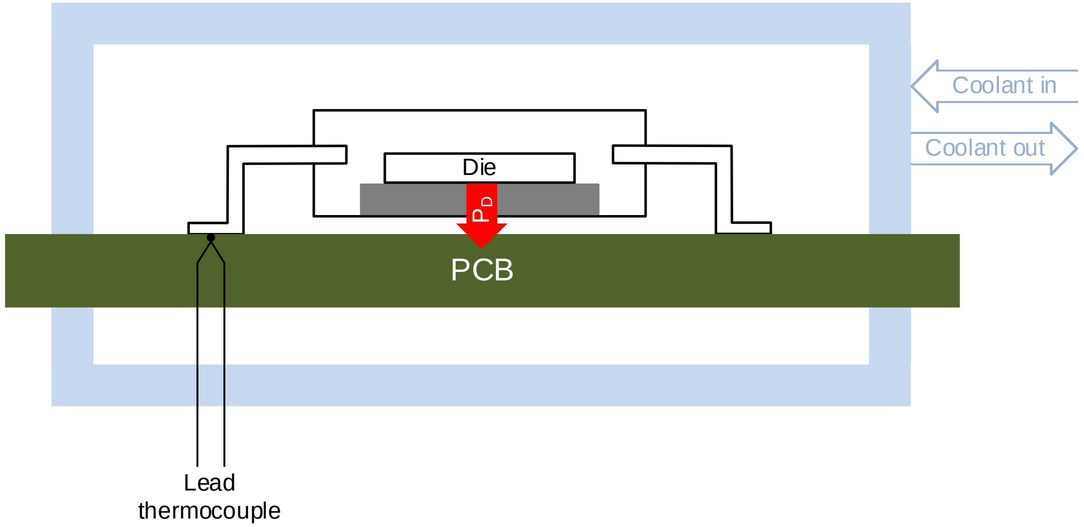
# PSI Junction-Board ($\Psi_{JB}$) vs. Theta Junction-Board ($\theta_{JB}$)

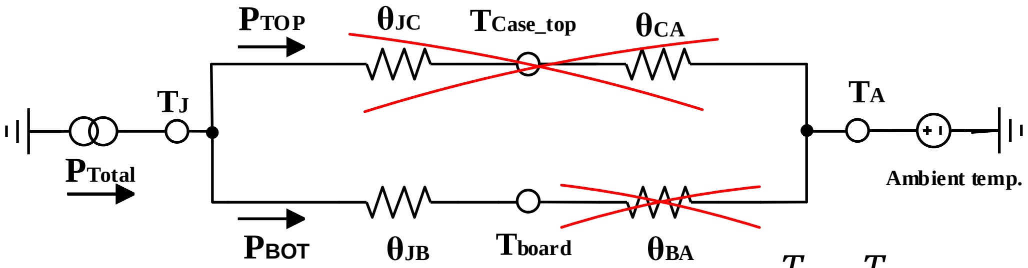



$$\Psi_{JB} = \frac{T_J - T_{board}}{P_{total}}$$

**PSI Junction-Board ($\Psi_{JB}$)**
**Power is dissipated in all directions**




$$\theta_{JB} = \frac{T_J - T_{board}}{P_{BOT}}$$

**Theta Junction-Case ($\theta_{JB}$)**
**All power is forced to dissipate into the board**

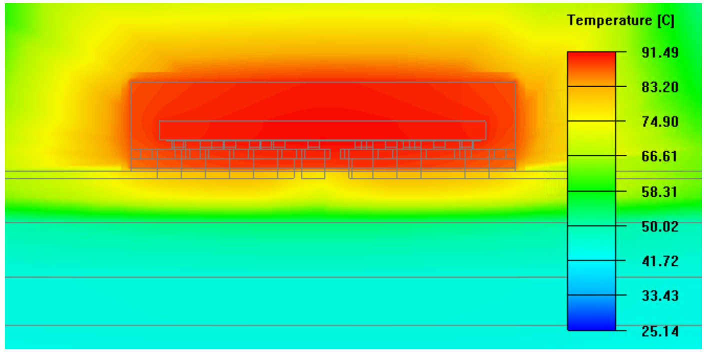
# MPQ6612A Simulated Thermal Parameters

## Theta JA (Junction-to-Air)

$R_{\theta JA} = (T_J - T_A) / P_H$

$T_J = 91.5°C$, $T_A = 25.1°C$

$\mathbf{R_{\theta JA} = 44.3°C/W}$

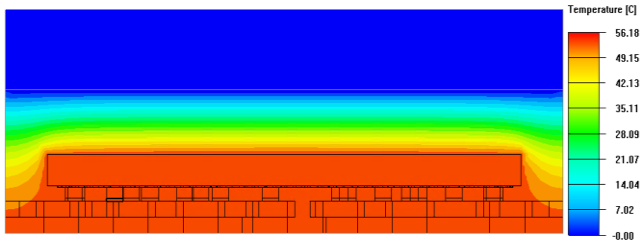



## Theta JC_TOP (Junction-to-Case Top)

$R_{\theta JC\_TOP} = (T_J - T_C) / P_H$

$T_J = 56.2°C$, $T_{C\_TOP} = 0°C$

$\mathbf{R_{\theta JC\_TOP} = 37.5°C/W}$

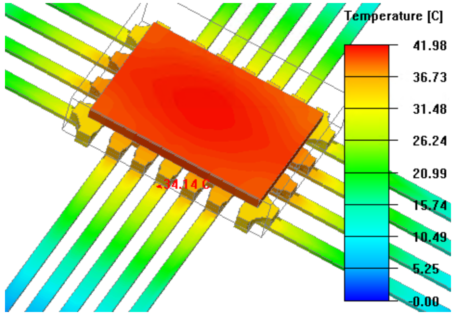



## Theta JB (Junction-to-Board)

$R_{\theta JB} = (T_J - T_B) / P_H$

$T_J = 42°C$, $T_A = 34.1°C$

$\mathbf{R_{\theta JB} = 5.3°C/W}$

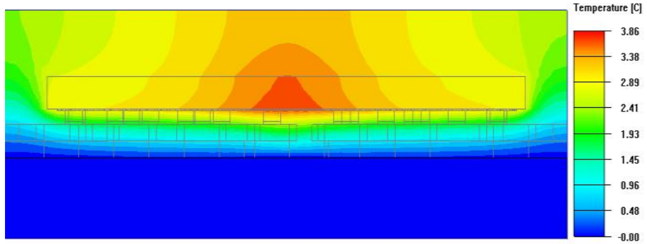



## Theta JC_BOT (Junction-to-Case Bottom)

$R_{\theta JC\_BOT} = (T_J - T_C) / P_H$

$T_J = 3.9°C$, $T_{C\_BOT} = 0°C$

$\mathbf{R_{\theta JA} = 2.6°C/W}$



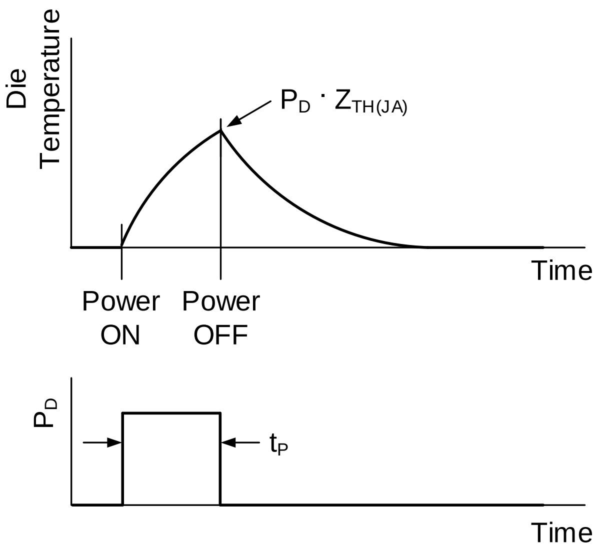

| | $R_{\theta JA}$ | $\Psi_{JT}$ | $\Psi_{JB}$ | $R_{\theta JB}$ | $R_{\theta JC\_TOP}$ | $R_{\theta JC\_BOT}$ | |
|---|---|---|---|---|---|---|---|
| MPQ6612A | 44.3 | 1.1 | 5.1 | 5.3 | 37.5 | 2.6 | (°C/W) |

# Pulsed Operation

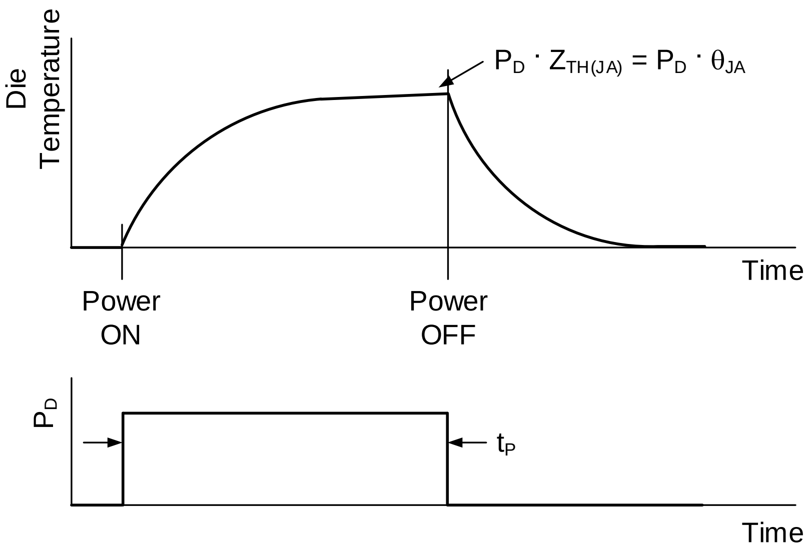
When a motor driver is subjected to a pulsed load, higher peak power dissipation must be tolerable. The materials in power packages have a definite thermal capacity; thus the critical junction temperature is not reached instantaneously, even when excessive power is being dissipated in the device.

Thermal capacitance ($C_{TH}$) is a measure of the capability to accumulate heat, like a capacitor accumulates a charge. For a given structural element, $C_{TH}$ depends on the specific heat capacity (c), volume (V), and density ($\rho$), according to the following relationship:

$$C_{TH} = c \cdot \rho \cdot V \quad \text{expressed in J/K}$$

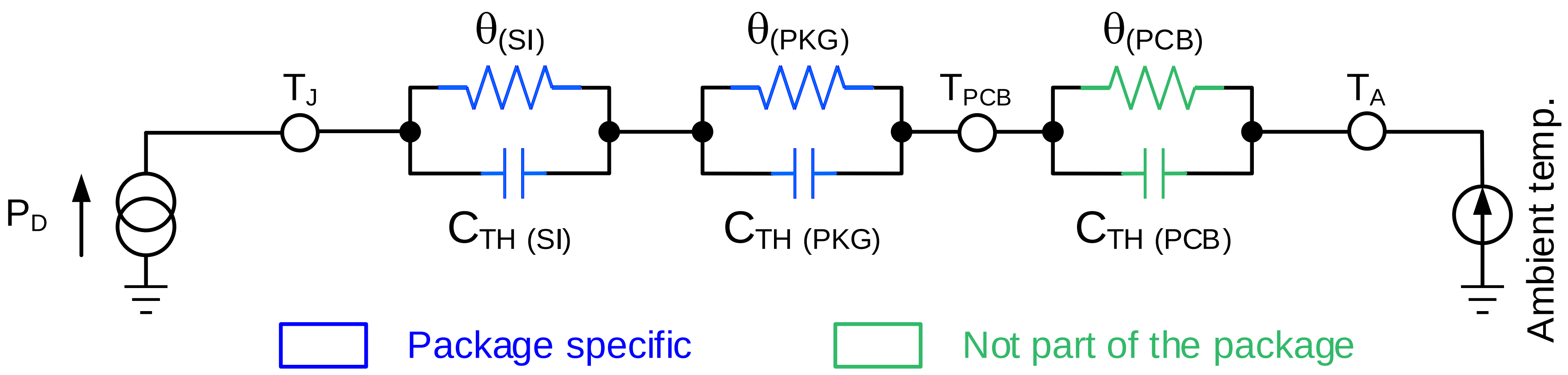



Short Single-Pulse Power




Long Single-Pulse Power

# First Order Transient Thermal Model




The first cell represents the thermal characteristics of the silicon itself, and is characterized by the small volume with a correspondingly low thermal capacitance.

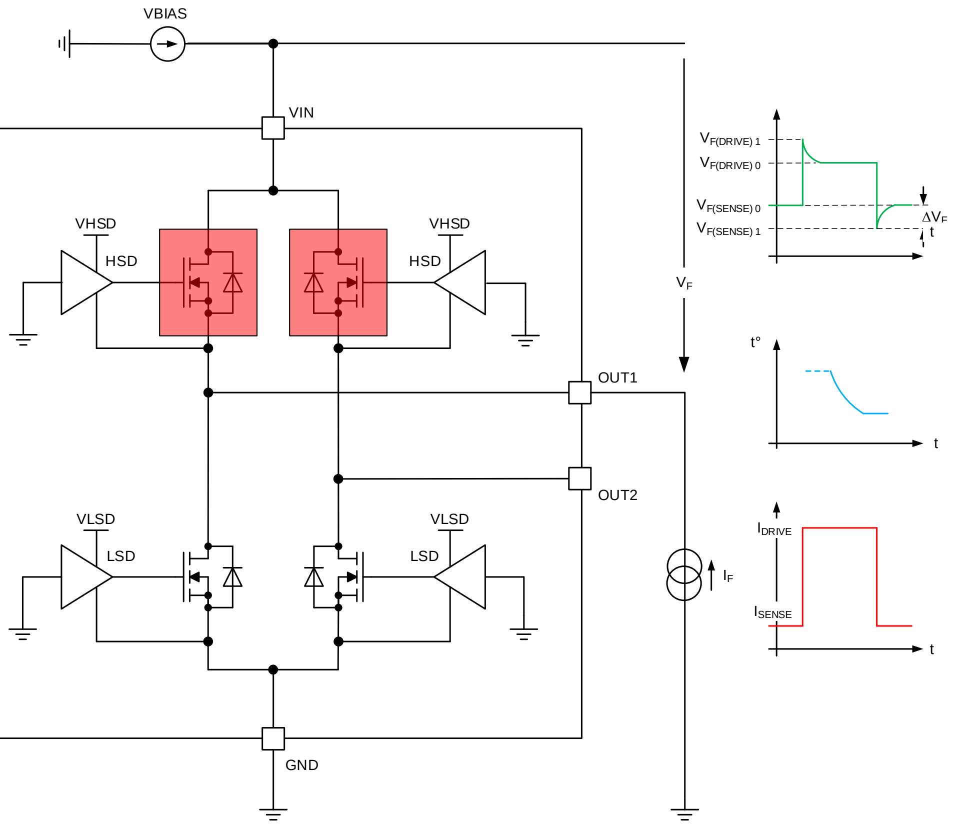
The second cell represents the package. The thermal resistance between the junction and the lead frame depends on die size and the interconnect type (wirebond or MeshConnect™). The thermal capacitance is typically small.

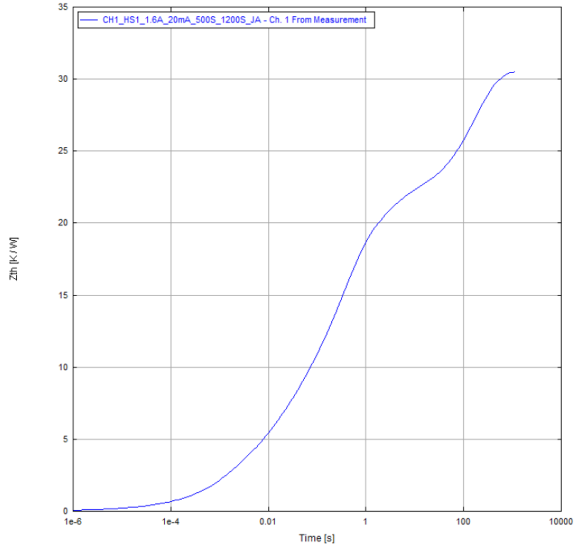
After the device itself has heated, convection and radiation to the ambient air starts. Depending on the PCB's thermal capacitance associated with this phase, it can represent anything from a purely resistive element (not desired) to a fairly large capacitance.

# Characteristic Thermal Impedance

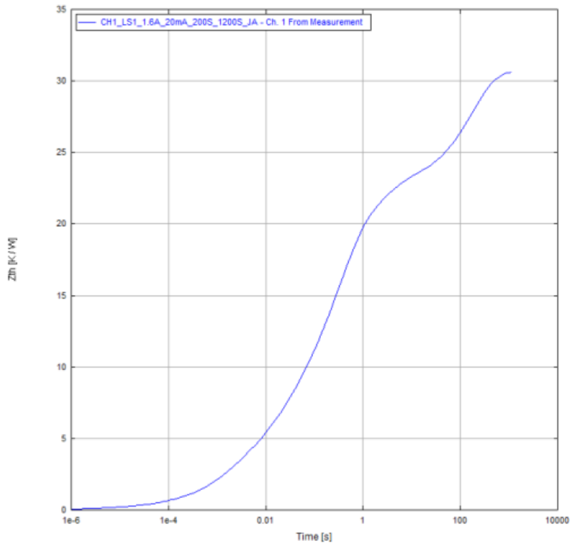
The transient thermal impedance is measured using the same MOSFET body diode for heating and monitoring the temperature. A pulsed current ($I_{SENSE}$, $I_{DRIVE}$) is applied to the device. The change in the diode's forward voltage is monitored before and after the pulse.

$$Z_{TH(JA)} = \frac{T_J - T_A}{P_D}$$



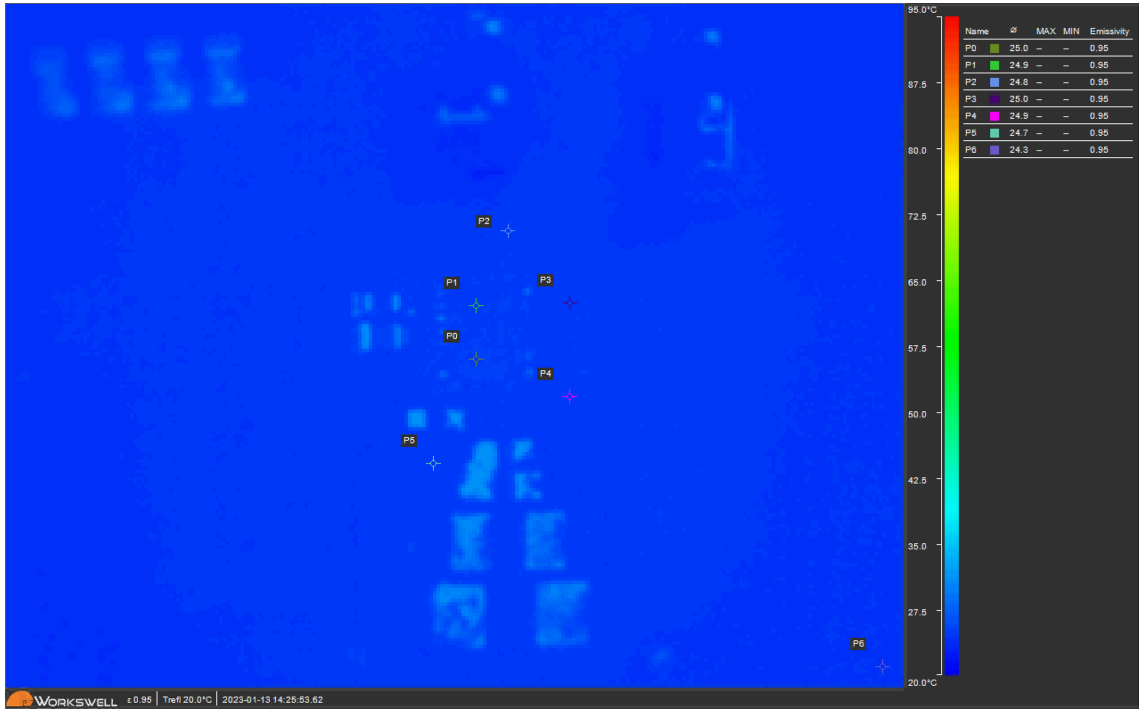

**Thermal Impedance ($\theta_{JA}$)**
**Output 1 High-Side Diode**



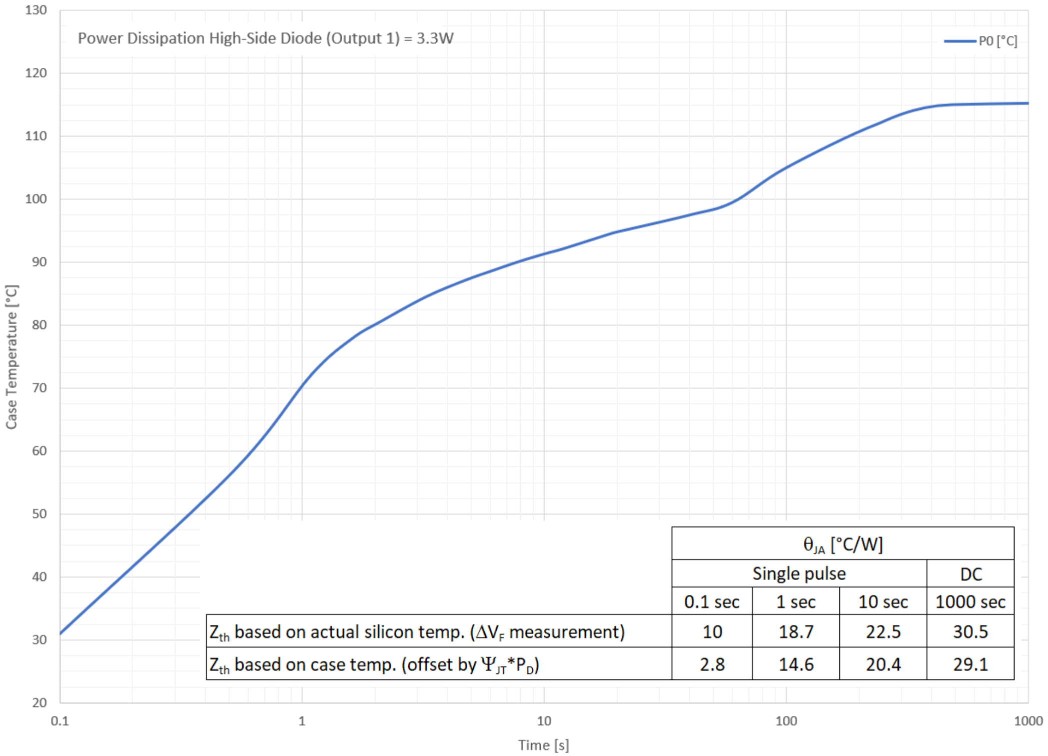

**Thermal Impedance ($\theta_{JA}$)**
**Output 2 High-Side Diode**

Measurement equipment: Mentor Graphics T3Ster thermal transient tester

# High-Side Diode Output 1 Power Dissipation (EVQ6612A-L-00A)




Single-Pulse (20s) Thermal Response (Heating, Cooling)

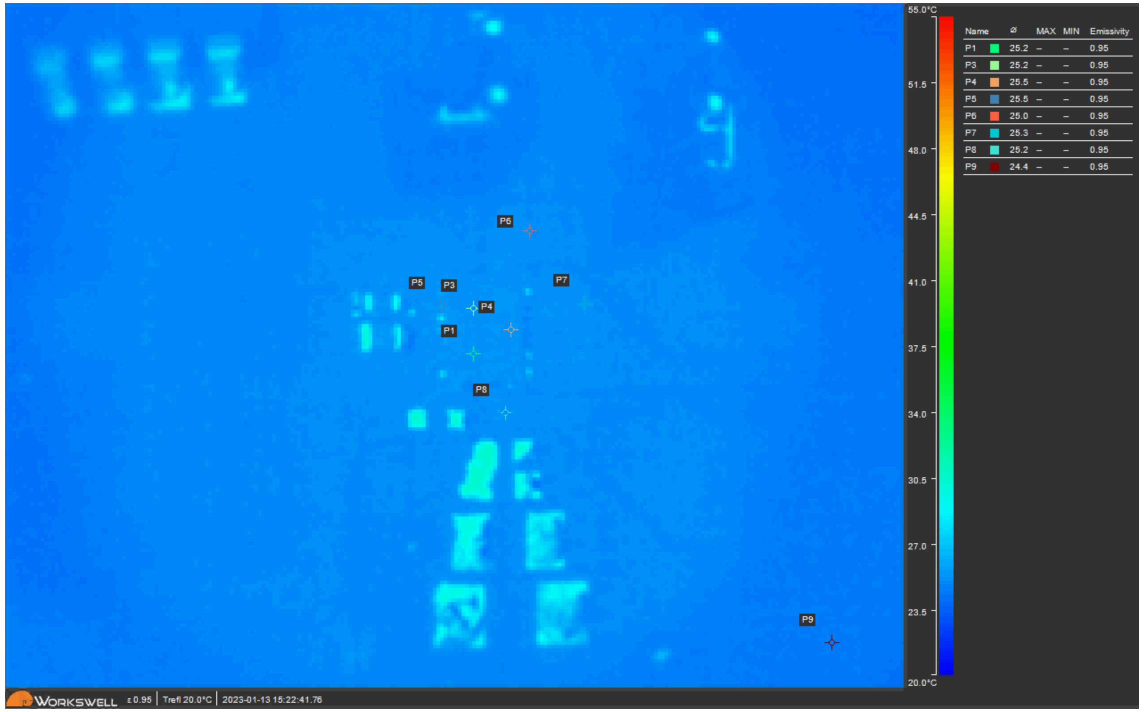



| | $\theta_{JA}$ [°C/W] | | | |
|---|---|---|---|---|
| | Single pulse | | | DC |
| | 0.1 sec | 1 sec | 10 sec | 1000 sec |
| $Z_{th}$ based on actual silicon temp. ($\Delta V_F$ measurement) | 10 | 18.7 | 22.5 | 30.5 |
| $Z_{th}$ based on case temp. (offset by $\Psi_{JT} * P_D$) | 2.8 | 14.6 | 20.4 | 29.1 |

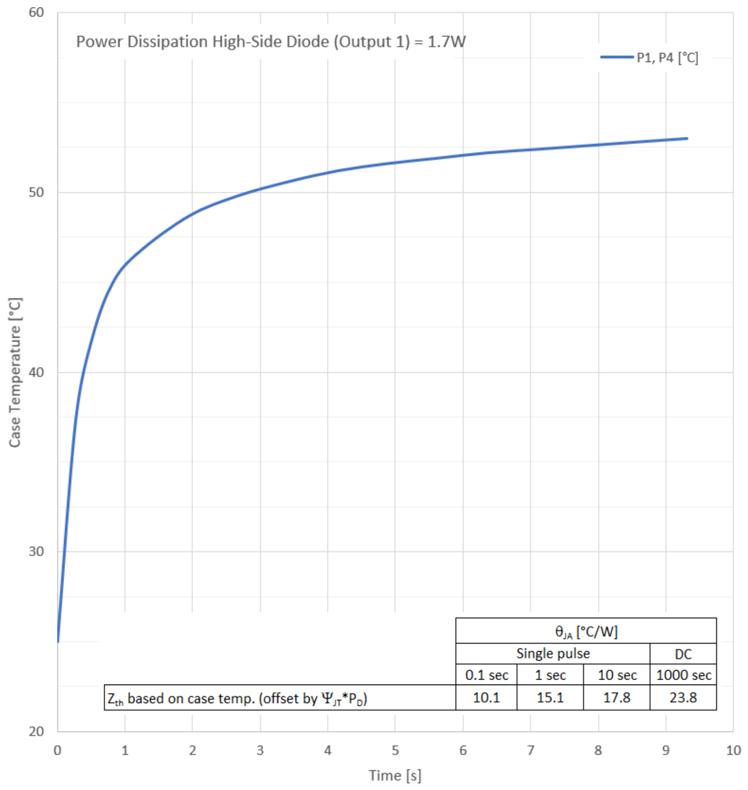
| Time [ms] | PSI_JT [K/W] |
|---|---|
| 0.1 | 0.73 |
| 1 | 2.13 |
| 10 | 5.31 |
| 100 | 7.78 |
| 1000 | 3.83 |
| 10000 | 2.1 |
| 100000 | 1.7 |
| 1000000 | 1.51 |

- Large thermal gradient over the chip area
- The junction temperature can be estimated accurately based on a package case temperature measurements
- Thermal steady state is reached after several minutes

# High-Side Diode Output 1+2 Power Dissipation (EVQ6612A-L-00A)




Single-Pulse (10s) Thermal Response (Heating, Cooling)




| Time [ms] | PSI_JT [K/W] |
|---|---|
| 0.1 | 0.35 |
| 1 | 1.06 |
| 10 | 2.76 |
| 100 | 5.06 |
| 1000 | 2.12 |
| 10000 | 0.88 |
| 100000 | 0.88 |
| 1000000 | 0.88 |

The IC's thermal performance is significantly better on an application board vs. a JEDEC board

# Thermally Enhanced PCB: Basic Rules

- Consider using thick copper for high power designs

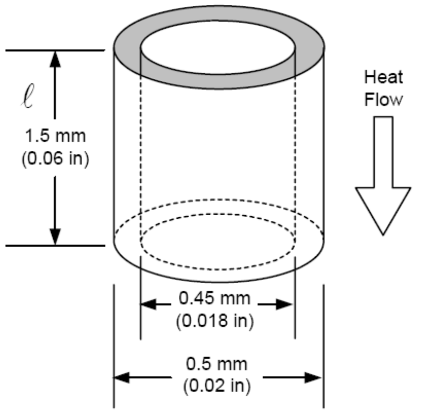
- Use multiple layers for ICs in small packages

- Make the PCB as thin as possible by reducing FR4 thickness
- Optimize top layer power trace design

- Use vias in power lines, placed as close as possible to the IC, to tie adjacent layers together

- The baseline temperature is a function of power dissipation and board area, not cooper thickness

**Use thick layers of copper**
**Use thin layers of FR4**



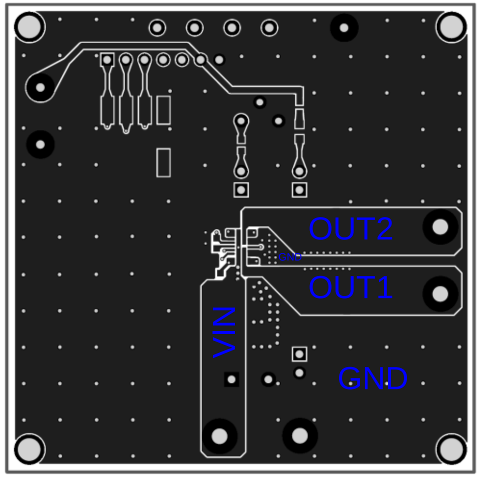

$$\theta = \frac{l}{(K \times A)}$$

$$\theta = \frac{l}{K \times \pi \times (r_o^2 - r_i^2)}$$

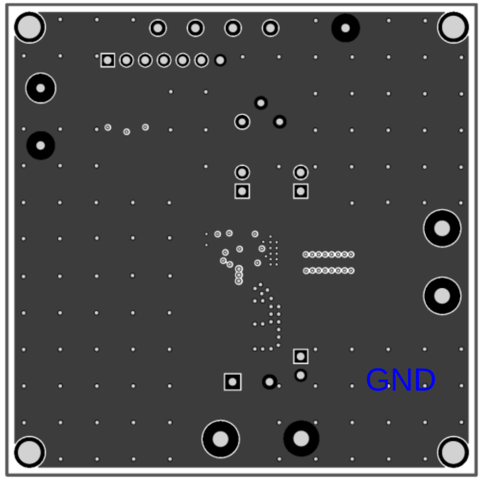
$$\theta = 100^o C/W$$

*A typical via has about 100°C/W thermal resistance*

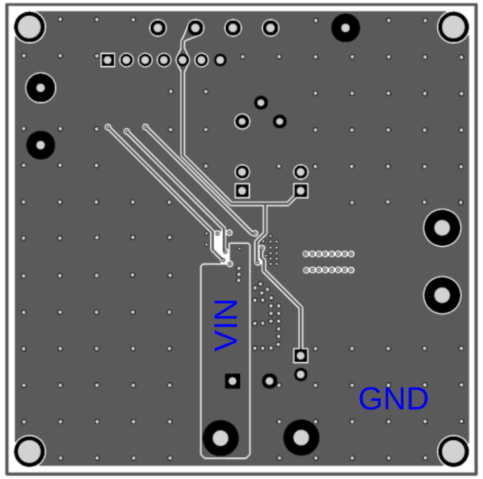
# MPQ6612A: 4-Layer Evaluation Board



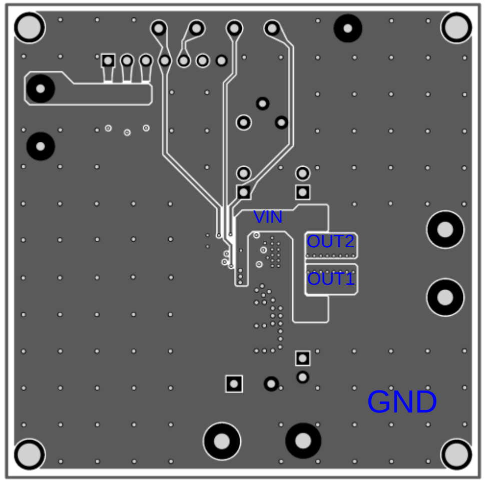

Top Layer




Mid-Layer 1




Mid-Layer 2

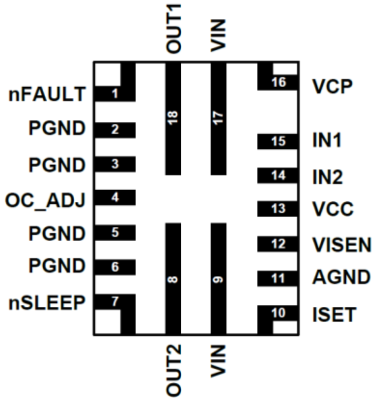



Bottom Layer

PCB Characteristics:

- 4-layer board (63.5mmx63.5mm)
- 70µm copper on all layers
- 1.6mm total thickness

TOP VIEW




MPQ6612A

# Conclusion

## Heat flow path through IC

- Heat flow path
- RJA, ψJT
- JESD51 Series, How to test RJA
- How to test Tjunction
- How to make sure Pjx
- MPQ6612A thermal test results

## Transient thermal impendience Zth

- How to test Zth
- MPQ6612A data analysis

## Simple guidelines to a thermally enhanced PCB design

## MPS’s Thermal Modeling Group Can Provide Additional Support

# Thank you for watching