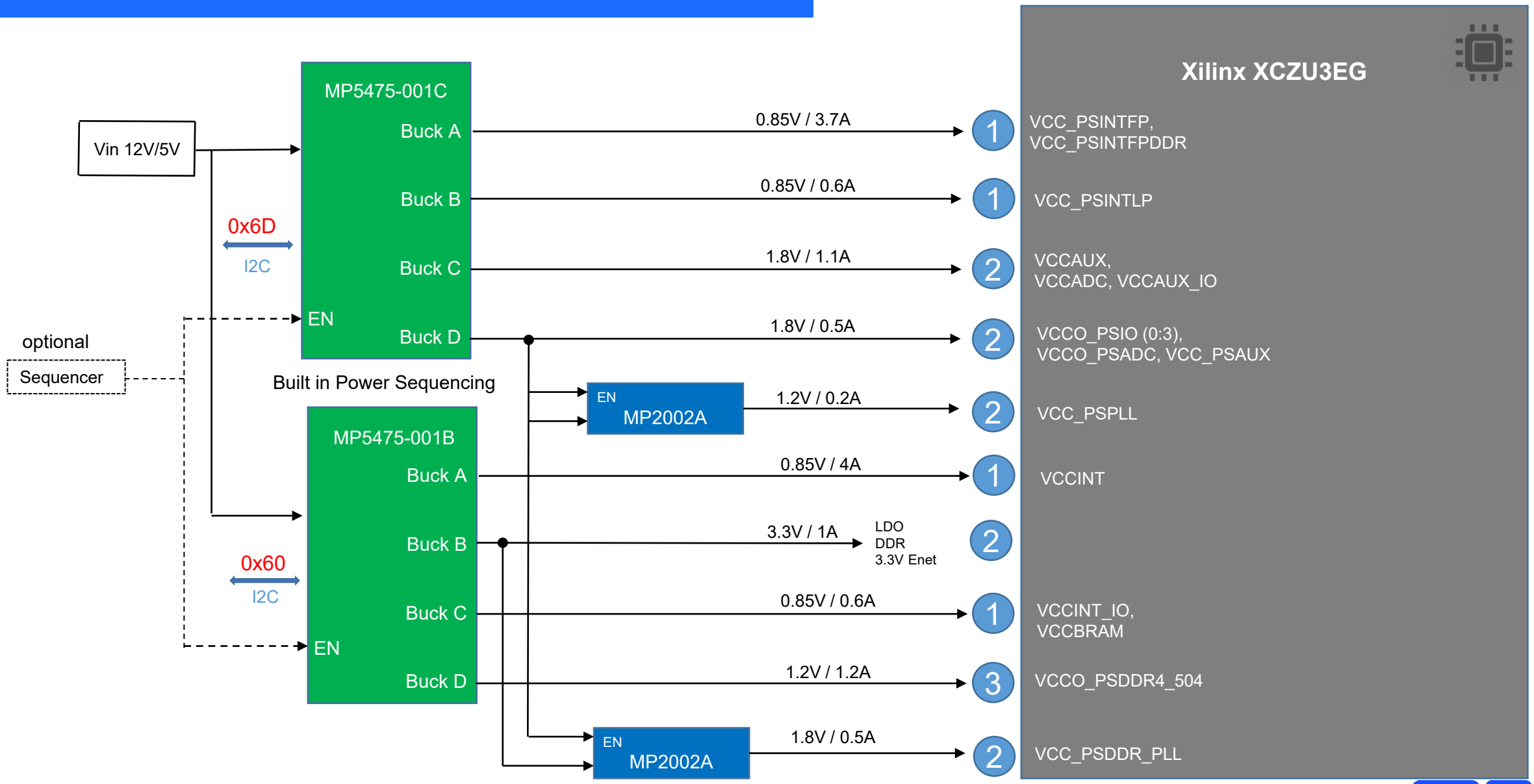
Xilinx XCZU3EG Test Report

MP5475 Reference Design

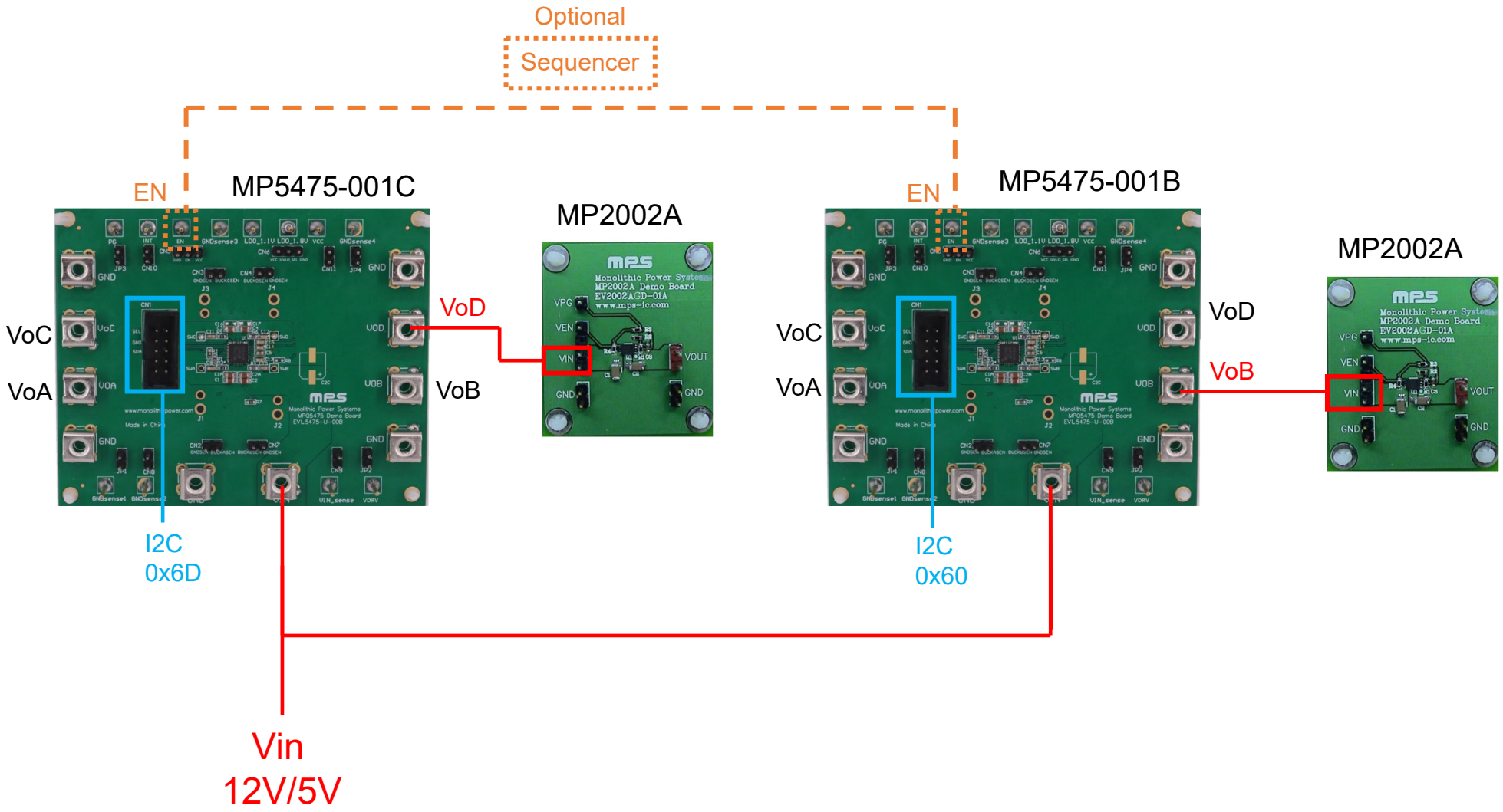
November 2022

MP5475

Power Sequencing



MP5475 EVB Connection

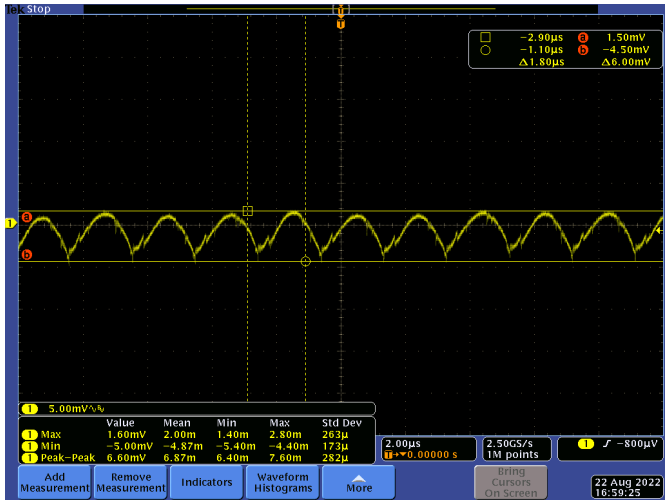


Design Targets

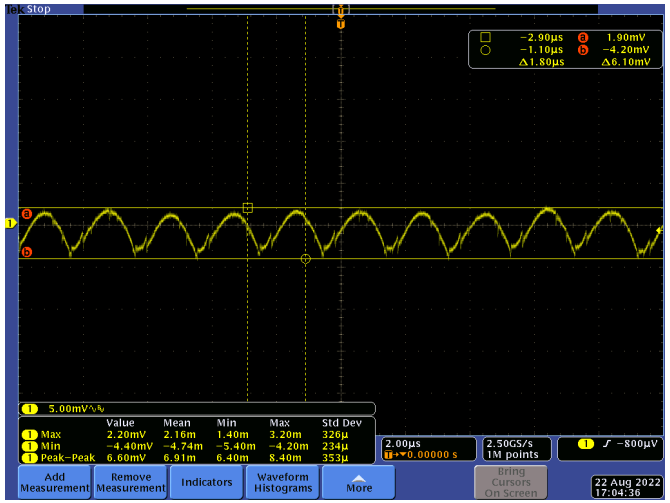
Rails	MPS Part #	Vin	Vo (V) No Load	AC + DC Tolerance	Max Current	Step Load	Slew Rate
VCC_PSINTFP	MP5475	5	0.850	+/-3%	3.7A	0.93A→2.78A→0.93A	2.5A/us
VCC_PSINTLP	MP5475	5	0.850	+/-3%	0.6A	N/A	N/A
VCCAUX	MP5475	5	1.800	+/-3%	1.1A	N/A	N/A
VCCO_PSIO	MP5475	5	1.800	+/-3%	0.5A	N/A	N/A
VCC_PSPLL	MP2002A	5	1.200	+/-3%	0.2A	N/A	N/A
VCCINT	MP5475	5	0.850	+/-3%	4A	1A→3A→1A	2.5A/us
VCCINT_IO	MP5475	5	0.850	+/-3%	0.6A	N/A	N/A
VCCO_PSDDR4	MP5475	5	1.200	+/-3%	1.2A	N/A	N/A
VCC_PSDDR_PLL	MP2002A	5	1.800	+/-3%	0.5A	N/A	N/A

MP5475 VCC_PSINTFP Ripple

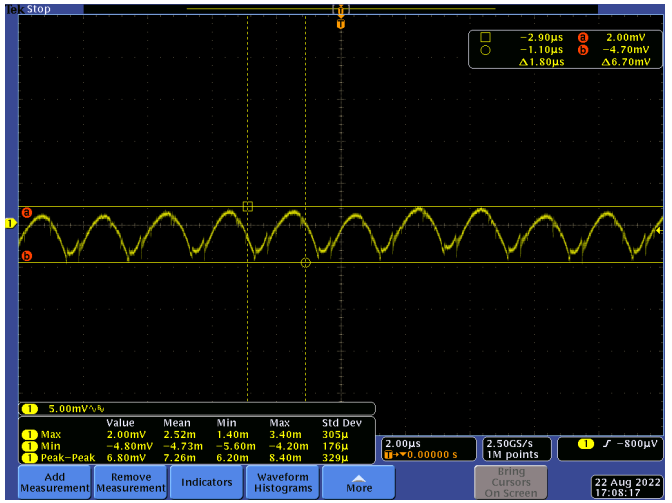
Standby



Half Load



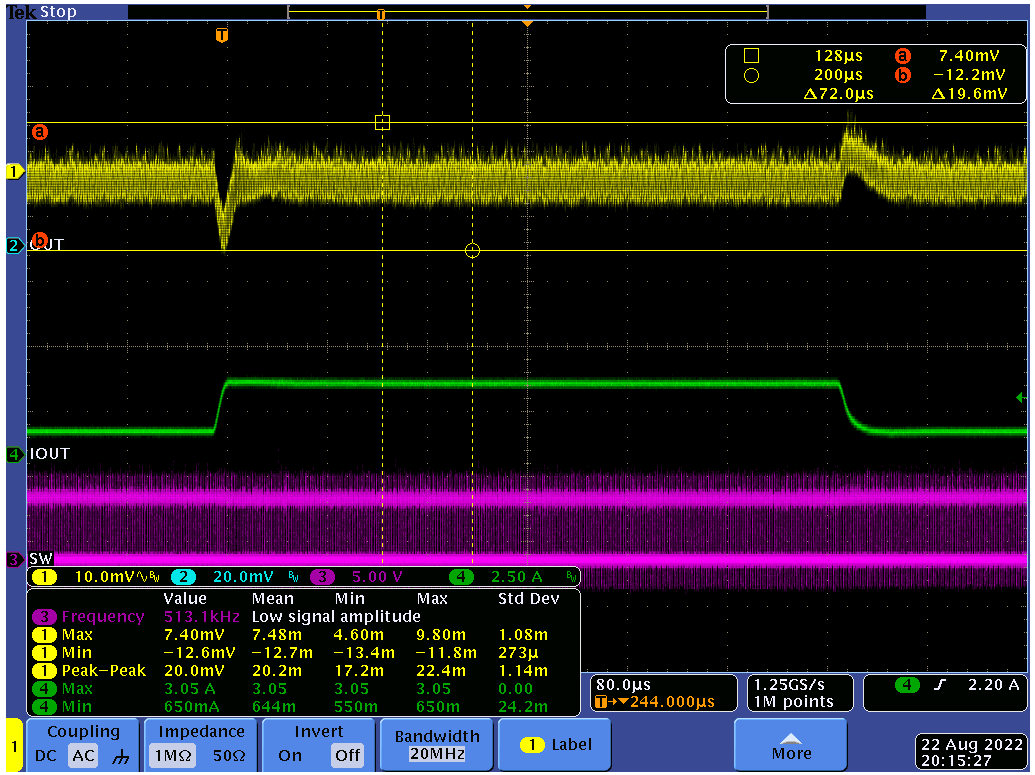
Max Load

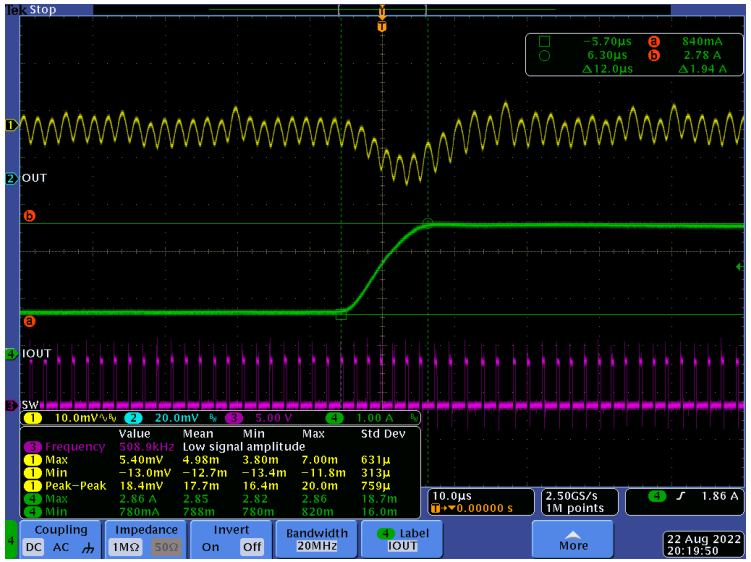


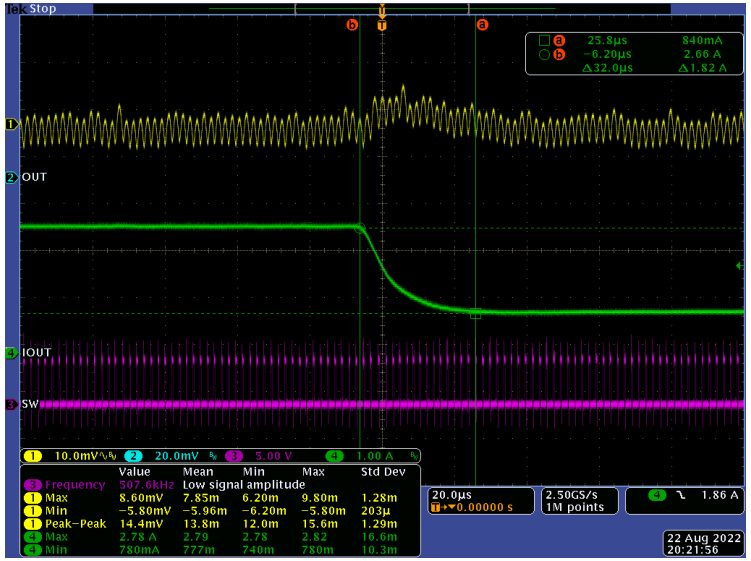
- ❑ 0.78% (6.60 mV) peak-peak ripple at Standby
- ❑ 0.78% (6.60 mV) peak-peak ripple at Half-Load
- ❑ 0.80% (6.80 mV) peak-peak ripple at Full-Load

MP5475 VCC_PSINTFP Transient

Step Load: 0.93A → 2.78A → 0.93A, 2.5A/us



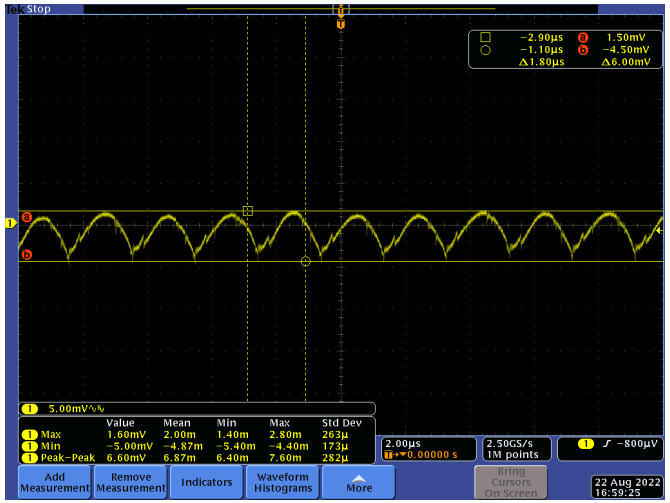




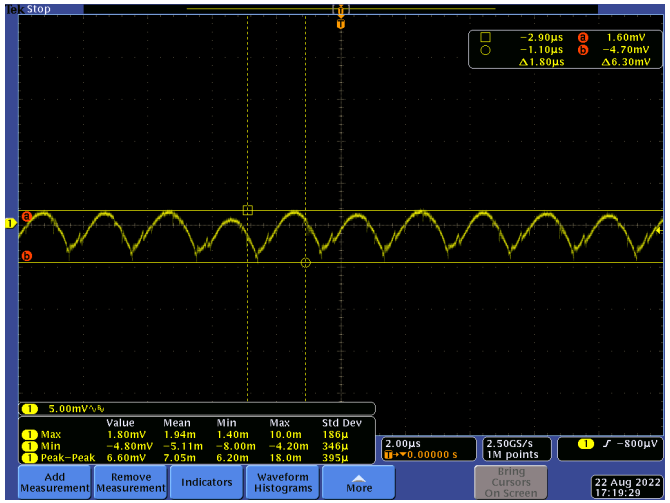
Vo ripple –1.48% (-12.6 mV) to +0.87%(7.40 mV) with load transient

MP5475 VCC_PSINTLP Ripple

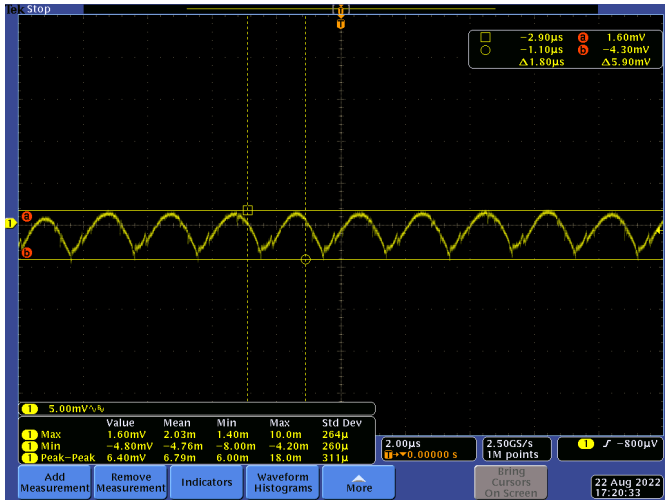
Standby



Half Load



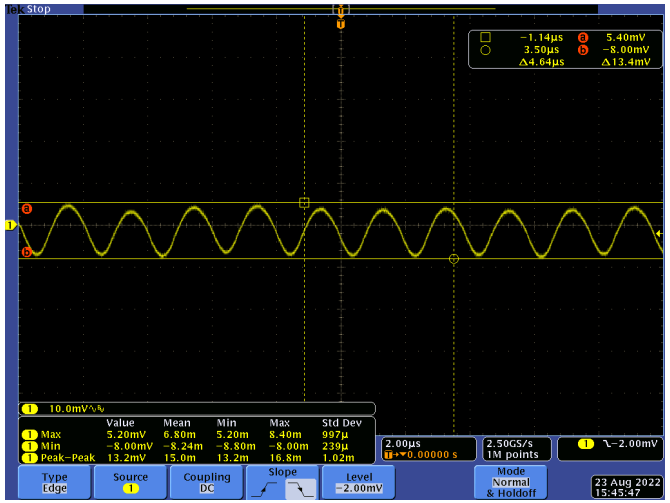
Max Load



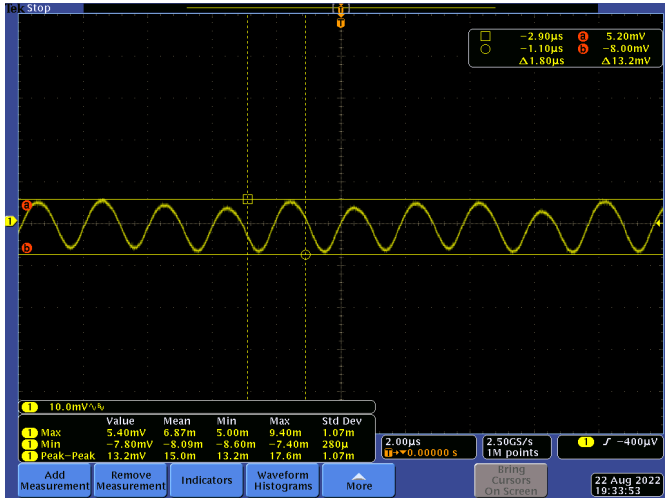
- ❑ 0.78% (6.60 mV) peak-peak ripple at Standby
- ❑ 0.78% (6.60 mV) peak-peak ripple at Half-Load
- ❑ 0.75% (6.40 mV) peak-peak ripple at Full-Load

MP5475 VCCAUX Ripple

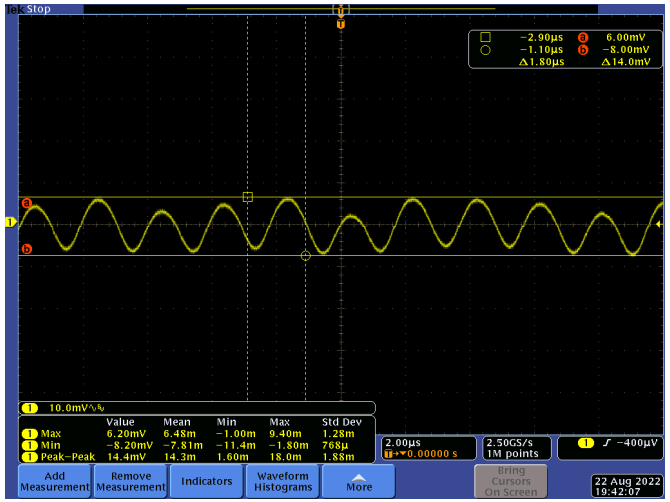
Standby



Half Load



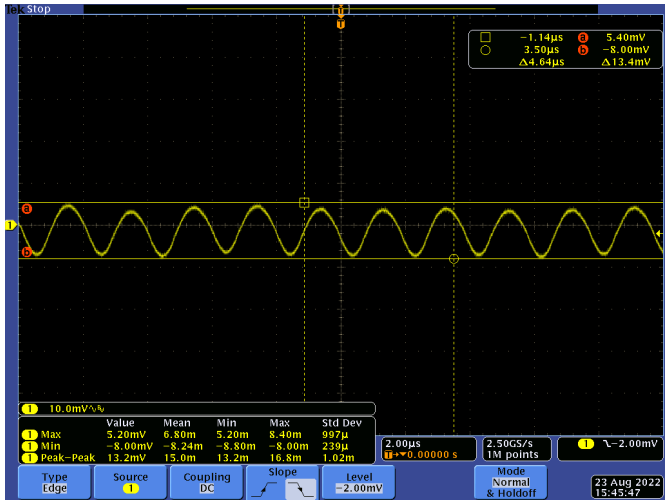
Max Load



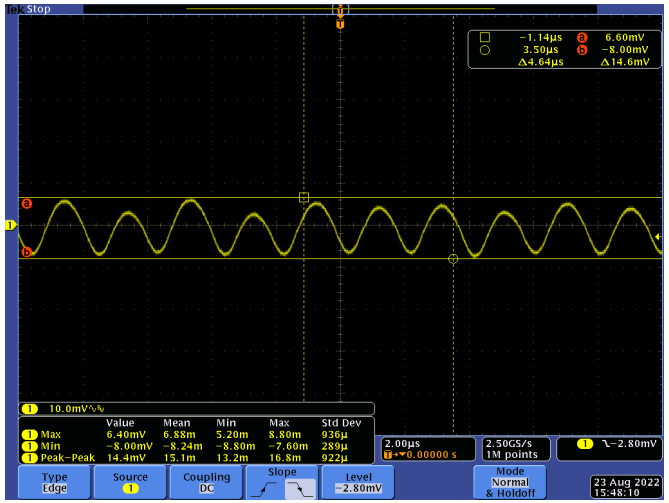
- ❑ 0.73% (13.2 mV) peak-peak ripple at Standby
- ❑ 0.73% (13.2 mV) peak-peak ripple at Half-Load
- ❑ 0.80% (14.4 mV) peak-peak ripple at Full-Load

MP5475 VCCO_PSIO Ripple

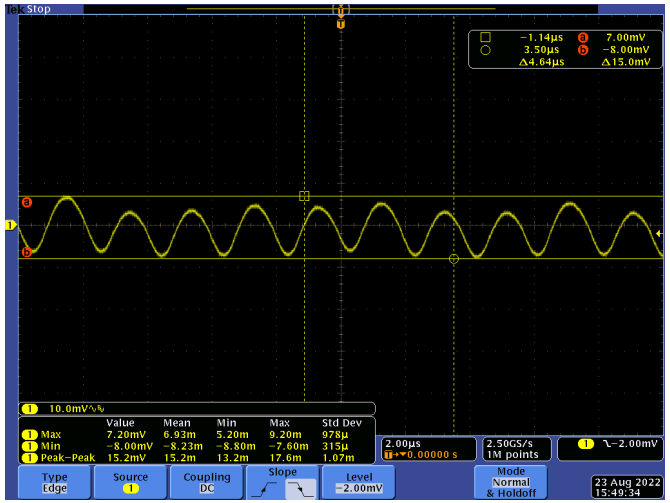
Standby



Half Load



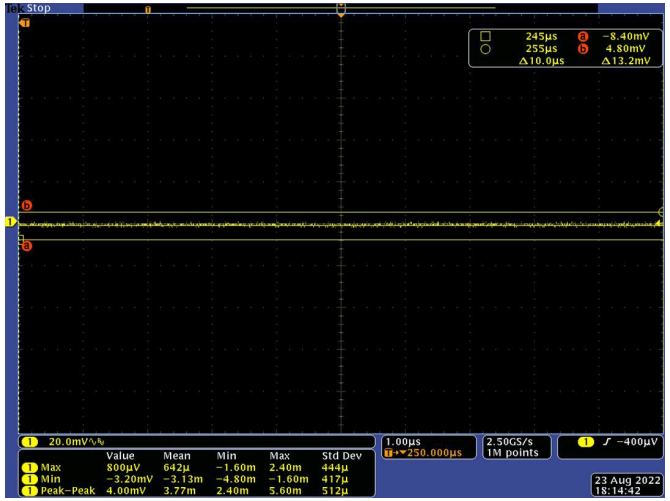
Max Load



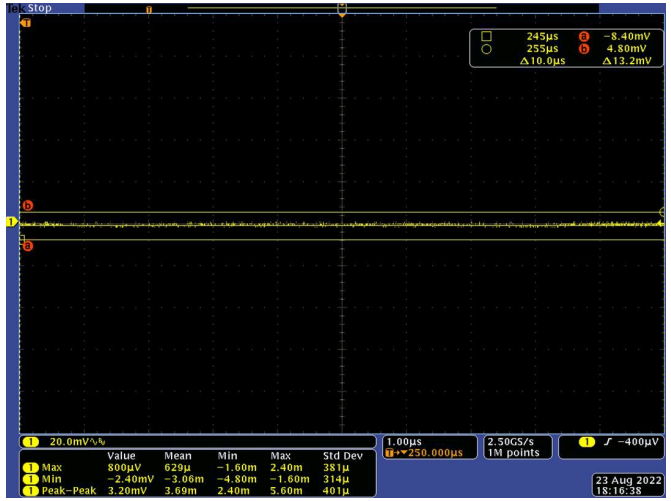
- ❑ 0.74% (13.2 mV) peak-peak ripple at Standby
- ❑ 0.80% (14.4 mV) peak-peak ripple at Half-Load
- ❑ 0.84% (15.2 mV) peak-peak ripple at Full-Load

MP2002A VCC_PSPLL Ripple

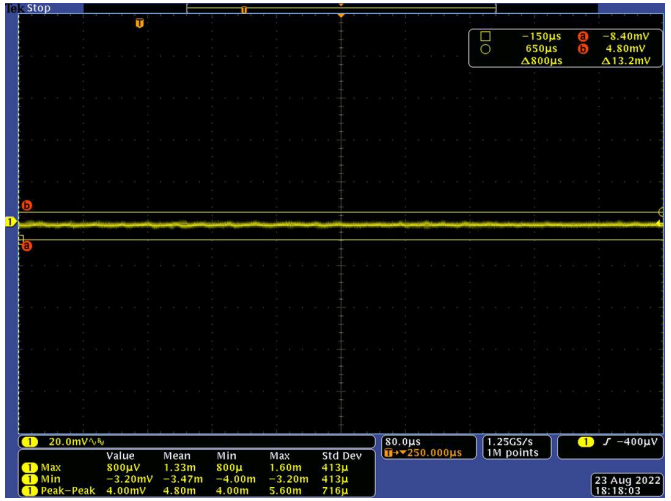
Standby



Half Load



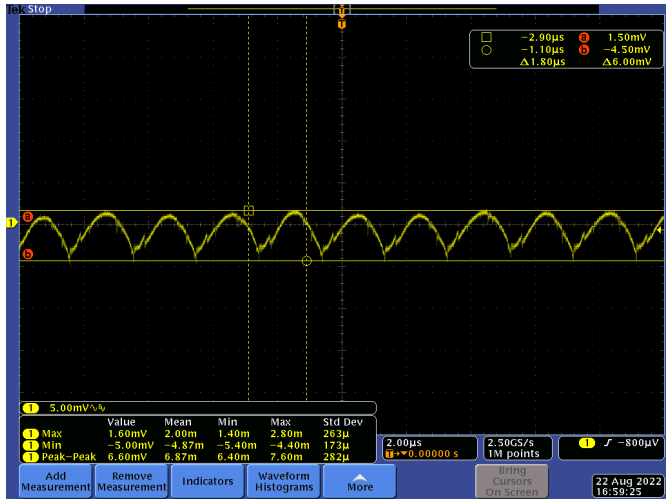
Max Load



- ❑ 0.22% (4.00 mV) peak-peak ripple at Standby
- ❑ 0.18% (3.20 mV) peak-peak ripple at Half-Load
- ❑ 0.22% (4.00 mV) peak-peak ripple at Full-Load

MP5475 VCCINT Ripple

Standby



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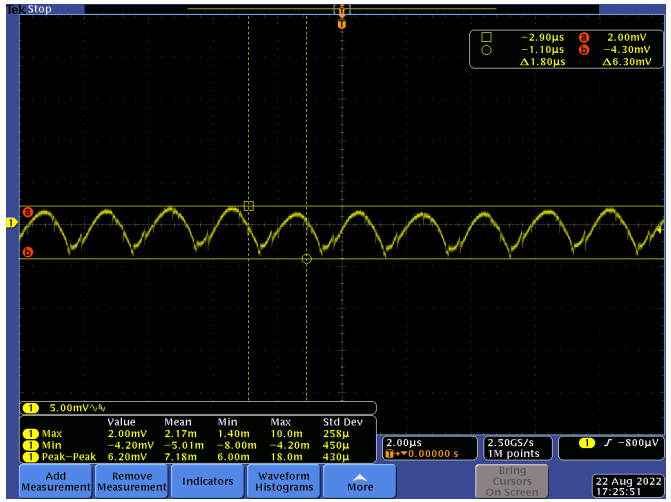
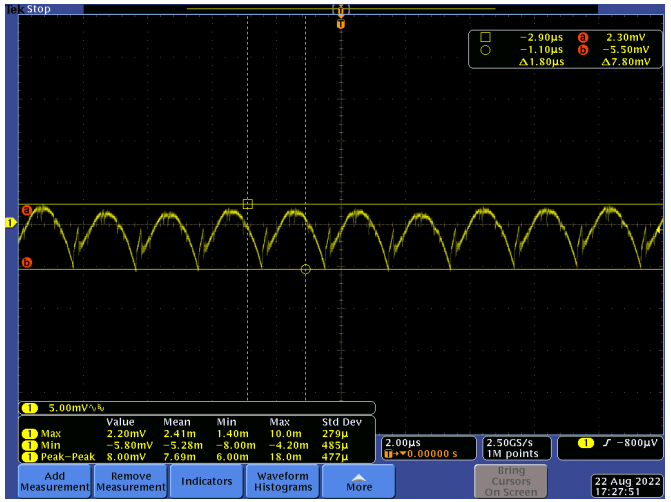


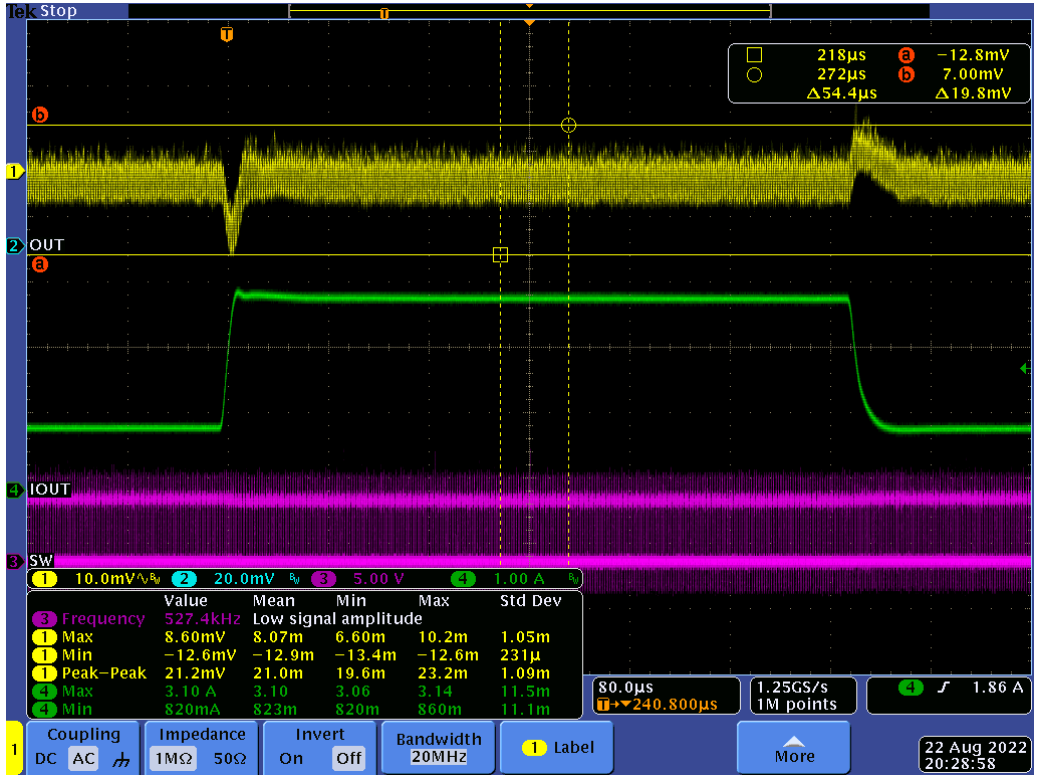
Max Load

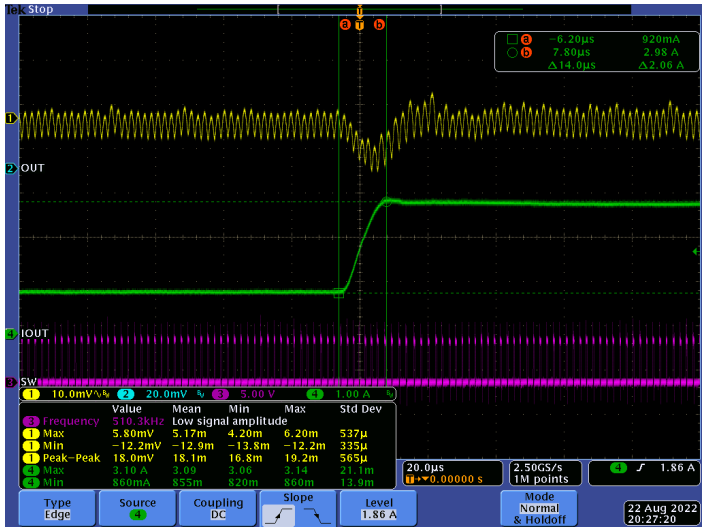


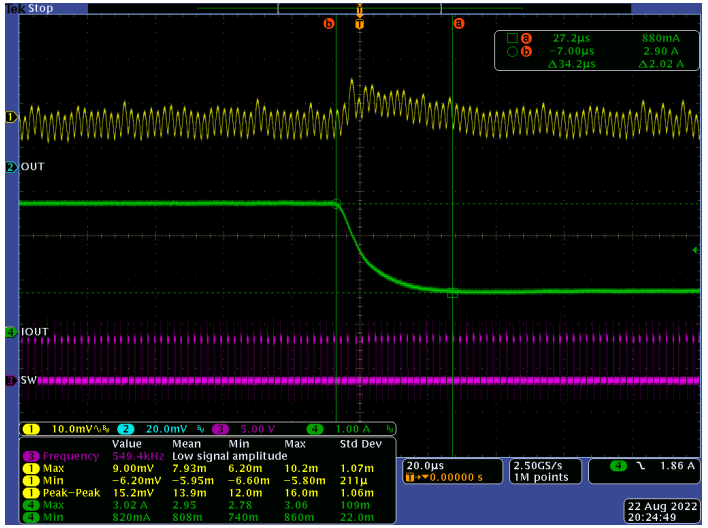
- ❑ 0.78% (6.60 mV) peak-peak ripple at Standby
- ❑ 0.73% (6.20 mV) peak-peak ripple at Half-Load
- ❑ 0.94% (8.00 mV) peak-peak ripple at Full-Load

MP5475 VCCINT Transient

Step Load: 1A → 3A → 1A, 2.5A/us



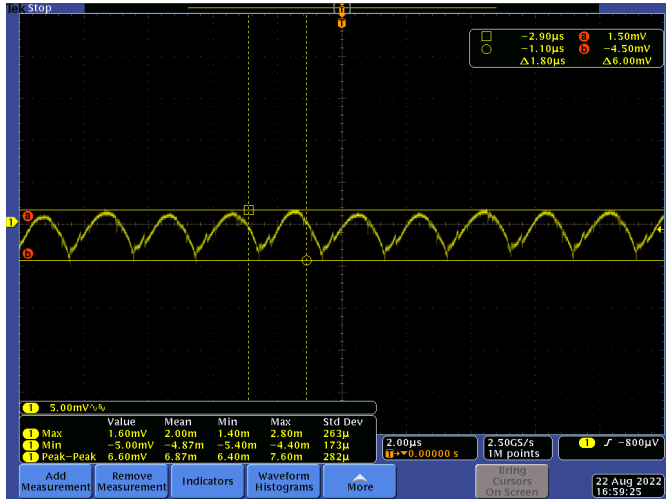




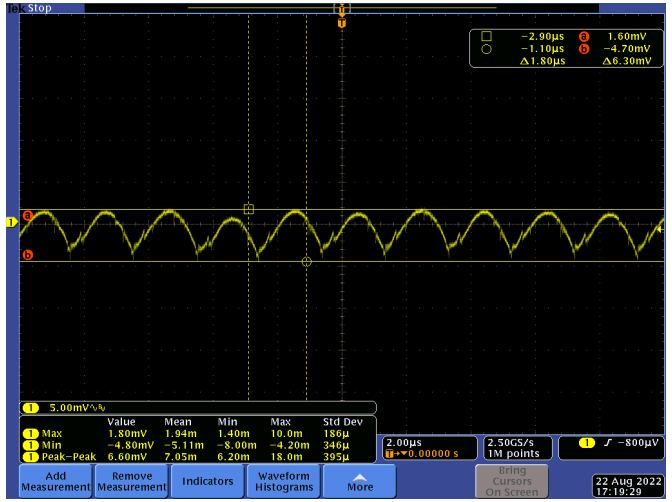
Vo ripple –1.48% (-12.6 mV) to +1.01%(8.60 mV) with load transient

MP5475 VCCINT_IO Ripple

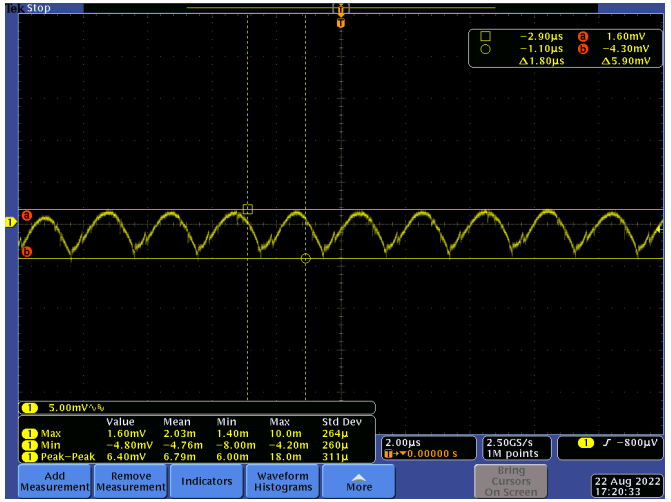
Standby



Half Load



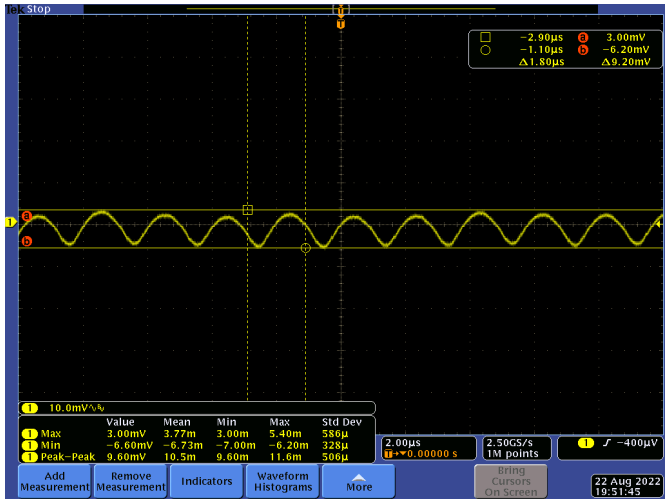
Max Load



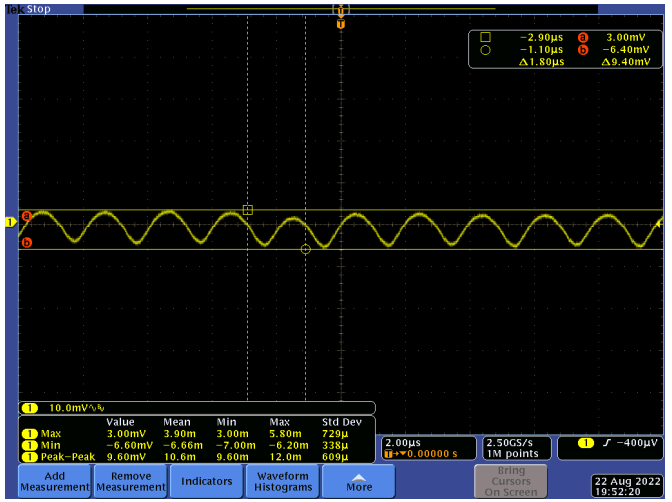
- ❑ 0.78% (6.60 mV) peak-peak ripple at Standby
- ❑ 0.78% (6.60 mV) peak-peak ripple at Half-Load
- ❑ 0.75% (6.40 mV) peak-peak ripple at Full-Load

MP5475 VCCO_PSDDR4 Ripple

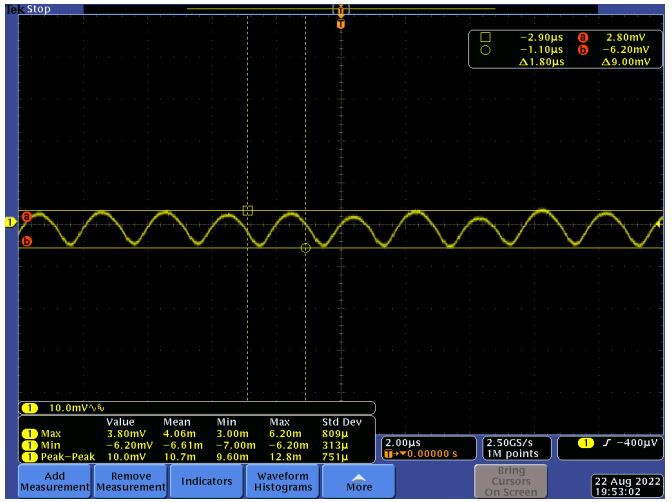
Standby



Half Load



Max Load

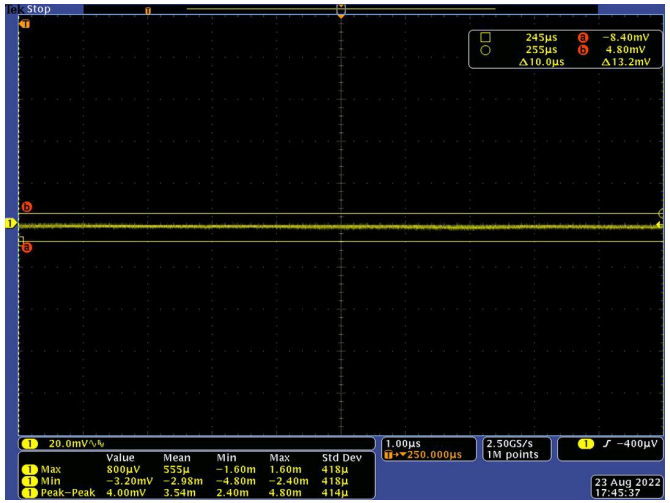


- ❑ 0.80% (9.60 mV) peak-peak ripple at Standby
- ❑ 0.80% (9.60 mV) peak-peak ripple at Half-Load
- ❑ 0.83% (10 mV) peak-peak ripple at Full-Load

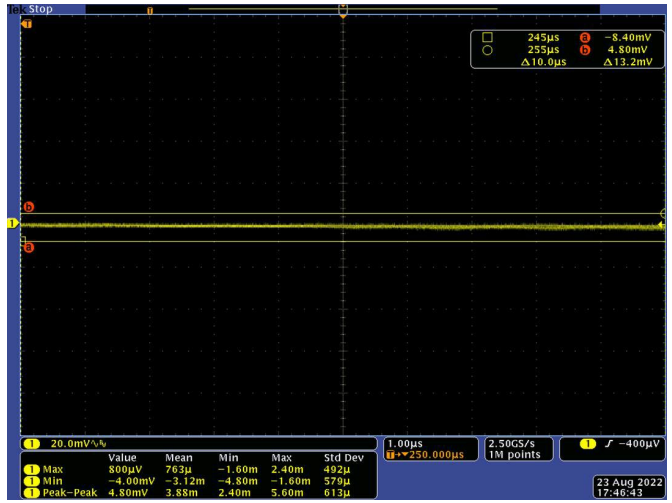
MP2002A VCC_PSDDR_PLL Ripple

Standby

Half Load



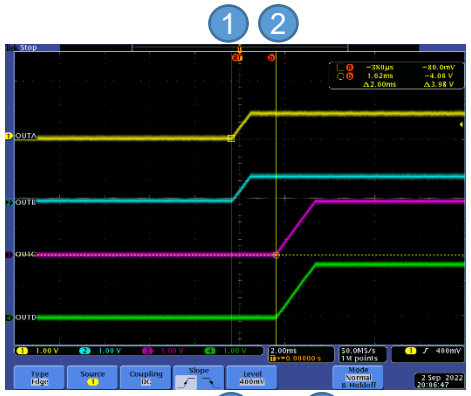
Max Load



- ❑ 0.18% (3.20 mV) peak-peak ripple at Standby
- ❑ 0.22% (4.00 mV) peak-peak ripple at Half-Load
- ❑ 0.27% (4.80 mV) peak-peak ripple at Full-Load

Power On Sequencing

MP5475-001C



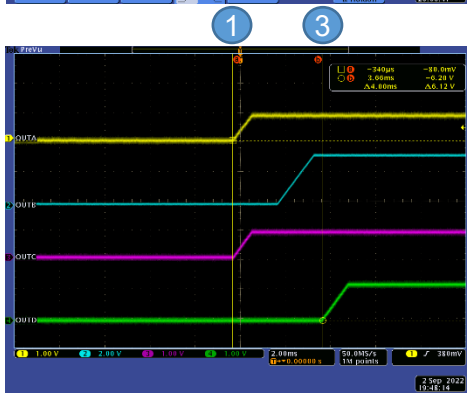
VCC_PSINTFP, VCC_PSINTFPDDR

VCC_PSINTLP

VCCAUX, VCCADC, VCCAUX_IO

VCCO_PSIO (0:3), VCCO_PSADC, VCC_PSAUX

MP5475-001B



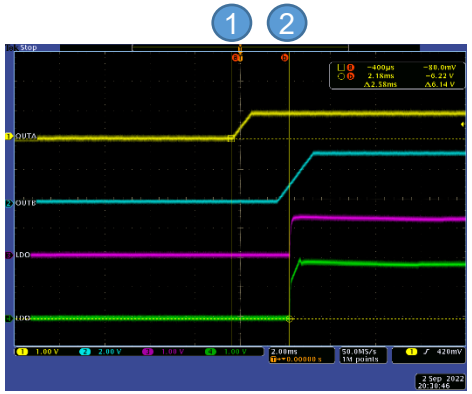
VCCINT

LDO, DDR, 3.3V Enet

VCCINT_IO, VCCBRAM

VCCO_PSDDR4_504

MP5475-001B
+
MP2002A



VCCINT

LDO, DDR, 3.3V Enet

VCC_PSPLL

VCC_PSDDR_PLL

Power Off Sequencing

MP5475-001C

VCC_PSINTFP, VCC_PSINTFPDDR

VCC_PSINTLP

VCCAUX, VCCADC, VCCAUX_IO

VCCO_PSIO (0:3), VCCO_PSADC, VCC_PSAUX

MP5475-001B

VCCINT

LDO, DDR, 3.3V Enet

VCCINT_IO, VCCBRAM

VCCO_PSDDR4_504

MP5475-001B
+
MP2002A

VCCINT

LDO, DDR, 3.3V Enet

VCC_PSPLL

VCC_PSDDR_PLL

MP5475 Result Summary

Rails		Vo (V) No load	Vo (V) Half load	Vo (V) Full load
VCC_PSINTFP	(0.85V/3.7A)	0.855	0.850	0.851
VCC_PSINTLP	(0.85V/0.6A)	0.855	0.854	0.854
VCCAUX	(1.80V/1.1A)	1.805	1.805	1.800
VCCO_PSIO	(1.80V/0.5A)	1.805	1.805	1.805
VCC_PSPLL	(1.20V/0.2A)	1.218	1.217	1.215
VCCINT	(0.85V/4.0A)	0.855	0.849	0.850
VCCINT_IO	(0.85V/0.6A)	0.855	0.854	0.854
VCCO_PSDDR4	(1.20V/1.2A)	1.205	1.204	1.201
VCC_PSDDR_PLL	(1.80V/0.5A)	1.805	1.805	1.800

MP5475 Result Summary

Rails		Ripple No Load	Ripple Half Load	Ripple Full Load	Pwr ON Seq
VCC_PSINTFP	(0.85V/3.7A)	0.78% (6.60mV)	0.78% (6.60mV)	0.80% (6.80mV)	1 (0ms)
VCC_PSINTLP	(0.85V/0.6A)	0.78% (6.60mV)	0.78% (6.60mV)	0.75% (6.40mV)	1 (0ms)
VCCAUX	(1.80V/1.1A)	0.73% (13.2mV)	0.73% (13.2mV)	0.80% (14.4mV)	2 (2ms)
VCCO_PSIO	(1.80V/0.5A)	0.73% (13.2mV)	0.80% (14.4mV)	0.84% (15.2mV)	2 (2ms)
VCC_PSPLL	(1.20V/0.2A)	0.22% (4.00mV)	0.18% (3.22mV)	0.22% (4.00mV)	2 (2.58ms)
VCCINT	(0.85V/4.0A)	0.78% (6.60mV)	0.73% (6.20mV)	0.94% (8.0mV)	1 (0ms)
VCCINT_IO	(0.85V/0.6A)	0.78% (6.60mV)	0.78% (6.60mV)	0.75% (6.40mV)	2 (2ms)
VCCO_PSDDR4	(1.20V/1.2A)	0.80% (9.60mV)	0.80% (9.60mV)	0.83% (10mV)	3 (4ms)
VCC_PSDDR_PLL	(1.80V/0.5A)	0.18% (3.22mV)	0.22% (4.00mV)	0.27% (4.80mV)	2 (2.58ms)